TIM: PLDs

Device Type

- Lattice (formerly Vantis/AMD) Mach4 and Mach5.
- Electrically, erasable, CPLDs. Programmed in-circuit via JTAG pins.

Design Environment

- Proprietary Vantis/AMD compiler.
- Text files:
  - Source (.src): “the design.”
  - Stimulation (.stm): expected inputs.
  - Physical information (.pi): maps signals to pins.

  are used to generate device simulation results (.sim) and programming files (.jed)
- Only Mach devices can be fitted.

Design, Simulation & Fitting Process

- Write .src file. Compile until no errors. (eg, pld5.src)
- Write .stm file. Simulate and check results (eg, pld5.sim)
- Fit device using chosen part fixing particular signals to pins (.pi) if required.
- Fix all signals to fitter assigned pins (.pi). Compile again.
- Add spare pins (.pi) and final compile.

Code Design Management

- Version control same as used for CLOAC boards.
- Differing versions stored in separate date labelled directories.
- All files associated with that version stored together.
- We are considering migration to CVS use in future.

TIM: PLD Fitting and Programming

Pin Assignment Strategies

- Register clocks fitted to clock pins where possible.
- Some busses were initial fitted in byte blocks but it was found this limited fitting resources.

Fitting

- First fit without any constraints.
- Then, fit with important signals eg clocks.
- Refit, fixing all pins to fitter defaults.
- Add 48 spare lines (4 x 8bit global + 2 x 8bit selected.)

Device Utilisation

	Pins	Macrocells	Routing	Device
PLD1	88	17	35	M5-384/184-7HC
PLD2	60	68	61	M5 512/256-7AC
PLD3	66	44	49	M5-384/184-7HC
PLD4a	61	21	53	M5-384/184-7HC
PLD4b	67	23	56	M5-384/184-7HC
PLD5	80	24	40	M5-384/184-7HC
PLD6	88	23	20	M4 256/128-7YC
PLD7	86	38	63	M5-384/184-7HC
PLD8	57	16	39	M5-384/184-7HC
PLD9	85	26	26	M5-384/184-7HC

Programming

- Devices programmed in accordance with Lattice guidelines.
- Lattice software used to program devices via a 2m lead connected to a PC parallel port.
- All JTAG signals buffered in/out of the board.

TIM: Other PLD Issues

Timing Verification

- Limited timing verification is possible post-fitting.
- Timing report can be generated showing all signal propagation times through PLD.
- The report is not interactive and can be difficult to interpret.

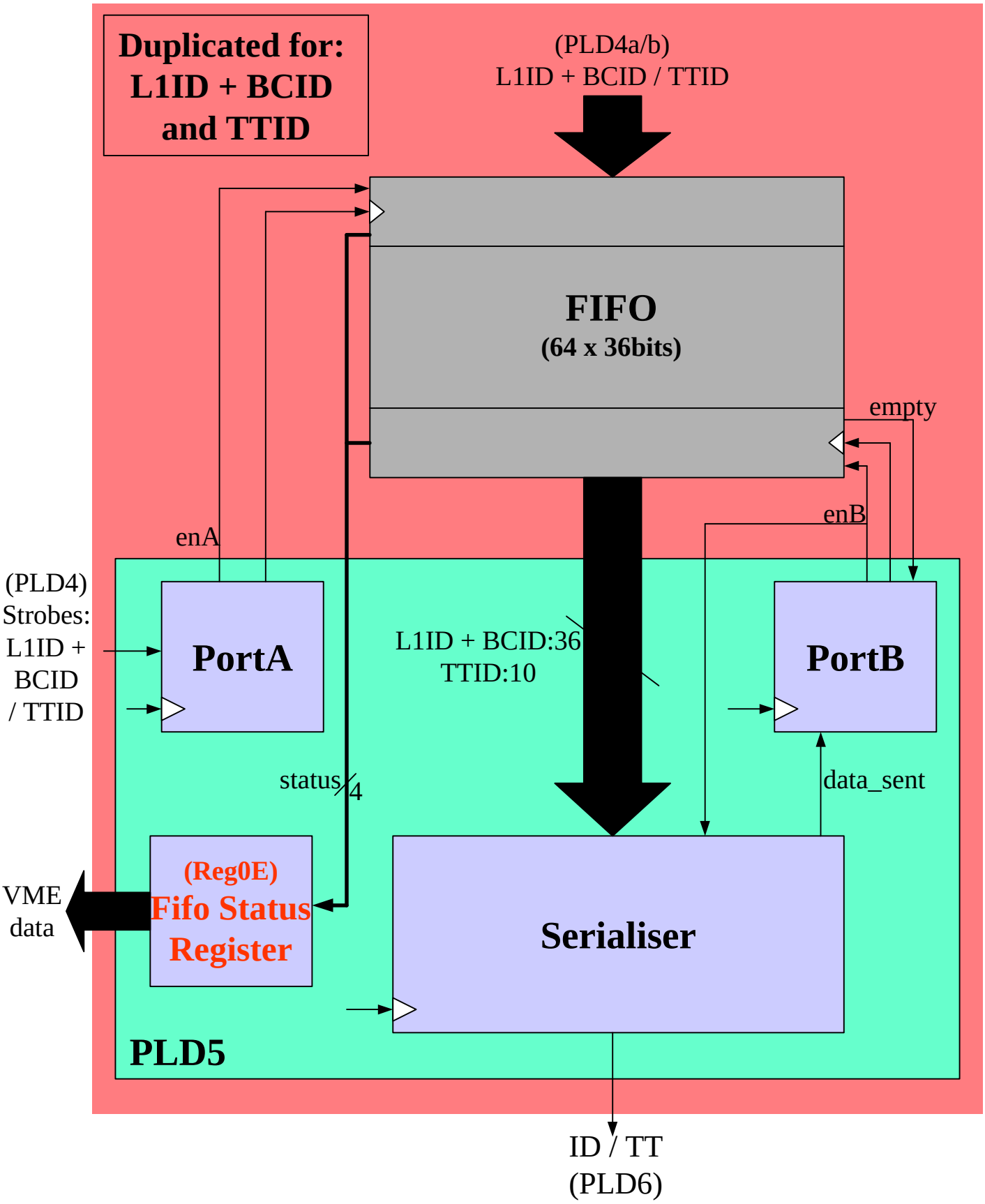
Reset Philosophy

- All registers (flip-flops) connected with a global reset line.

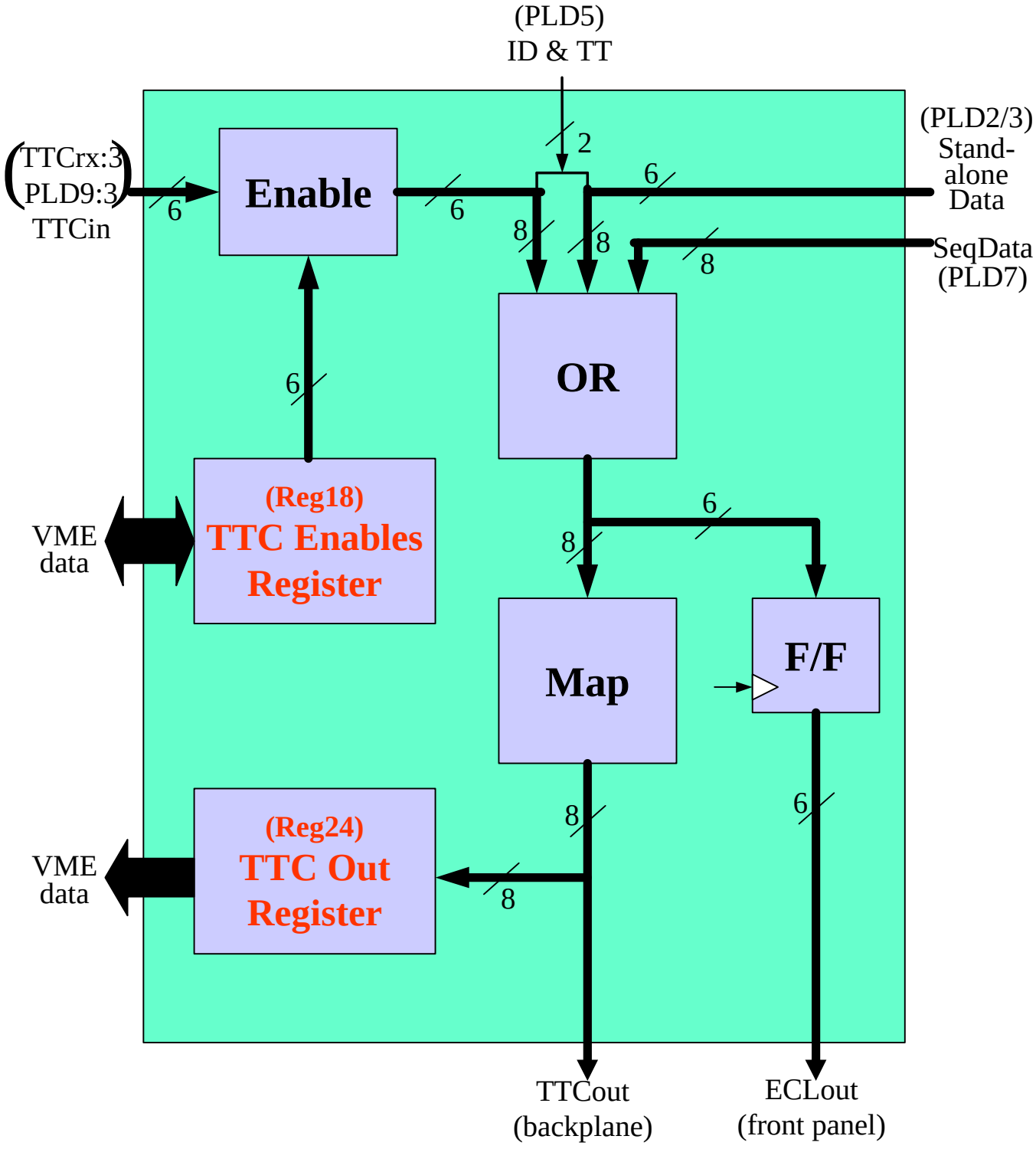
ESD Reduction

- No direct connection of any PLD pin to the outside world. (to help address ESD concerns)

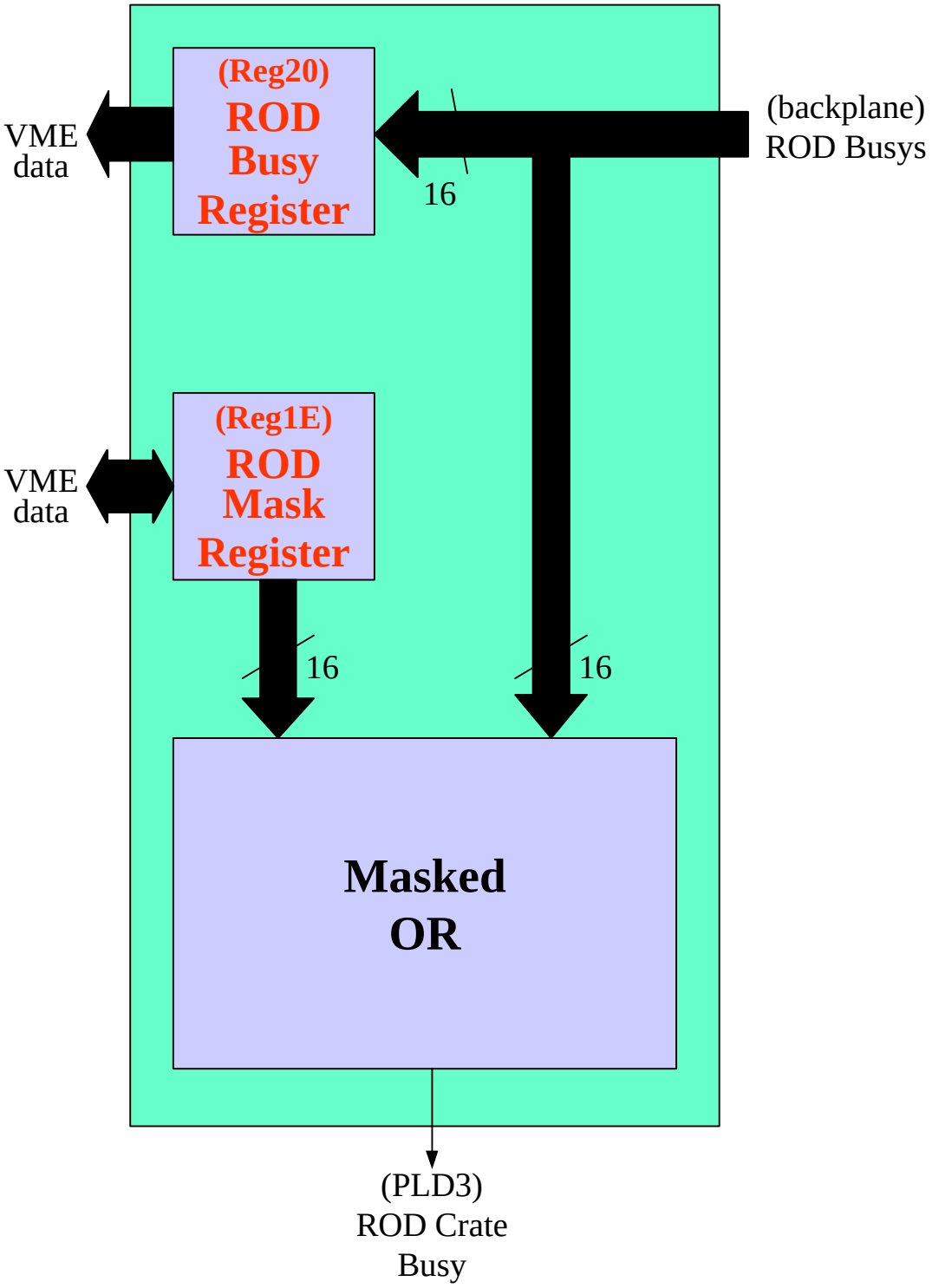
TIM: PLD5 & FRIENDS



TIM: PLD6



TIM: PLD8


(Reg20)
ROD
Busy
Register
VME
data
16
(backplane)
ROD Busys
(Reg1E)
ROD
Mask
Register
VME
data
16
16
Masked
OR
(PLD3)
ROD Crate
Busy