Physics & Astronomy
HEP Electronics

TTC Interface Module for ATLAS Read-Out Electronics:

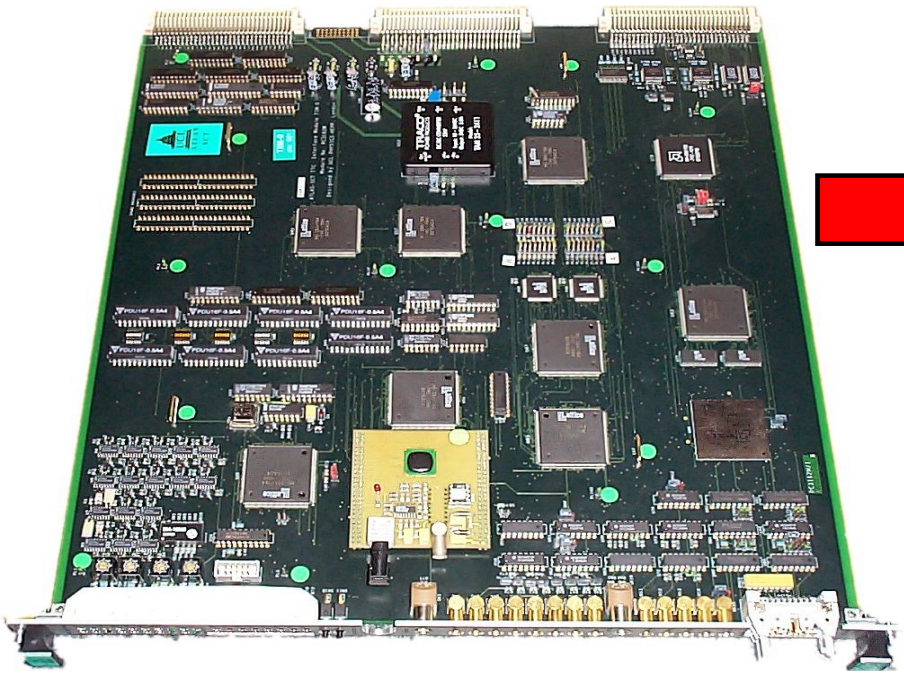
Final production version based on Xilinx FPGA devices

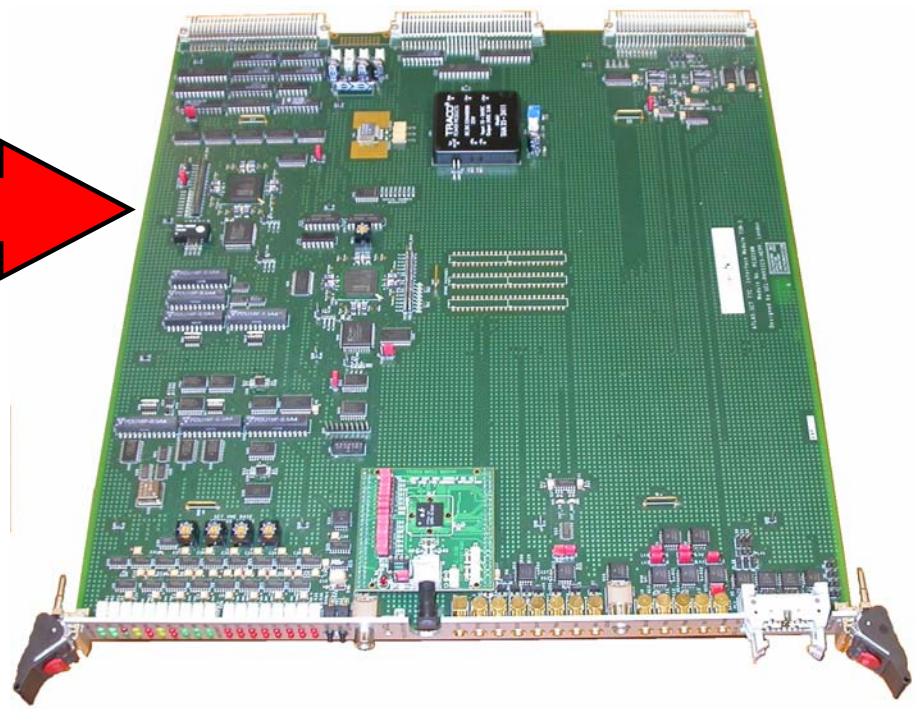
LECC 2004

Matthew Warren
warren@hep.ucl.ac.uk
Jon Butterworth, John Lane, Martin Postranecky

Outline

- Introduction to TIM - ~~detailed description~~
- Changes/additions to TIM design.
  - Hardware.
  - Firmware.
- Fixed Frequency Trigger Veto (FFTV).
- Status/Future.

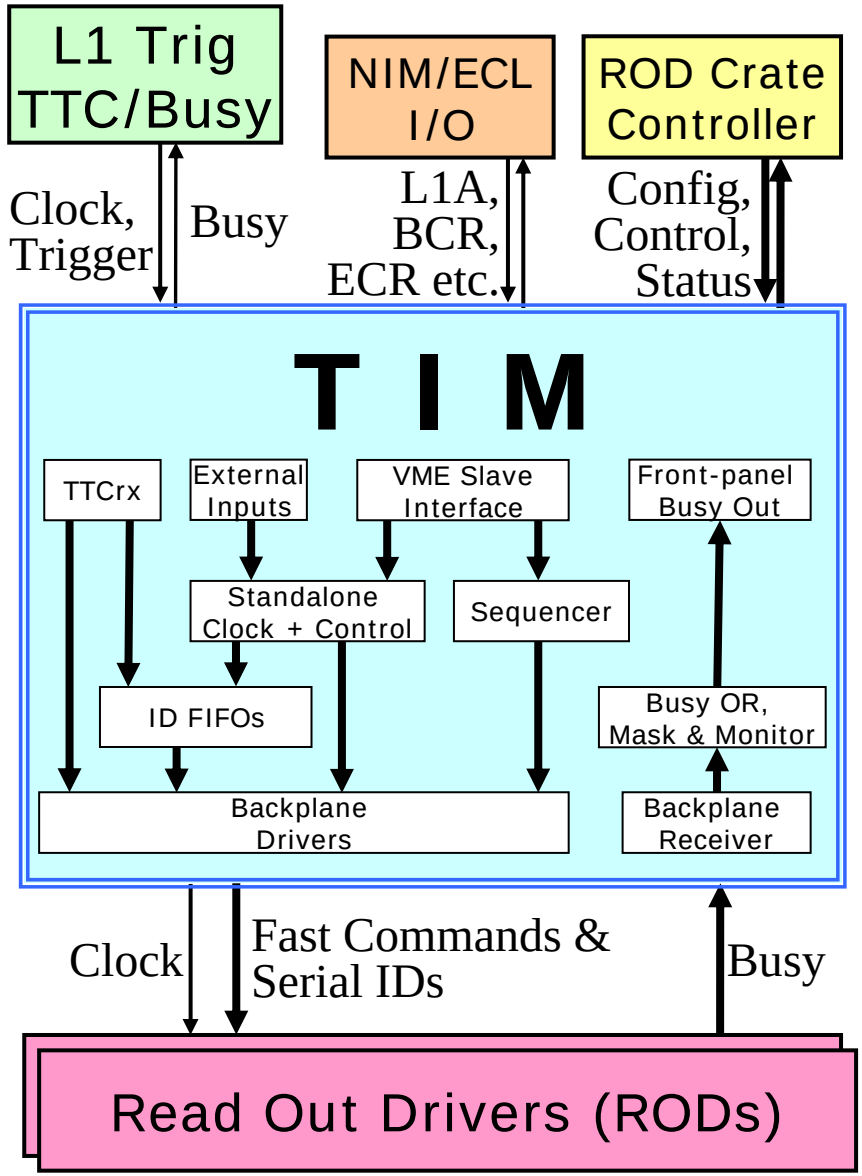




Introduction

TTC (Trigger, Timing & Control)
Interface
Module

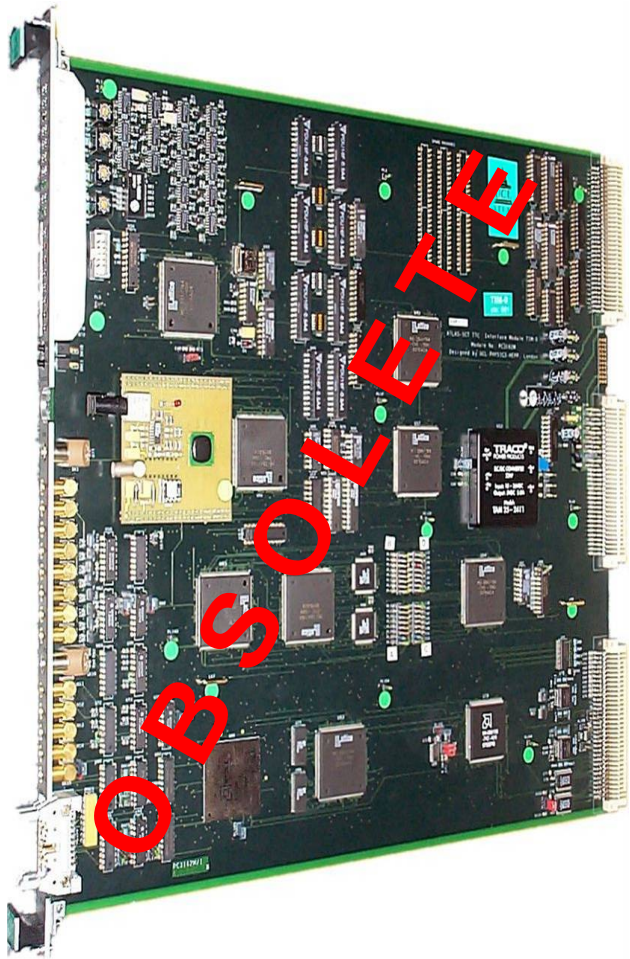
- Interfaces ATLAS L1 Trig to SCT, Pixel, MDT & CSC RODs over a custom J3 backplane.
  - IDs serially.
- TTC Clock & Trigger IN. Busy OUT.
- Stand-alone mode:
  - Generates TTC-like signals.
  - External inputs.



Hardware: Changing …

Prototype-TIM:

- AMD/ Lattice MACH5 CPLD
  - Devices now obsolete.
  - Firmware obsolete (DSL , MachXL).
- Worked to spec, but change requests happen – ECR-ID, TTCrq
  - Spare resources scattered.
  - RAM/FIFO fixed



Production-TIM Goals:

- More TIMs!
- Drop in replacement for prototypes.
- Well supported/maintainable firmware.
- Room to grow (e.g. orbit counter, busy analysis).

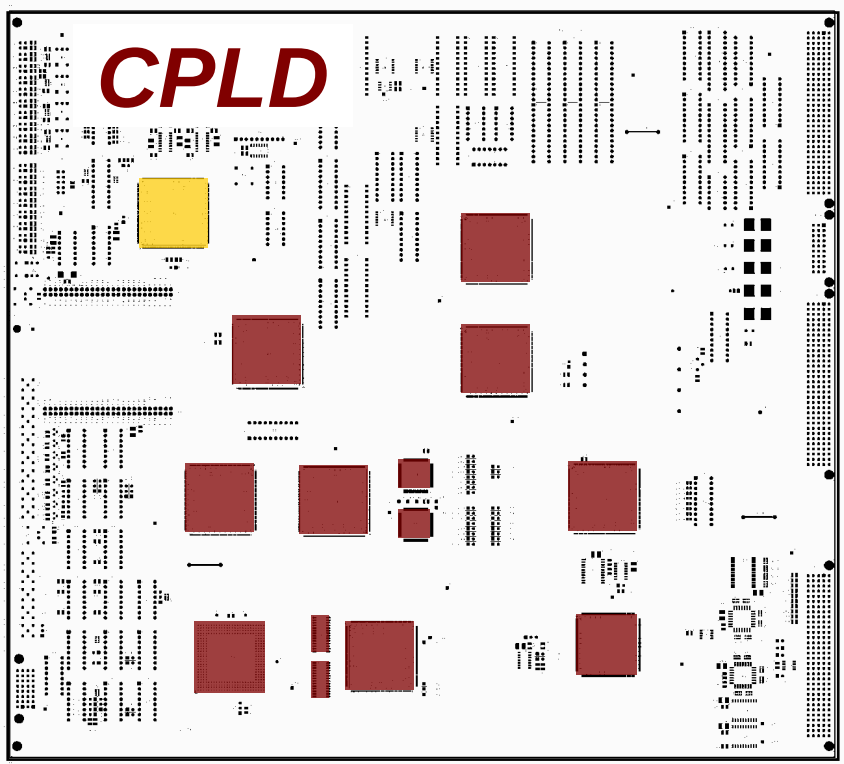
… from CPLD to FPGA

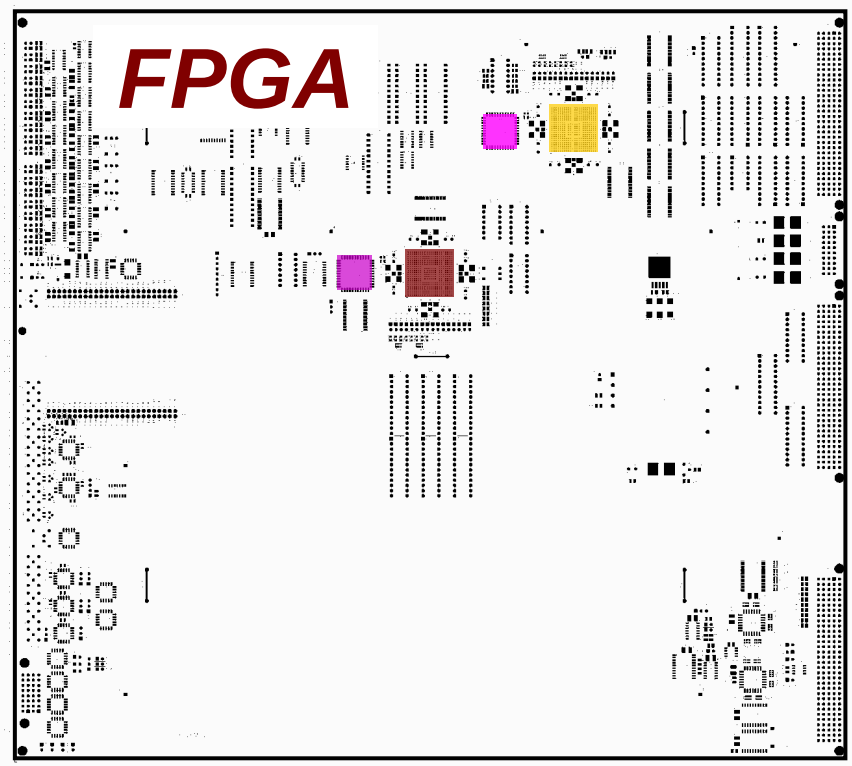
FPGA: much more logic & RAM/FIFO **&** cheaper.

- 10 CPLDs + RAMs + FIFOs = 2 FPGAs

Xilinx Spartan IIE family chosen:

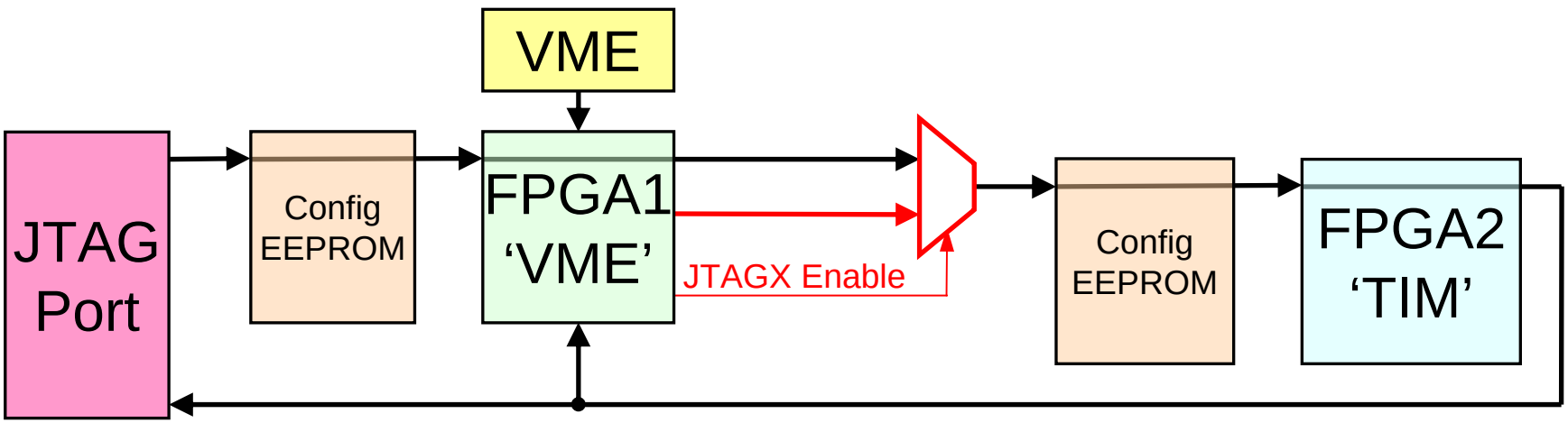
- Our friends use Xilinx & Spartan much cheaper than Virtex II.
- 600E part released 2003 (not obsolete!) + matched our needs.



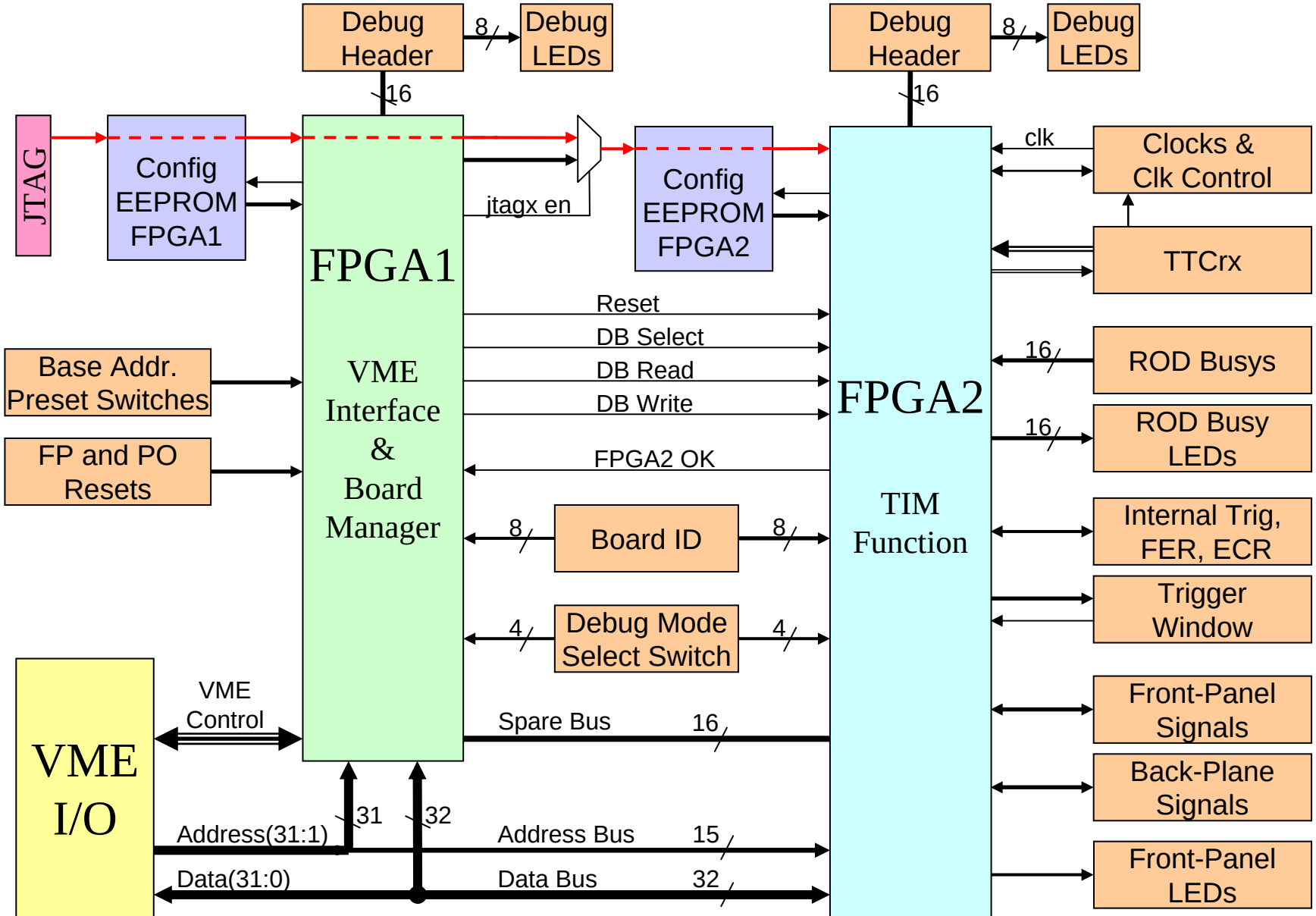


Hardware Changes II

- Clocks controlled via dedicated fail-over, glitch-free MUXs.
- TTCrq QPLL control connector added and routed to FPGA.
- 32 bit VME data bus connected (was only 16 bit).
- Busy TTL-OC out (jumper selected) – wire-OR of busy.
- Remote firmware update:
  - FPGA1 is VME interface – code stable quickly.
  - FPGA2 handles TIM functions, so more likely to be modified.
  - FPGA1 can intercept JTAG chain under software control.



Hardware Functional Layout



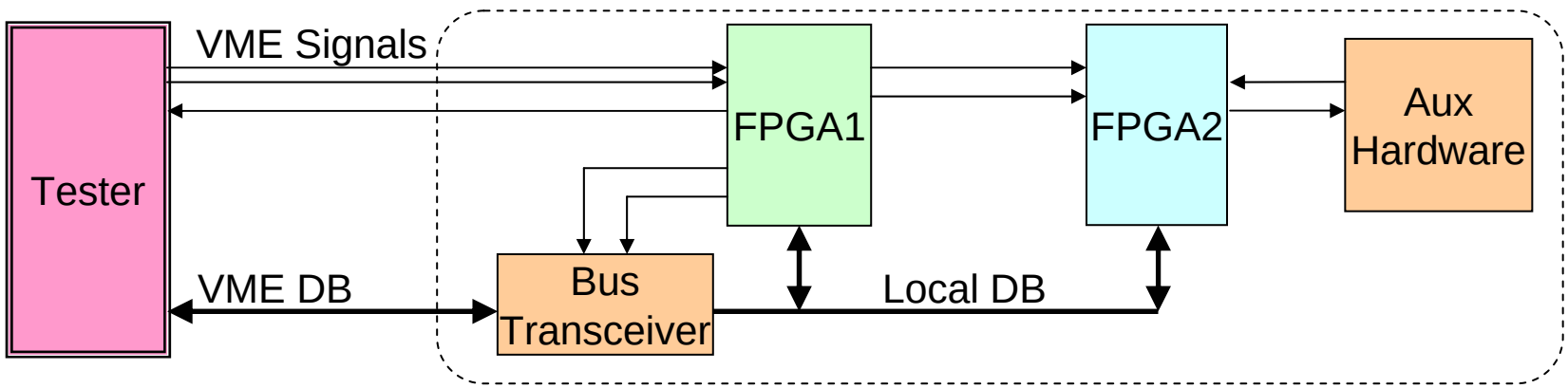
MRMW v1.2 13-09-04

Firmware

- Written in VHDL.
  - Widely supported by hardware & software vendors.
- Structured around original CPLD blocks.
  - Retro-fit to CPLDs possible (but not efficient).
- Synchronous design always, except:
  - External NIM/ECL signals input as clocks to FFs.
- Tools:
  - Mentor Graphics FPGA Advantage.
  - Xilinx ISE.
- Functionally not different from prototype, except:
  - Wider FIFO for ECR-ID
  - More debug registers.
  - Fixed Frequency Trigger Veto for resonant wire-bonds (more later).

Simulation

- *ModelSim*.
- Simulation fast enough to carried out at FPGA level.
  - Post place-and-route too.
- Test-bench includes both FPGAs and other components.
- Tester drives the board from the 'VME connector'.
  - Procedures written to do bus-like reads/writes.
  - Testing via routines similar to those in the test software.



FPGA Resource Utilisation

- Plenty of room for growth!

From Xilinx ISE Place & Route Report:

FPGA1

Number of External GCLKIOBs	1 out of 4	25%
Number of External IOBs	161 out of 285	56%
Number of BLOCKRAMs	4 out of 14	28%
Number of SLICEs	**280 out of 2352**	**11%**
Number of DLLs	1 out of 4	25%
Number of GCLKs	1 out of 4	25%
Number of TBUFs	128 out of 2464	5%

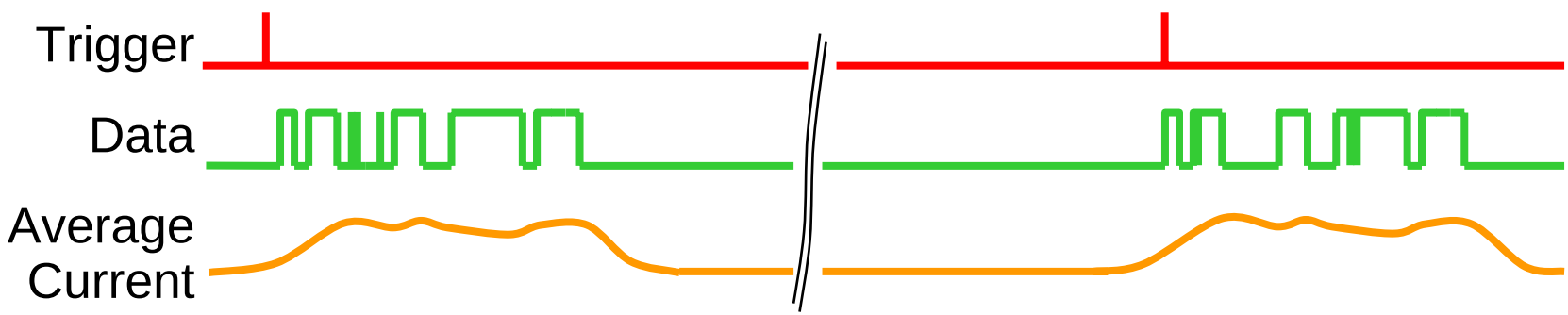
FPGA2

Number of External GCLKIOBs	2 out of 4	50%
Number of External IOBs	244 out of 325	75%
Number of BLOCKRAMs	**64 out of 72**	**88%**
Number of SLICEs	**1843 out of 6912**	**26%**
Number of DLLs	1 out of 4	25%
Number of GCLKs	1 out of 4	25%
Number of TBUFs	160 out of 7104	2%

Resonant Wire-Bonds

[Summarised from "Resonant Bond Wire Vibrations in the ATLAS SemiConductor Tracker" by T. J. Barber et al., Accepted for NIM, CERN-04-053]

- Triggers induce large variations in current in some wire-bonds as they read-out.
- CDF saw wire-bonds break with trigger rates close to their mechanical resonant frequency in a strong magnetic field.
- Physics triggers are 'random' but, calib./test triggers often at fixed frequencies. e.g. 1 bunch LHC runs – 11.2kHz
- Work has been done to evaluate the effects of this problem on the ATLAS SemiConductor Tracker (SCT).



Experimental Results

- SCT like wire-bonds were operated in 1.8T magnetic field.
- Resonances seen from 15kHz – 90kHz.
- Failures observed after a few minutes.
- Found NOT to have large affect on SCT
  - barrel orientation good
  - end-cap uses very short bonds.
- BUT may have implications over the life-time of detector.

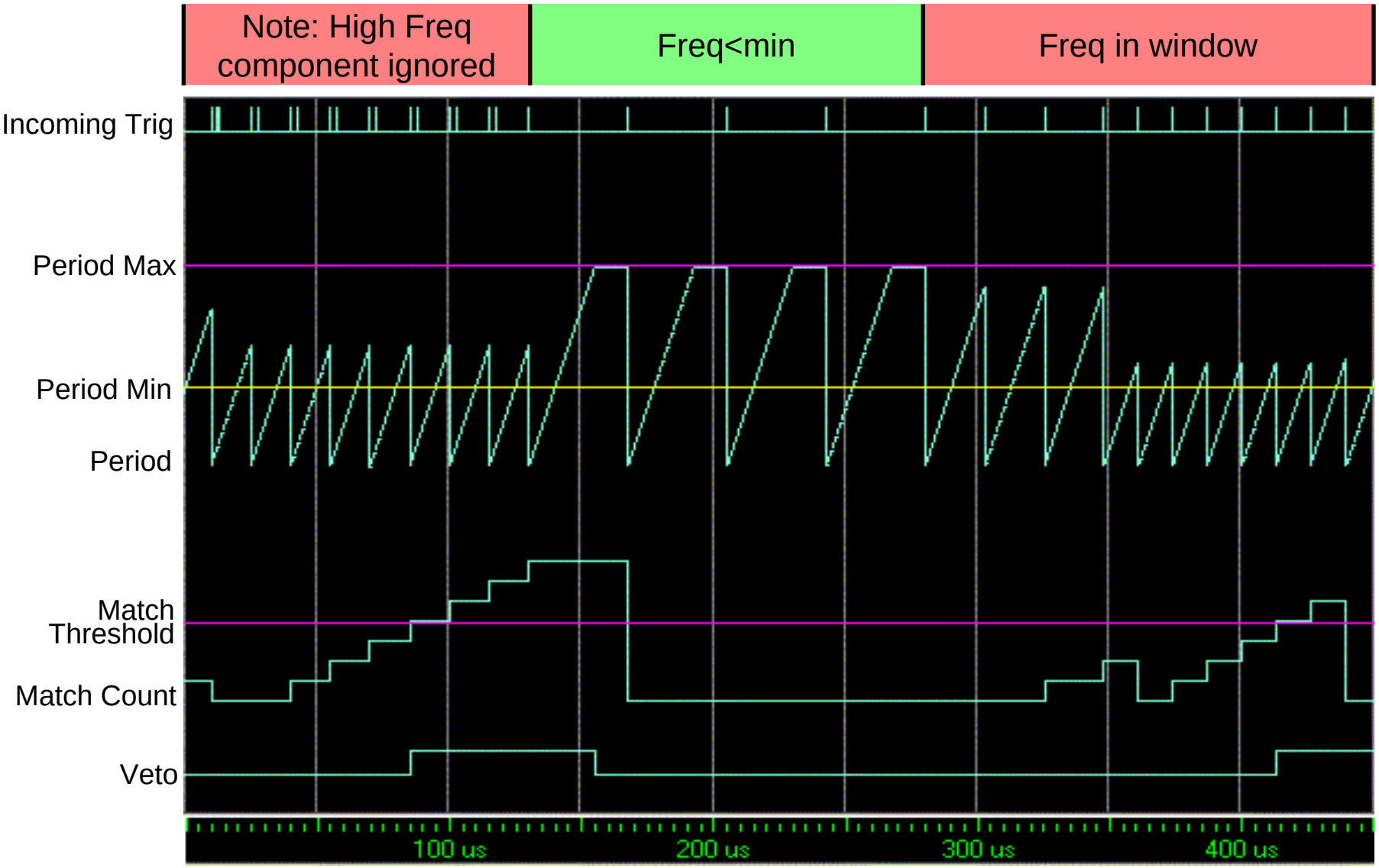
Photo showing a wire-bond with a current of frequency 15 kHz - off resonance.

Current frequency 17 kHz - on resonance

FFTV: Fixed Frequency Trigger Veto

- FE components too far into production to fix at source.
  - 'Avoidance' techniques required.
- TIM is well located for this in the trigger tree:
  - sub-detector specific and handles busy.
- Algorithm (enhanced CDF version):
  - Compares successive trigger periods, increments counter if matching (within programmable 'tolerance').
  - Generates a Veto when match counter hits preset limit.
  - Period Max setting allows passing of low-freq triggers.
  - Period Min setting allows high freq triggers to be ignored.
- Missing triggers would cause a big problem – L1ID?
  - In stand-alone mode, triggers are 'killed'.
  - In run-mode the busy is asserted.
  - Counter keeps track of time in FFTV state for stats.

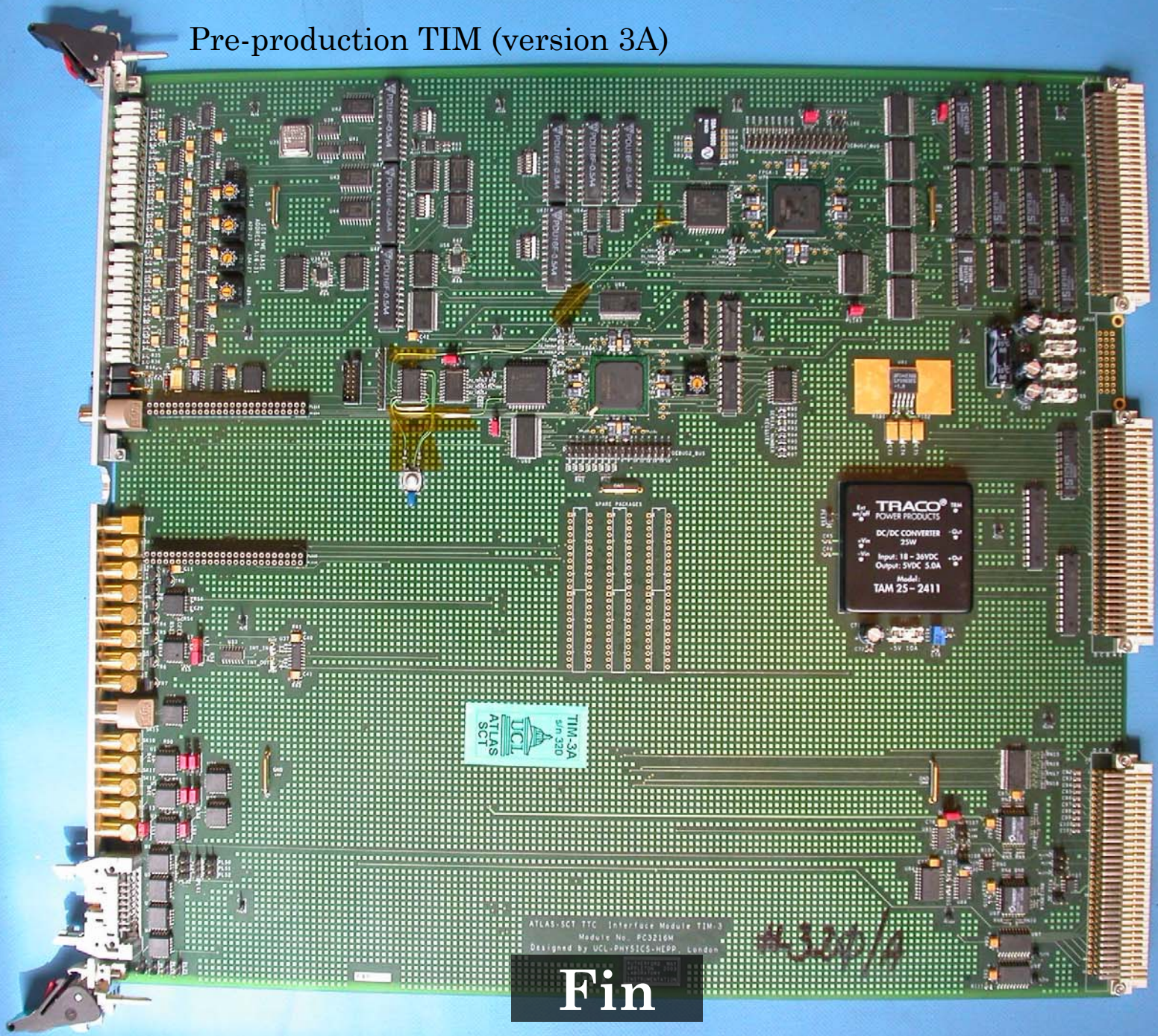
FFTV System Simulation



Status/Future

- 2 Pre-production TIMs manufactured and tested.
  - Replaced prototype in SCT ROD test setup in Cambridge without problems.
- Passed FDR in June.
- 4 pre-series being assembled now.
  - JTAG testing next week, ready by October.
- User evaluation (incl. test beam?).
- Q1 2005 – 16 more for all SCT & Pixel needs.

Pre-production TIM (version 3A)



Fin