U N I V E R S I T E D E P A R I S - S U D
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NEMO III , GEIGER ACQUISITION

NOTE: ***This text is written with MicrosoftWord, and uses the hyper word link(*** blue ***underligned words)***
From one linked board, to come back to the main text ,use the left ***green/blue*** ***arrow at the board top***

01 GENERAL INFORMATIONS *

- The main goal of the NEMO3's detector is to search for neutrinoless double beta decay.

- The Nemo3 detector is located in the LSM (laboratoire souterrain de Modane).
  (see board 077, « lsm »)

- The geiger electronic acquisition (like all the electronics, calorimeter etc..) is external to the detector, and it is located under this detector,in 4 cabinets bays .
  (see board 069, « geiger cabinets bay position »)
  (see board 073, « frame detector 1 »)
  (see board 075, « frame detector 2 »)
  (see board 078, « frame detector 3 »)

- The design of the geiger electronic started in 1996 to finish in 2001.
- This geiger user's manual is CD stored, and goes with :
  - an archiving « *red book* » which contains :
    - electronic schemes
    - software programs

    there are only 4 *red books* specimens

  - more than 180 boards.
    (see board 125, « boards list ,direct linking »).

- All references,sources,designer and contacts names etc.. are in :
  (see board 124, « references,sources,designers,contacts »)

02 GENERAL DESCRIPTIONS *

Note :
to see this chapter is sufficient to understand without deepening.

02_01 Geiger detector:

There are 18 layers of cells per sector (9 internal, 9 external)
(see board 000, « one sector »)
(see board 001, « nemo3 synoptical acquisition »)
(see board 054, « the detector »)

3x12 + 2x14 + 4x16 + 4x18 + 2x20 + 3x23 = 309 cells per sector, there are 20 sectors :
20 x 309 = 6180 cells
There are 3 signals per cell (one anode A, 2 cathodes Kh high, Kb basse/low):

3 x 6180 = 18540 signals
note: the electronic geiger acquisition possibilities are: 40 x 3 x 160 = 19200 signals, or 6400 cells, thus there are inputs which are not used.

02_02 Geiger acquisition:

(see board 000*, « one sector »)*
(see board 001*, « nemo3 synoptical acquisition »)*
(see board 034*, « picture 2, acquisition geiger card»)*

(see board 017*, « timing »)*
(see board 018*, « dialog trigger geiger »)*

a) the trigger sends to the geiger acquisition a *start mesure* signal
b) From each struck cells leave three signals :
(see board 024*, « signals »)*
A : anode signal
note : a ***hit*** is an A signal digital TTL formated
Kh : high cathode
Kb : low cathode
- the A signal starts three electronic counters A, Kh and Kb
- the Kh and Kb signals stop respectively the Kh and Kb electronic counters
- evry 102µs all counters are set to zero(raz),by an internal geiger signal, named « *time out* » .

c) An « *or electronic wired* » of the *hits* of the cells from one layer generates a ***HIT.***
There are *18layers* x *20sectors* = *360 HITS*

The trigger receives these *HITS*, adjusts their time to about 5µs, and according to its decoding configuration generates a three signals event :

- *trigger signal*,or still named « *stop time out* », this signal stops the raz counters , which if not occurs every weekevry 102µs.
- *stop A* ,to stop the A counter
- *stop mesure*, to stop the acquisition

notes :
* between the stop A and the stop mesure signals, there is an α observation time.
* between the start mesure and the stop A signals, there is a β observation time.

d) the LSM software geiger acquisition is assured thanks to Lynx with Cascade,and a C compilator .

e) The LSM hardware acquisition is assured thanks to **2**

hardware branchs with each one :

a) 4 VME geiger cages no standardized with 21 slots
- slots 1 to 20, 20 geiger acquisition cards
- slot 21 ,one CES VME VMV VIC8250 card controller

b) 4 insulators distribution crates

c) 4 slow control, interlocks crates

total hardware :
- 8 geiger cages (2 cages per bay,there are 4 bays)
- 20 VME geiger cards per cage (2,5 sectors per cage)
- 20 x 8 = 160 VME geiger cards
- 8 auxilaries slow control crates(2 crates per bay)
- 8 HV insulators distribution crates(2 per bay)

(see board 068, « general system acquisition »)
(see board 065, « 2 vmv branches »)
(see board 013, « cages implantation »)
(see board 014, « 4 cabinets bays »)

02_03 Auxilaries electronics Geiger:

a) insulator distribution:

➔ *(see board 163, « insulator principal document »)*

(see board 015, « insulator_1,theorical scheme »)
(see board 016, « insulator_2,mother card »)
(see board 037, « picture 5, insulator distribution »)
(see board 013, « cages implantation »)
(see board 014, « 4 cabinets bays »)

- There are 8 insulators distribution crates, one for each geiger VME cage.
- There is one insulator distribution mother card for each VME geiger card(160).
- There are 20 insulator distributor mother cards per insulator crate(like geiger cages)
- There are 15 daugthers card per insulator mother card total : 15 x 160 = 2400 daughter cards
- There are 18 different HV possibilities values because of the 18 layers of cells
- The goal of the insulator distribution is :
  - ¤ to put the anodes of the detector cells to HV (and the cathodes to some hundreds of volts)
  - ¤ to insulate from the HV the anodic and cathodic detector signals, and to transmit them to the geiger acquisition

- Like the VME geiger cages there are :

* two insulators crate per cabinet bay,
* 160 mother cards
* one insulator card for each VME geiger card
* each insulator card insulates 40 cells :
  - 40 anodes
  - 40 high cathodes
  - 40 low cathodes

- Each daughter card insulates 8 signals(anodes or cathodes)
- The 15 daughter cards of an insulator mother card are :
  - ¤ 5 daughter cards anodes
  - ¤ 5 daughter cards low cathodes
  - ¤ 5 daughter cards high cathodes

b) slow control, and interlocks: (goto slow control chapter)

(see board 060, « interlocks and secutities cages »)
(see board 014, « interlocks and 4 cabinets bays »)

the goal of this control is :

- to survey relatively slowly, all the voltages, currents,temperatures etc..via*Labview* software,and to warn the operator, with an alarm message
- to generate fast interlocks to stop the 220v AC geiger cage power ,when there are important defaults like excess of temperature,fans problems etc..

c) bench LAL tests and maintenance: (goto bench maintenance)

the goal of the LAL bench :

- was to test the prototyping acquisition geiger cards

- was to make a lot of acquisition runs with the 9 and 20 cells chambers manufactured by the LAL's physicists
  (see board 041, « 20 cells LAL chamber »)

- was to test the 175 geiger cards after wiring

- was to test the 8 geiger cages , the 8 slow control crates (during a lot of weeks,night and day), before their deparature to the LSM.

- and ***now*** to assure the geiger cards maintenance

notes :

- OS9 and MicroWare C compilator are the bench LAL software
- The bench hardware LAL is composed of:
  - 3 CES manufactured VME cards
  - 3 LAL designed VME cards

d) LSM cabinets bay:

(see board 013, « cabinet bay »)
(see board 014, « interlocks and 4 cabinets bays »)

- There are 4 cabinets geiger bays :bay B10,20,30,40

- A cooling 2 fans extractor is installed on the right hand of the bay

- An evacuation of the calories of all bays (not only geiger bays) is envisaged ,but not made at this date

- In one cabinet bay there are :
  * 2 VME geiger cages cooled individually
  * 2 insulators distribution crates,without individual cooling
  * 2 slow control crates,without individual cooling

*03 GEIGER ASICS **

03_01 Asics generalities:

asic :application specific integrated circuit

(see board 010, « synoptical scheme of digital and analogical asic »)

- The asics always go by couple, one analogical asic with its digital asic
- One pair of ASIC contain 4 whole electronic cells acquisition(4 anodes, 4 high cathodes,4 low cathodes)
- There are 10 couples of asics per geiger card , total: 160 x 10 = 1600 couples of asics
- The asics are welded (like all the others integrated circuits) directly on the geiger card

03_01 Analogical asics:

- designed by LAL, manufacturing by CMP (in AMS 1.2µm CMOS technology) and package in PLCC44
  (see board 039, « asics package »)

- LAL sorting and debuging, with a special designed LAL bench(not here discribed),without burning

  (see board 010, « synoptical scheme asic »)
- One quarter of an analogical asic is made of :

  - 3 analogical current to tension amplifiers
  - 3 analogical tension comparators

analogical current to voltage amplifier note:
an input current of 100uA gives 1.7V at the preamplifier output.

with Zin=250Ω,and Iin=100µA
there is :Vin= 25mv,thus G = 1700/25 = 68

here is the empirical calibration graph:
(see board 022, « calibration method »)
(see board 023, « calibration threshold »)
(see board 024, « signals »)
note: the threshold calibration is fixed definitively by hardware on the geiger card, here is an example of different experiments before to choose the best and final calibration
(see board 027, « calibrations experiments »)

- The analogical threshold of the comparator comes from a 8 bits (256 resolution steps), DAC (digital to analogical converter) located in the numerical asic
- The digital TTL output of the analogical comparator sends a signal to the asic digital counters to start or to stop the the counters
- The inputs of the analogical asic can come from 3 places:
  * in *normal mode*,from the detector cells, via an external insulator distribution, through an internal « ***smc*** (surface mounting component)» protection capacitor welded on the geiger card.

  * in *dynamic gene40 tests mode*,from the gene40 card (go to see gene40 card)

  * in *static tests mode*, named "*external analogical tests*", from the digital asic, in this case the A,Kh and Kb signals are known and calibrated thus,they can be easily compared:
    ¤ the digital asic generates
      - one analogical A signal
      - one analogical K signal,identical for Kh and Kb
      note:
        * these analogical signals are digital signals from the numerical asic,shunted and filtered
        * in fact the K signal is doubled, and separated from a few seconds ,only the first signal is taken into account

    ¤ the level of these tests signals generated by the digital asic are voluntarily low, because of crosstalk, thus it is necessary to respect a threshold gap in tests mode :
    (see board 023, « calibration threshold »)

    ¤ the A and K *tests values* are stored in a HD (hard disk)file,this file can be modified, however it will be necessary to replace the original A and K

tests values in this file, to do not generate defaults during the tests programs

note: * the *tests values* are identical for the 2 modes : "internal digital tests" and *"external analogical tests"*
* A and K *tests values* are the number of ticks (counter pulses) between A and K signals

(see board 129, « OS9 nemo3 »)
(see board 157, « OS9 primary menu 1»)
[***Y)*** and primary menu] *storing file modifications*
[***n) k) l)*** primary menu] *external tests*

note: there are 10 *tests values* per card, one per asic therefore :
10 x 160 = 1600 *tests values* stored
(see board 131, « salvar »)
(see board 130, « read me salvar »)

¤ - the signals : *start mesure*
stop time out
stop mesure
are generated by the digital asic
- *stop A* signal :
* if it is not present,the A counter is stopped by the *stop mesure* signal
* if it is generated by the trigger,the A counter is stopped prematurely by the *stop A* signal

¤ the resolution tick is 80ns
note :the 20ns of resolution tick is only during the acquisition mode

- ***Wrong α***,there is a possibility to get a wrong α event:
* because of the anodic cell signal aspect (crosstalk A with K in the detector)
(see board 025, « wrong alpha 1 »)

An alpha event is true if :
* the α counter is modulo 4096 of the A counter
* if not the α values counters have to be eliminated
* *example:*
Y = α counter / 4096.
Z = (int) Y
If (Y - Z) 4096 = A counter, it is a true α
(accept +- 2 ticks)

- ***about the crosstalk :***
¤ between the 4 cells of an analogical asic,the tests show there is a crosstalk,but it is eliminated with a threshold of 9mv
(see board 032, « crosstalk inter cells of an asic »)

¤ between inter analogical asics of one geiger card,there is no crosstalk, thanks to the work of meticulous person who positioned wire after wire, to correct the automatic wire positionning of the CAO
¤ between inter geiger cards,there is no crosstalk detected

03_02 Digital asics:

- Designed by LAL and manufactured by ES2 (1.0µm CMOS) in PLCC 68 package
  (see board 039, « asics package »)
- ES2 sorting and debuging,without burning,with LAL verifications

  (see board 010, « synoptical scheme asic »)
  (see board 009, « asic digital to asic analogical link »)

- One quarter of a digital asic is made of 2 nearly identical parts,each one made of:

  * a digital bloc coherence, which shows by means of a "*status register*" if the counters have been started after an struck cell,this "*status register" is made of:*
    4 fieds of 3 bits,b0,b1 and b2,one field for each cell
    notes: ¤ one asic receives 4 cells
    ¤ the A,Kh and Kb counters start simultaneously
    - b0 anode started(*hit*) ----> `1` ok
    - b1 high cathode,Kh stopped ----> `0` ok
    - b2 low cathode,Kb stopped ----> `0` ok

    example: 1 0 1 -> 5 Kb not stopped,Kh stopped,A started

  * 4 digital counters
    - two 12 bits (4096)counters for Kh and Kb
    - one 12 bits (4096)counter for A
    - one 17 bits (131072) counter α
      ¤ The time resolution of the counters is :
      * 20ns(50Mc/s) in *"mesure mode"* (named tick)
      * 80ns(12.5Mc/s) in "*tests mesure mode*"
      * this factor 4 because of the tests asic digital hardware cannot support 50Mc/s

- The digital asic generates from its internal 8bits DAC, to the analogical asic comparator,an analogical signal to fix the level of the comparator threshold of the analogical inputs signals of the cells.

  ¤ the *threshold values* are stored in a HD file, this file can be modified, however it will be necessary to replace the original *threshold values* in this file,to do not generate defaults during the tests programs
  (see board 129, « OS9 nemo3 »)

(see board 159, « OS9 primary menu 2»)

[**y)** and primary menu]
note: there are 10 *treshold values* per card, therefore 10 x 160 = 1600 *treshold values* stored
(see board 131, « salvar »)
(see board 130, « read me salvar »)

- there is a general electronic common to the 4 cells,of an asic, to generate tests signals,here is their descriptions:
(see board 010, « synoptical scheme asic »)

  * *Read and write AAA/555* :
  read or write of a digital hexadecimal word (AAA or 555) in the 16 (4 x 4) counters of an digital asic.
  * *Internal digital tests* :
  This function starts and stops the asic counters with the digital asic internal signals, **thus the analogical asic is not used.**
  In this case (like *"external analogical tests")* the A,Kh and Kb are known and calibrated by means of to the software,thus they can be easily compared:

    ¤ the digital asic generates
    - one digital TTL, A signal
    - one digital TTL, K signal,identical for Kh and Kb

    ¤ the A and K *tests values* are stored in a HD file, this file can be modified, however it will be necessary to replace the A and K original *tests values* in this file, to do not generate defaults during the tests programs
    note: the *tests values* are identical for the 2 modes *"internal digital tests"* and "external analogical tests"
    (see board 129, « OS9 nemo3 »)
    (see board 160 " OS9 primary menu 3")
    [**Y)** and primary menu] *storing file modifications*
    [**m) k) l)** primary menu] *external tests*
    (see board 131, « salvar »)
    (see board 130, « read me salvar »)

    ¤ - the signals : *start mesure*
    stop time out
    stop mesure
    are generated by the digital asic
    - *stop A* signal :
    * if it is not present,the A counter is stopped by the *stop mesure* signal
    * if it is generated by the trigger,the A counter is stopped prematurely by the *stop A* signal

    ¤ the resolution tick is 80ns

note :the 20ns of resolution tick is only during the acquisition mode

- ***Reading error counter***

obviously if a cell is hit 2 times during the 102µs of a time out, the reading counters of this cell is false.
(see board 028, « error if 2 events in a time out »)

- ***Reading error cell status coherence***

a lot of LAL tests with the 20 cells chamber, show there are some errors with the reading coherence of the *status register* of a cell(go to see coherence)
(see board 029, « cell status error »)
note : there never was coherence error with gene40 card tests

*04 GEIGER CARDS **

(see board 002, « VME card 1 »)
(see board 034, « VME picture »)

04_01 cards generalities:

- *All the 160 geiger VME cards are identical*
- One card,to the maximum,can receive 40 cells signals, 40 A,40 Kh,40 Kb
- The cells distribution of one sector is like this :

➔ *(see board 003, « sector dispatching layers »)*

thus certain cards don't receive 40 cells, there are cards with:

- 40 cells,and there are 3 types of them(types 1,2 and 3)
  (see board 004, « wired electronic or type 1 »)
  (see board 005, « wired electronic or type 2 »)
  (see board 006, « wired electronic or type 3 »)

- 39 cells,and there is 1 type (type 4)
  (see board 007, « wired electronic or type 4 »)

- 36 cells,and there is 1 type of them(type 5)
  (see board 008, « wired electronic or type 5 »)

These five configurations are imposed by the P' *« wired electronic or »* of the mother board of the geiger cage.

The recapitulation layers,sectors,geiger cages is

described in this following ***basic board*** :

➔ *(see board 038, « nemo cab »)*

note:

the 20 x 18 = 360 *HITS* are dispatched like this :

- 4 geiger VME cages of type I which generate 44 HITS
- 4 geiger VME cages of type II which generate 46 HITS
- (44 x 4) + (46 x 4) = 360 *HITS*

and this ***basic listing :***

➔ *(see board 083, « P' cab »)*

Here the listings of different cells marking

(see board 135 , « cell marking cage 0 and 1 »)

(see board 136 , « cell marking cage 2 and 3 »)

(see board 137 , « cell marking cage 4 and 5 »)

(see board 138 , « cell marking cage 6 and 7 »)

04_02 cards hardware:

(see board 011, « VME geiger card »)

a) 10 couples of asics,one analogical,one digital

b) Here are the addresses of the digital asic counters and registers

(see board 085, « addresses »)

Here are the boolean equations of the PAL(programmable array logic)

(see board 127, « pld logic»)

c) There is a quartz oscillator 50Mc/s (CP) on each geiger card, to define the counting resolution of 20ns during the acquisition mode

- jitter:+-50ppm [0,70°] +-1picosec,+-2500c/s,[20,001ns,19,999ns]
- annual drift: 2ppm cumulable

d) protocole VME to numerical asics

- t = 20ns max
- T = about 500ns

(see board 033, « VME to digital asic protocol »)

e)

- the *hits* asics outputs are totempole TTL (**true** '1'), its image is memorized in the « status asic register ».
- to protect the asic, the *hits* are buferized before to build the « *electronic wired or* », with open collector buffers without load, the loads are located on the interface card.
- the « *electronic wired or* » is internal to the ***P'*** mother card wiring

f) The cells analogical signals arrive from :
- ¤ the insulator distribution,thanks to coaxial cables, via 3 double connectors 3M 3x2x20 = 120 signals (total 240 inputs because each one has a ground)
  - 40 anodic coaxial signals
  - 40 high cathodic coaxial signals
  - 40 low cathodic coaxial signals

  Here are the signals distribution on a geiger card:
  (see board 040, « geiger card signals inputs »)

- ¤ the detector,thanks to a lot of coaxial cables too
  (see board 014, « 4 cabinets bays »)
  (see board 076, « frame detector and cables »)

g) coaxial cable insulator to geiger card characterisics:
Z = 50Ω
C = 100pf/m
L1 = 1m, L2 = 1.5m ,there are 2 lengths of cables
ϕ 2mm

h) The number of the VME geiger card signals inputs is different according to the VME slot number, but the number of coaxial cables is always 120 , goto see "the sector cells distribution"

i) On the geiger card there is a *preliminary status register*, it is a 10bits hexadecimal register, one bit per digital asic.
Each bit indicates if there is an asic with a struck cell
example : asic nb 9 8 7 6 5 4 3 2 1 0
1 1 1 1 1 1 1 1 1 1 => *3FF*
1 0 1 0 1 1 1 1 1 1 => *2BF*

3FF : none of the 10 asics is struck,it is not necessary to read a counter in this card

2BF : the asics 8 and 6 are struck,its necessary to read this card,and only the counters of the asic number 8 and 6 .

j) there are a lot of possibilities to reset (***raz***) the digital asics counters :
- hardware : général at the *cold start,* automatically
- software :
  * general *broadcast*,simultaneously all the counters 8 cages,160 cards,1600 asics(not used to the LSM).
  * one cage, 20 cards,200 asics
  * one card ,10 asics
  * one asic, 4 counters
  * one counter

(see board 012, « geiger card raz »)

k) - the mecanical metal front face of the VME geiger card is

not standardized
- on each VME geiger card there are 2 leds :
  - *mesure "on"*,green led (inhibited with the black strap)
  - *select card* ,red led (inhibited with the red strap)
  - all green led are inhibited (black strap off) on a geiger cage,but the first left geiger card of each cage,only the first card on the left indicates the *mesure mode on*

*05 GEIGER CAGES **

05_01 cages generalities :

- There are 8 VME geiger cages
- There are 4 VME geiger cages of *type I*(44 *HITS*),and 4 VME geiger cages of *type II*(46 *HITS*),because of :
  (see board 083, « P' cab »)
  (see board 038, « nemo cab »)
- It is the internal wiring of the ***P'*** mother card, which defines the type I or II.
- The **J1** VME mother card is standardized
- The **J2** VME mother card is not standardized,it is named ***P'***.
- ***P'*** has 21 VME connectors, 20 of these connectors are used:
  - *to define*
    - the « *electronic wiring or* » of the *hits*
    - the geographical addresses of the cards
  - *to receive some signals*
    - the *start* and the *stop mesure*,the *stop Anode*,and the *stop time out (*still named *trigger)*, these 4 signals come from the trigger via a differential ligne drivers interface card between the trigger and the geiger acquisition.
  - *to receive the 2 none VME standardized alimentation:*
    - 7v 4A
    - 5V 3A

05_02 cages structure :

(see board 031, « geiger VERO cage structure »)
(see board 042, « geiger VERO cage structure 2 »)
(see board 043, « geiger VERO cage structure 1 »)

- mother board ***J1***, 21 slots(20 geiger cards,1 VIC8250)
- mother board ***P'***, 21 slots(20 geiger cards,1 VIC8250)
  (see board 164, « pinout mother board of geiger cage »)

  - the pinout of P' connector is the same for *type 1* or *type 2* geiger cage,only the internal wiring is different.
  - the VIC 8250 are linked between them, with double flat ribbon cables like this :
    (see board 067, « VIC8250 link »)

the instructions of VIC8250 switchs should be respected
(see board 066*, « VIC8250 switchs config »)*
➔the CSR number and the Crate number have to be identical

- one alimentation 5V 100A, cutting, for digital electronic
  - ¤ about 2A by geiger card (about 45A per cage)
  - ¤ manufactured by UniPower USA ,model PG2000
  - ¤ with current and voltage monitoring provided
    current monitoring: 5v for 100A
  - ¤ cooling integrated

- one alimentation 7V 4A,linear,for analogical asics
  - ¤ about 85mA per geiger card (about 1.7A per cage)
  - ¤ manufactured by Convergie model CEL DS 12.
  - ¤ without current nor voltage monitoring
  - ¤ without cooling
  - ¤ *current monitoring:* 1v for 1A , via monitoring card (see monitoring card)
  - ¤ this 7v 4A alimentation is a 12v 6.8A
    - * voltage reference modified by Convergie
    - * secondary winding of AC transformer modified by the LAL, to avoid the regulator overheating

- one alimentation 5V 3A,linear, for analogical asics
  - ¤ about 35mA per card(about 700mA per cage)
  - ¤ manufactured by Convergie model CEL BS 5 0VP
  - ¤ without current and voltage monitoring
  - ¤ without cooling
  - ¤ *current monitoring:* 1v for 1A , via monitoring card (see monitoring card)

- a interface line divers card(see interface card)

- a monitoring card (see monitoring card)

- 2 temperature probes T1 and T2 (see temperature)

- 1 thermo 54°c switch

- digital and analogical signals(temperature,voltage and current alimentations monitoring) leave the connectors on the back of the cage, to arrive to the slow control electronic

- 3 leds are located on the back of the cage for the 3 alimentations 5V 100A,7V 4A,5v 3A.

- a power 220V AC on/off switch is located on the back of the cage :

* it has always to be in the « on » position, because the AC power is controlled by the *slow control* electronic
* this on/off AC power switch contains :
  - ¤ the on/off power switch
  - ¤ a AC fuse
  - ¤ a AC filter
  - ¤ the AC plug in input connector

- manufactured by VERO,according to LAL's directives
  note : the 3 fans cage are outside the geiger cage
  (see fans crates)
  Here are some of these directives:

  ¤ the general ground distribution
  (see board 045, « geiger VERO cage,general ground distribution »)
  ¤ the 5v 100A distribution
  (see board 044, « geiger VERO cage,5v 100A distribution »)
  ¤ the position of the alimentations
  (see board 043, « geiger VERO cage,cage configuration»)
  ¤ the linking monotoring card
  (see board 046, « geiger VERO cage,link with monitoring card »)
  ¤ link between interface card and mother geiger cage card
  (see board 082, « geiger VERO cage,wiring link with interface »)

05_03 monitoring card :

- the connections of the monitoring card
  (see board 046, « geiger VERO cage,monitoring card connections »)
- the outputs of the monitoring card
  (see board 047, « geiger VERO cage,monitoring card outputs »)

- the goal of the designed LAL monitor card, is to create for the 2 linears alimentations 7v 4A and 5v 3A :
  - ¤ a current monitoring voltage, because these 2 alimentations are not equipped with it by the manufacturer.
    note : the 5V 100A is equipped with it by the manufacturer
  - ¤ a digital signal to indicate, if the power is correct,because these 2 alimentations are not equipped with it
    note : the 5V 100A is equipped with it by the manufacturer
- the monitoring electonic schemes are in the «*red book*»
- the monitoring card is located on the back of the cage , which opens with hinges
- here are the current to voltage conversion of the monitoring current of these 3 alimentatons(of

course *Labview* compute directly this conversion).
5V 100A 5v per 100A
7v 4A 1v per 1A
5v 3A 1v per 1A

05_04 interface,geiger to trigger card :

- There is an interface card (trigger to geiger acquisition) in each geiger cage
- This interface card is located on the back of the geiger cage, and it is extractable
- this card is linked with the trigger thanks to a double flat ribbon cable
- the goal of the interface card is :
  * to transmit to the trigger via a RS 485 line drivers protocol(drivers SN75LBC173 and 172) the *HITS* outputs.
  * to receive from the trigger, the 4 inputs signals via the same RS485 protocol :
    start mesure
    stop anode
    stop time out
    stop mesure
  * there is a wiring between this interface card and the P' mother card,via an *interadapt* little card
    (see board 082, « link between interface card and P' »)

- the time transit for the *HITS* (or the command signals,*stop time out*, *stop anodic,start* and *stop mesure*), because of the differential lines, is about 50ns.

*06 MISCELLANEOUS **

06_01 : tests calibration signals A and K *

- from the numerical asics ,these signals are common to the 4 cells of an asic,there is one signal for the anode, and one another signal common to the two cathodes .
- the timing of these tests are software programmable from the numerical asic,with a 80ns resolution
- *amplitude:* TTL signal ,without DC component, using a serial capacitor and resistor,to reduce the TTL signal to about 20mv.
  (see board 023*, « calibration threshold »)*
- *width:* 160ns , jitter: 20ns

06_02 : registers length *

All registers are on the 12 datas bits,but :

- the threshold and the injection registers : 8 bits
- the alpha counters : 17 bits
- the preliminary status register : 10 bits

06_03 : slow counting(alpha) *

- There are 4 counters in the digital asic: two cptA (anodic counter),and two cptK (cathodic counter).
- We don't need 2 cptA, the second cptA(low) is used as cptα
  * after the geiger acquisition received its *stopA* signal from the trigger, the geiger acquisition remains still opened during about 1ms(time fixed with an electronic programable monostable in the trigger, jitter monostable cptα : 2 to 3 µs) till the *stop mesure* signal.
    - if there is an event :
      * the α counter starts,then stops thanks to the *stop mesure signal*
      * the anodic counter counts at the same time as the α counter(modulo 12bits, 4096),only if anodic counter did not already starts in β mode

* the cathodic counters count at the same time as the α counter, stop with the cathodic signals,only if these counter did not already start in β mode

- a standard reading consists of to read 12 bits, but for the 17 bits of the counter α, there are two consecutive readings :
  first reading :12 bits
  second reading : 5 bits

06_04 : stop start mesure *

- there are two possibilities :
  * by software (VME command), for the conveniences of maintenance and tests.
  * by hardware from the trigger,under normal acquisition
    - asic input, *start mesure* true '1'
      (see board 017, « timing »)
    - a *start mesure* has to always be preceded by a raz counters

06_05 : VME functions not used *

- The ACFail control protocol of the VME alimentations
- The VME block transfert of datas
- There is neither manual nor SysReset VME raz
-

06_06 : rate of the events *

There is an event about each second(about 10 cells are struck)

06_07 : HV *

- There are as many HV as of layers (18)
- The insulator distribution can be powered with the HV,even the VME geiger acquisition is not fed by the AC 220v power

06_08 : trigger to geiger signals *

- After the trigger has received the order to send at the same time, to the 8 geiger cages the order « *start mesure* », it sends if there is an event, according to a timing, at the same time too, to the 8 geiger cages, the 3 signals :
  - *stop timeout*
  - *stop A*
  - *stop mesure*
- These 4 signals,*start mesure,stop A,stop timeout,stop mesure* are transmitted to the geiger acquisition via RS485 differential line drivers, thanks to the *interface card.*
- these 4 signals commands are ***pulses*** signals , it is necessary to memorize on the geiger card, these signals (but *stop A*), because the asic only recognizes ***level*** signals .

06_09 : HITS *

The geiger acquisition receives (if there is the HV) permanently the *hits,* and thus generates permanently *HITS*, even if the geiger acquisition is idle(no *start mesure* signal).

06_10 : counters reset *

The raz (remise à zéro) of numerical asics, of course, do not raz the thresholds registers

06_11 : digital asics outputs *

The numerical asics cannot generate a necessary VME TTL tristate, this tristate is created artificially , on the VME geiger cards.

06_12 : alpha and beta signals *

The β and α signals from the detector, have the same form and same amplitude

06_13 : 5v 100A current monitoring offset *

The current monitoring of the 5V 100A cutting alimentation, (provided by the alimentation), generates an offset voltage of about 600mv(12A).
This offset is corrected with the *Labview* software

06_14 : no standardized VME card *

➔ ***"CAUTION"***

Because of ***P'*** , the geiger card connector is not VME standardized,this implies never not to put the VME geiger card in an other VME cage, but the VME geiger cage, if not the VME geiger card and VME cage can be deteriorated.

06_15 : VIC 8250 CES VMV card *

➔ ***"CAUTION"***

The CES VMV controller VIC 8250 card have to be installed in the Slot 21(at the extreme right hand side),if not this card and the VME geiger cage can be deteriorated.

06_16 : extension card to test a geiger card *

➔ ***"CAUTION"***

- There are 2 extension cards to test the geiger cards, these extension cards are specific for geiger cards and geiger cages. Do not use an extension card in the geiger cage other than the specific extension card,if not the VME geiger card and VME cage can be deteriorated.
- Use imperatively these specific extension card to also test the gene40 and the trig80 cards.

06_17 : gene40 card, timing *

- The timings of the two gene40 cards(there is a spare card) to test the VME geiger cards,are slightly different(2 or 3 ticks),

because of the output filters components and their shield, use rather the number: 1 gene40 for the dynamic tests, if not timing errors will appear during the files comparison .
(goto see dynamic tests)
(see board 129, « OS9 nemo3 »)
(see board 162, « OS9 secondary menu 3 »)
[**F)** and **;)** secondary submenu]

- The gene40 is a heavy and large card, it has to be fixed in its slot with screws, if not, there will be bad electrical contacts

*06_18 : trig80 card **

- The are are 3 trig80 cards :
  - an old card
  - 2 new cards(number 1 and 2)
- ➔ The old trig80 card can be used with an specific geiger extension card (or not),but always with pair of flat «twisted» ribbon cables
- ➔ The 2 new trig80 card can be used exclusively with an specific geiger extension card(because of contacts problems),and always with a pair of flat « not twisted » ribbon cables

*06_19 : slots of the LAL geiger cage tests **

- There are some slots which have bad contacts, because these slots were used many times , also it is necessary to use preferably : * gene40 nb :1 card in slot 8
  * old trig80 card in slot 12
- ➔ imperatively : * geiger card in slot 2
- The geiger cage of the LAL bench is of *type 1*

*06_20 : splash **

- Some cell wires are connected to the geiger acquisition,and don't arrive to the detector.
- These no connected cells,if the threshold is low,can generate a spurious signal (named *splash*)
- There are 3 possibilities to avoid this :
  - ¤ install on the insulator distribution a capacitor on the empty cells,this solution does not remove completely the *splash*,thus this solution was not selected.
  - ¤ the best it's to adjust correctly the threshold
  - ¤ or never not to read these no connected cells, and to accept the trace if it is coherent, it was the method adopted by the physicists during the LAL tests !

*06_21 : datas reading, bit 15 **

- Each digital asic provides an output digital signal named « *acknoledge* » ,to indicate a correct reading datas.
- The 10 acknoledges of the 10 asics are « *or wired* » on a

single digital signal, and located on the 15th and most significant bit of the data bus of the geiger card.
- This 15th bit always has to be read before to accept the datas.
- The acknoledge at the output of the asic is a totempole TTL,true '0'.

*06_22 : bay power **

power max :1000w per bay

*06_23 : all is not in this geiger manual **

you will not find in this geiger manual :
- the LSM acquisition software
- the trigger
- the *Labview* slow control software
- the internal theorical schemes of the analogical asics
- the internal theorical schemes of the digital asics
- the description of the debuging LAL bench of the analogical asics

if you want information about these subjects :
(see board 124*, « references,sources,and designers »)*

*06_24 : 3M connectors mechanical intervention **

- there are 3 connectors 3M (2 x 2 x 20), on the geiger card
- the marked connector of a cross has to be located between the 2 others,this central connector is shorter than the 2 others, its ends were mechanically worked.

*06_25 : ACTQ244 mechanical intervention **

- the 2 ACTQ244 M44 and M35,on the geiger card are shorter than the others, their ends were mechanically worked, with a grinding stone,and an auxilary card.
- these shorter ACTQ244 are marqued in a separated package
- there is this problem because of the delivery of a batch of ACTQ244 longer than envisaged

*06_26 : 75LBC173 RS485 line drivers **

- The 75LBC173 convert an input RS485 protocol differential signal to an output logical TTL signal
- if the line input of the 75LBC173 is opened, the input of the driver is not fixed , therefore the TTL output of the

driver too

- these 75LBC173 TTL outputs are the command signals:
  - *start mesure*
  - *stop mesure*
  - *stop A*
  - *stop timeout*

  If the line of the driver is opened, or for example,if the trigger is "power off", these signals are hazardous.

➔ - This problem is only annoying in the testing mode of the geiger card(*internal* or *external* mode),because these tests cannot start if there is a permanent *start mesure* signal to '1' TTL.

- to avoid this inconvenience, it is necessary to sort the 75LBC173, and choise one with at the cold power starting, a start *mesure signal* always inhibited '1' TTL(pin 11),use the mini card tests 75LBC173 (see mini card 75LBC173)

- in the spare material there are a special package with 75LBC173 sorted ("*ok*" marked)

*06_27 : By pass a slow control crate **

- sometimes it is necessary to disconnect a slow control crate from the *Labview* control, to drive a geiger cage only with the local manual buttons.
- to do that :
  - disconnect the 9b female connector from IN RS485 *Labview* control,of the slow control crate
  - disconnect the 9b male connector from OUT RS485 *Labview* control,of the slow control crate
  - connect the 2 cables one in the other,and thus the slow control crate will be by passed

(see board 057*, « Adam moduls slow control »)*
(see board 060*, « Interlocks crate »)*

*07 GEIGER SLOW CONTROL **

*07_01 : slow control generalities **

(see board 013*, « cages implantation »)*
(see board 014*, « cabinets bay »)*
(see board 042*, « cages config 2 »)*

07_01_01 : The control can be divided in 3 parts :

- *Labview* **slow control**
  - the control supervises all the voltages , currents, temperatures etc..via the *Labview* software
  - *Labview* warns the operator, with an alarm display if there is an excess
  - *Labview* stops the 220v AC power of the geiger cage if the consigns are exceeded
  - *Labview* sends digital commands to start or stop the 220v AC power of a geiger cage,if an operator wants it

- **local,manual slow control**
  - it is possible to start or stop the 220v AC power of a geiger cage via *a local manual push button,* if an operator wants it
  - it is possible to survey the currents, voltages, temperatures with a multimeter,via a rotactor located on a the front face of the slow control crate

- **interlocks**
  - the control generates fast *interlocks* to stop the 220v AC geiger cage power , when there are important defaults (not detected if *Labview* fails) like excess of temperature,fans problems etc.. and it informs much later the software which displays a message to the operator.
    note : example about the temperature :
    the *Labview* software has to act first at 45°c (that depends of the check list consigns), to stop the AC 220v power of the geiger cage, *(see* board 084*, « Labview consigns »)*
    if *Labview* cannot act (for example :power off, or some other defaults..) then the interlocks acts at 54°c , thanks to a thermoswitch.
    (see ,how to *by pass* a slow control crate)

07_01_02 : Hardware crates are of 3 types :
(see board 013*, « cages implantation »)*
(see board 014*, « 4 cabinets bay »)*

- **slow control type 1 crate :**
  - with an analogic and digital *mesurement station* common to the high and low geiger cages located in one cabinet bay
  - there are 4 slow control type1 crates, one per bay

- **slow control type 2 crate:**
  - without an analogic and digital mesurement station
  - there are 4 slow control type2 crates,one per bay

- **fans crates:**
  - ¤ cooling crate for only the 21 cards of the geiger cages
  - ¤ there are 8 fans crates, two per geiger cages

*07_02 : slow control hardware **

07_02_01 : RS485 network bus

-a: There are 8 slow control crates, 4 of type1,4 of type2.

-b: Only the 4 type1 crates (with 2 others process : *gaz* and *electric boxes*) are linked on a RS485 differential line.

-c: Via this RS485 line, each slow control crate only of type1,thanks to an address, can receive or send datas from *Labview* software,located in a master PC .
(see board 055*, « RS485 network »)*

-d: The port COM2 of the PC sends RS232 *Labview* dialog to the RS232 to RS485 converter (ADAM module 4520)

-e: There is a loading resistor of 120Ω at the beginning, and at the end of the RS485 line.

-f: The inputs and outputs of the RS485 cables line, are located on the front face of the slow control crate of only type1, because the analogical and numerical *mesurement station* ,in the type1 crate, is common to the two slow control crates type1 and type2

-g: Because of this *mesurement station* common for two crates, there are only 4 slow control crates of type1 linked on the RS485 line

-h: Here is the wiring cables of the 4 slow control gages :
(see board 056*, « RS485 cables »)*
(see board 057*, « ADAM modules »)*

07_02_02 : slow control crates

- Two types of slow control crates(see *chapter 07_02_01*)
- These 2 types 1 and 2 are almost similar :
  - ¤ ***slow control common items in type1 and 2 crates:***
    - * for the digital electronic,a block modular alimentation 5v 1A
    - * a card, common for the slow control and the interlocks, the theorical electronic schemes are in the *red book*, here is the synoptical of the interlocks
      (see board 063*, « interlocks synoptical »)*

* a front and back crate faces equiped with:
(see board 060, « slow control crate »)
1) a lot of leds
2) a 6 position manual analogical rotactor,to control locally with a multimeter,the following voltages:
   ¤1: 5V 100A monitoring current,cutting alimentation, 5v per 100A

   ¤2: 5V 3A monitoring current,linear alimentation, 1v per 1A

   ¤3: 7V 4A monitoring current,linear alimentation, 1v per 1A

   ¤4: temperature T1

   ¤5: temperature T2
   (see board 042, « geiger VERO cage structure 2 »)

   Here is mV to T conversion for the temperature AD22100K probes Analog Devices :
   T °c = (Vmv - 1375) / 22.5

   Note :
   A lot of temperature measurements in the geiger cages indicated that it was necessary to install an additional fan above the low geiger cages,only in bays 10 and 40
   (see board 013, « cages implantation »)
   (see board 080, « geiger cages,temperature measurements »)

   ¤6: none

3) a double push button start/stop 220v AC geiger cage

4) a general switch contact 220v AC slow control crate breaker

* *slow control card,modification note:*
The current monitoring output (provided by the alimentation manufacturer) of the 5V 100A of the cutting alimentation, is a mode common output,and the analogical inputs of the Adam 5051 are differential, from which the requirement modification
(see board 062, « monitoring modifications »)

¤ ***slow control additional items in type1 crate only:***
The digital and analogical ADAM 5000 *mesurement station* receives (and sends) signals from (to) the slow control crates of type 1 and 2.

* for the ADAM modules, a block modular alimentation

12v 1A
* An ADAM 5000 support,with the ADAM modules :
(see board 058, « ADAM 5000 support »)

a) 2 x 5017,8 analogical 0 to 5v differential inputs
(see board 059, « ADAM 5017 analogical inputs dispatching »)
all analogical inputs are shunted with a 0.1µf

b) 1 x 5051,16 digital TTL inputs
c) 1 x 5056,16 digital TTL outputs
(see board 079, « ADAM digital I/O dispatching »)

07_02_03 : fans crates

- each geiger cage has its separated fans crate(3 fans) to cool only the 21 VME geiger cards
- manufactured by VERO
- silencious,with internal monitoring and interlocks
  - ¤ a thermo probe makes it possible to control the speed of the fans according to the temperature, however the probe is inhibited and the fans always turn at maximum speed.
  - ¤ the internal interlocks was LAL modified to make these internal interlocks external too, and thus to be able to inform the slow control
    Here is this LAL modification
    (see board 064, « fans interlocks LAL modifications »)

    These fans *interlocks* stop the 220v AC power of the geiger cage if there is a default ,even if only one fan fails(there are 3 fans),and a buzzer alarm warns the local operator.

07_02_04 : link, geiger cages to slow control crates

(see board 061, « interlocks interconnexions »)

- The slow control type1(*with measuring station ADAM*) crate
  - ¤ sends digital commands signals (start, stop 220v AC)
    * directly to geiger cage of type1 HIGH(*46 HITS*)
    * undirectly via the slow control cage type1, to geiger cage of type2 LOW(*44 HITS*)

  - ¤ receives analogical(voltage from monitoring current of the alimentations,temperatures) and digital signals TTL (on/off of alimentation,fans ..)
    * directly from geiger cage of type 1 HIGH(*46 HITS*)
    * undirectly via the slow control cage type1, from geiger cage of type 2 LOW(*44 HITS*)

*07_03 : slow control software **

- The *Labview* software is used and located in a LSM PC.
  - ¤ the geiger cages are on a RS485 bus with 2 others (gaz,electric boxes)

  - others process, *Labview* controled too,are on the CAEN bus, or RS232 bus

- With *VNCviewer* it is possible to drive *Labview* from the LAL ,if the authorization is given from the LSM.

- It is possible to only watch from the LAL,the *Labview* windows thanks to an address web

- The *Labview* software is slow, it does not control only the 8 geiger cages,there are others process to control.
  (see board 055, « RS485 network bus »)

- The *Labview* software loops permanently on all the processes, compares its measurements to a check list of standard values(consigns), if there is a default, and if this default is identical after 10 loops,*Labview* stops the 220v AC power of the geiger cage
  (see board 084, « Labview consigns »)

- All *Labview* geiger functions from the PC keyboard are also possible locally thanks to push buttons, switchs,leds... located on the front face of the slow control crate.
  Here are these functions :
  - 220v AC power start/stop
  - T1 and T2 temperature display
  - 5v 100A,5V 3A,7V 4A, current monitoring display

- *Labview* can display one view per geiger cage
  - All leds have to be green, if not,there is a default
  - The « *save* » box makes that it is possible to record the temperature and the monitoring current of the alimentations

  (see board 048, « Labview geiger bay number 20 »)
  (see board 049, « Labview geiger bay number 30 »)
  (see board 052, « Labview geiger bay number 10 »)
  (see board 053, « Labview geiger bay number 10,with defaults»)

- *Labview* can display a general view of all processes,geiger cages,PM cages,HV etc..
  (see board 050, « Labview general view of the processes,with defaults »).

  (see board 051, « Labview general view of the processes,without defaults »).

*08 GEIGER LAL BENCH MAINTENANCE **

08_01 **general notes:**

The LAL datas acquisition tests and maintenance is assured :

** by software thanks to :*

OS9 and a C MicroWare compilator

(see board 100, « OS9 read me »)

** by hardware thanks to :*

(see board 035, « picture 3 »)

(see board 036, « picture 4 »)

1 branch with :

- 1 (1 to 8)VME geiger cage (type 1),21 slots
- 1 VMV VIC8250 CES controller in slot 21
- 1 VME geiger card in slot 2 ←
- 1 trigger80 card in slot 12
- 1 gene40 card in slot 8
- 1 insulator distribution mother card,with 15 daughter cards

The A, Kh and Kb signals can come from 3 possibilities:

(see board 019, « LAL bench »)

- ***from*** a 9 or 20 cells experimental LAL physicists manufactured chambers
  About one year long was necessary to the physicists to analyse the results of a lot of datas acquisition from 3 successive prototypes geiger cards, before definitively to manufacture the 175 geiger cards .

- ***from*** a generator 40 VME card
  This card can send simultaneously 40 A, 40 Kh and 40 Kb signals to a geiger card to test it.
  (see gene40 card)

- ***from*** geiger asics dynamic external tests signals
  This mode permits to test the geiger card in "stand alone" mode, without gene40 and Trig80 VME cards.
  (see external tests)

08_02 **bench LAL software:**

A large menu of possibilities commands exists:

➔ *(see board 129, « OS9 nemo3 »)*

here is the check list software OS9 C compilated routines

(see board 088, « Os9 mesa rout »)

here are the 10 files C source LAL software of the bench tests,with their *make file* and its *offset.h* definitions file

note:

these programs are also in the archiving " *red book* ".

(see board 087, « OS9 makefile »)

(see board 099, « OS9 offset.h »)

(see board 089, « OS9 nemo »)
(see board 090, « OS9 nemo a »)
(see board 091, « OS9 nemo b »)
(see board 092, « OS9 nemo c »)
(see board 093, « OS9 nemo d »)
(see board 094, « OS9 nemo e »)
(see board 095, « OS9 nemo f »)
(see board 096, « OS9 nemo g »)
(see board 097, « OS9 nemo h »)
(see board 098, « OS9 nemo i »)

There are 3 principal programs:

***08_02_01*: acquisition from 9 or 20 cells chamber**

Here are the acquisition listing acquisition datas with the 20 cells chamber, and its graphical representation by the physicists .

(see board 129, « OS9 nemo3 »)
(see board 158, « OS9 secondary menu 1 »)
[**e)** and **y)** secondary submenus]

(see board 041, « 20 cells LAL chamber »)
(see board 140, « 20 cells typical acquisition »)
(asic_run nb: 05)

(see board 148, « 20 cells statistic nb:1 results »)
(see board 149, « 20 cells statistic nb:2 results »)

(see board 166, « OS9 primary menu 3 »)
[**S)** primary menu]

Here are some others graphical results,from electronic specialists:
(see board 150, « 1 cell statistic nb:1 graph »)
(see board 151, « 1 cell statistic nb:2 graph »)
(see board 152, « 1 cell statistic nb:3 graph »)
(see board 153, « 1 cell statistic nb:4 graph »)
(see board 154, « 1 cell statistic nb:5 graph »)
(see board 155, « 1 cell statistic nb:6 graph »)

Here are some physicists graphical results:
(see board 141, « 9 cells K physicists graph »)
(see board 142, « 20 cells K physicists graph »)
(see board 143, « 20 cells beta A physicists graph nb:1»)
(see board 144, « 20 cells beta A physicists graph nb:2»)
(see board 145, « 20 cells physicists graph A »)
(see board 146, « 20 cells alpha physicists graph nb:2 »)
(see board 147, « 20 cells alpha physicists graph nb:2 »)

***08_02_02*: static tests of one geiger card**

The geiger card receives 21600 tests vectors :

- read write counters
- read write threshold registers
- internal signals injections
- external signals injections
- raz
- etc...

With each time,a reading followed by a comparison with a standard value.
The trigger80 card only generates a *stop A* signal

notes :

¤ The true hardware inputs are not tested because nothing is injected to them.

¤ The static tests are the tests which are also applied with the LSM geiger cards, but without *stop A* signal,to test them.

(see board 129, « OS9 nemo3 »)
(see board 161, « OS9 secondary menu 2 »)
[**f)** secondary sub menu]

08_02_03: dynamic tests of one geiger card

- In this case,the 40 geiger electronic acquisition inputs of one geiger card,can receive simultaneouly 120 signals :
  - ¤ 40 anodic signals
  - ¤ 40 high cathodic signals
  - ¤ 40 low cathodic signals

  These 120 signals are generated by a *gene40* VME LAL designed card.
  These simultaneous 120 signals form one dynamic run,and there are successively 90 dynamic runs.

- Obviously a dynamic test with the gene40 cannot be applied to LSM cards.

- The dynamic test can only be applied in LAL, to only one card, one by one .

- The 90 dynamic runs are stored in a memory,and then compared with standard values .

(see board 129, « OS9 nemo3 »)
(see board 162, « OS9 secondary menu 3 »)
[**F)** secondary submenu]

➔ Here are the standard values
(see board 132, « asic run standard 01 »)

08_03 bench LAL hardware:

The *08_01* chapter already discribed a little bit this bench hardware.

(see board 019, « LAL bench »)

***08_03_01* : CES manufactured cards**

(see board 074, « synoptical tests bench »)

In a standard VME master crate there are:
- FIC 8234 CPU card
- DIS 8002 display VME card
- VIC 8250 VME/VMV control card
- a hard disk and a floppy disk mechanisms

  note: this VIC8250 links with :
  - a VIC8250 of a geiger cage type 1, named "*LAL VME bench cage*" in which there are;
    * the geiger card which must be tested in slot 2 **imperatively,** because of the triger80 card decoding event .
    * a VME gene40 card in slot 8
    * a VME trig80 card in slot 12

  (see board 035, « picture 3,bench tests »)
  (see board 036, « picture 4,bench tests »)

***08_03_02* : TRIGGER80 LAL designed card**

- This VME card (no standardised because of the geiger cage) named *trig80*, 80 because of its local clock pulse(CP) is 80Mc/s (12.5ns), while the geiger cards CP is 50Mc/s(20ns).
- The trig80 card simulates the LSM true trigger .
- The electronic theorical schemes are in the archiving " *red book* ".
  (see board 021, « trig80 specifications »)
- the trig80 card have to generate the following 4 signals:
  - *start mesure*
  - *stop time out*
  - *stop A*
  - *stop mesure*

***08_03_03* : GENE40 LAL designed card**

- This VME card (no standardised because of the geiger cage) named *gene40*, 40 because of this card can generate simultaneously 40 signals to the 40x3 inputs of a geiger card, its CP is 80Mc/s like the trig80 card (12.5ns).
- The gene40 card simulates the detector signals.
- The electronic theorical schemes are in

the archiving " *red book* ".

- To summarize,the gene40 card is made of 3 programmable separated differents generators and these 3 generators can be dispatched on each input of the geiger card.

(see board 020*, « gene40 specifications »)*

Here is an example of *gene40* possibilities: 3 cells hit, with only 2 generators, Gene2 is not used

- ¤ one cell with Gene1 β
- ¤ one cell always with Gene1 β
- ¤ one cell with Gene3 α

(see board 030*, « gene40 example »)*

08_03_04 : Geiger cards maintenance and history

- After wiring a lot of geiger cards (about 80%) returned to Bellegarde(wiring society),because of defaults.

- Only the principal wiring defaults are nomenclatured in a *history file*.

(see board 126*,« maintenance geiger cards history »)*

➔ - An annoyng problem after wiring taked place in 1999,on 10 geiger cards appeared some internal cutting wire .

- The wiring employed is the multiwires technologie

- The RCI manufacturer of the geiger cards recognized the defaults on **05-99 delivery**, and exchanged them free, but the 05-99 delivery included 27 geiger cards.

- since the cut of wire continued on some cards (about 6),but seems stable from now !

(see board 086*, « RCI letter »)*

08_04 auxilaries hardwares:

a) LM336 sorting card
b) Cab connector to test analogical outputs of geiger cage
c) Cab connector to test digital outputs of geiger cage
d) Box to test the crate fans interlocks

e) Mini card to test 75LBC173 line differential drivers

➔ *f*) Card to test the interface geiger/trigger card

g) Box with double commands and interloks

➔ *h*) A P'mother board testing card

i) Two extension cards for specific geiger card

j) One extension card VME specific

k) Two extension cards for interface geiger/trigger card

l) One board card to make the 74ACTQ244 shorter

m) A "gene one", card

a- mini card to test the LM336 5v reference, the LM336 have to be sorted (absolute precision +- 0.5%), the LM336 is the 5v reference of the DAC (digital to analogical converter) for the threshold input geiger card.

b- cap connector to test with a multimeter the analogical outputs of the monitoring card of a geiger cage ,currents and voltages of :
- 5v 100A cutting alim
- 5v 3A linear alim
- 7v 4A linear alim

c- cap connector with leds to test the digital outputs of the monitoring card of a geiger cage, these leds have to be powered by the internal geiger cage *card monitoring*

d- test box of fans crate,this box have to be powered with an auxilary 5v alimentation

e- mini card to test the differential ligne drivers of the interface (trigger/geiger) 75LBC173
(see 75LBC173 RS485 line drivers)

f- card to test the interface card(trigger/geiger), this little card simulate the trigger, and generate and inject the 4 following signals in differential mode in the differential inputs of the interface card:
- *start mesure*
- *stop time out*
- *stop A*
- *stop mesure*

(see board 070*, « tests interface geiger/trigger card »)*

g- a double command box hardware slow control,go to see slow control, this box was the prototype of the slow control crates

h- a *card to test the P' mother board* of a geiger cage, this card is very important
(see board 072*, « tests P' mother card synoptical »)*

The electronic theorical schemes of this tests card are in the archiving " *red book* ".

This card have to be installed on a "extention specific geiger card",***especially not*** on a "extention VME card". Move this card from slot to slot to test the P' mother card of a geiger cage,and move the strap a long the 40 *hits* pins possibilities.

(see board 083*, « P' cab »)*

i- two "extension specific geiger card":
CAUTION:
don't use these cards to a VME standardized bus, and oppositely don't use a standardized VME extension card with a geiger cage,under penality of causing important failures.

j- one "extension specific VME standardized card":
CAUTION:
don't use this card to a geiger cage, and oppositely don't use an *extension specific* geiger card with a standardized VME bus cage, under penality of causing important failures.
Notes :
- The geiger cage is not a standardized VME cage
- The master CPU cage of the bench test LAL is a standardized cage VME

k- two extension cards for the interface trigger to geiger

l- one board card to make the ACTQ244 mechanically shorter, with a grinding stone.
(see mechanical intervention on some ACTQ244)

m- a card named « *gene one* » card, can inject in the geiger card (directly in the 3M front face inputs connectors),repeatedly, thanks to a clock pulse (or in single shot mode with an external trigging), the 3 analogical signals which simulate a cell (one anode, and 2 cathodes) .
(see board 026*, « gene one synoptical »)*

*09 LSM MAINTENANCE **

10_01 **software maintenance *:**

there are 22 programs to tests the asics

(see board 071, « lsm software list »)

(see board 101, « lsm raz 10 asics »)
(see board 102, « lsm raz 1 asics »)
(see board 103, « lsm raz cage »)
(see board 104, « lsm raz card »)
(see board 105, « lsm read 10 asics »)
(see board 106, « lsm read 1 asic »)
(see board 107, « lsm read threshold 10 asics »)
(see board 108, « lsm read threshold 1 asics »)
(see board 109, « lsm read status 10 asics »)
(see board 110, « lsm read status 1 asic »)
(see board 111, « lsm read preliminary status 1 card »)
(see board 112, « lsm read preliminary status 20 cards »)

(see board 114, « lsm test ext 10 asics »)
(see board 115, « lsm test ext 1 asic »)
(see board 116, « lsm test int 10 asics »)
(see board 117, « lsm test int 1 asic »)
(see board 118, « lsm write 555 10 asics »)
(see board 119, « lsm write 555 1 asic »)
(see board 120, « lsm write AAA 10 asics »)
(see board 121, « lsm write AAA 1 asic »)
(see board 122, « lsm write threshold 10 asics »)
(see board 123, « lsm write threshold 1 asic »)

There is a principal program named « *static run tests* »,to test the geiger cards of all the 8 cages.
➔ *(see board 113, « lsm static run tests »)*
with its
(see board 156, « geiger.h lsm »)

note:
this *static run tests* program is also in the archiving " *red book* ".

This program obviously cannot inject signals to the geiger connectors inputs,only the LAL bench tests, with its *gene40* card can do that.
The « *static run tests* » program don't use the trigger, consequently There is no :
- *stop A* signal, the A counters are stopped by the internal geiger *stop mesure* signal
- *stop time out*, in static mode this signal is not necessary, because the *time out* does not act in the static mode

(see board 167, « how to login to the LSM machines »)
(see board 139, « how to start static run tests program »)

The « *static run tests* » program generates an errors archive file named « *run static errors* », you have to read it to know the errors.
(see board 128, « lsm run static errors »)

notes : - the « *static run tests* » program is not, of course the acquisition LSM software.
- the LSM acquisition geiger software team received from LAL,the following consulting geiger hardware check
(see board 081, « ires informations »)

10_02 **hardware maintenance ***
How to change a card in a geiger cage
(see board 134, « hardware maintenance »)

10_03 **spare electronic components ***

(see board 133, « spare electronic components »)

*10 SOURCES and REFERENCES **

(see board 124, « sources, references and designers »)

*11 BOARDS LIST **

(see board 125, « list of boards, direct linking »)