Fit by FPGA

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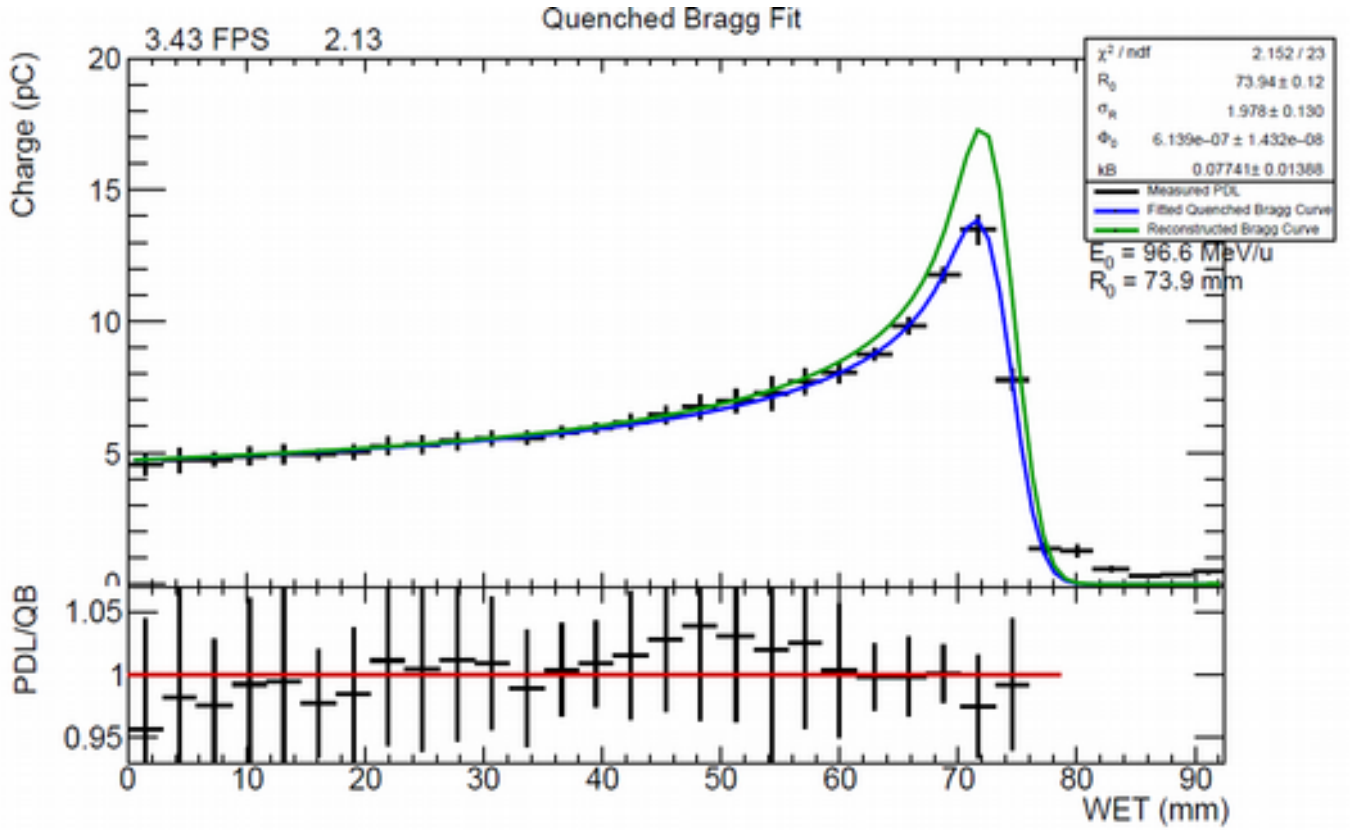
Bragg curve fitting

Original fit sample



Purpose

Improve fitting speed

Base status

Root TF1 Fit (4 para)
FUMILI minimizer

Processing time bottleneck

Two integral calculation for fit function
Average calculation in the bin for expected value for a bin

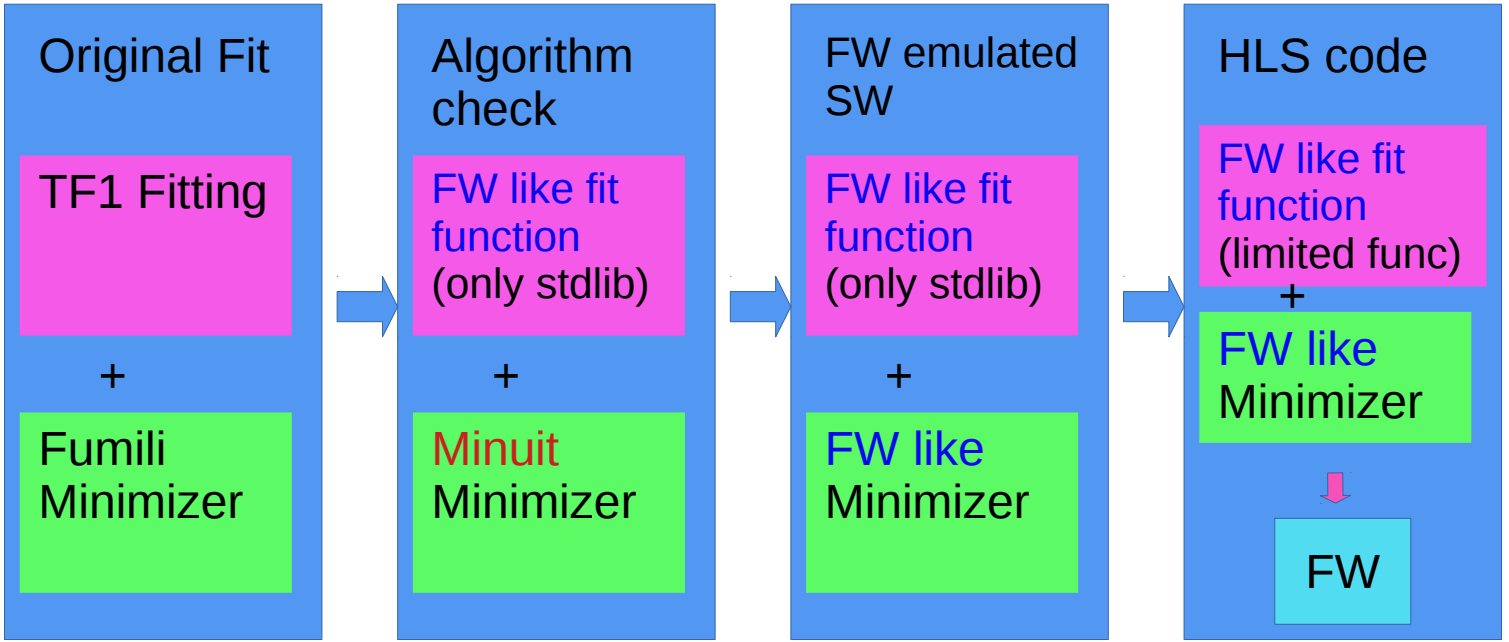
Goal

~20 times speed up

Current speed ~4 Hz (my loacl pc)

Goal is ~100 Hz

test process



- Check the fit results with pseudo data
- Compare processing speed in each step
- FPGA resource usage and speed with expected improvement

Algorithm check

FW like fit function (only stdlib)

+

Minuit Minimizer

Fit function replacement

All root lib function was replaced by std function from Fit function including two integration and one average calc for a bin. i.e. All parameter is flexible.

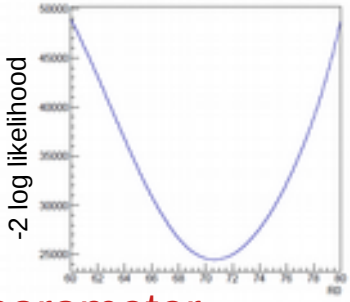
Ask: full absorption?

- Integration's resolution is region/16
- average of 4 region in a bin

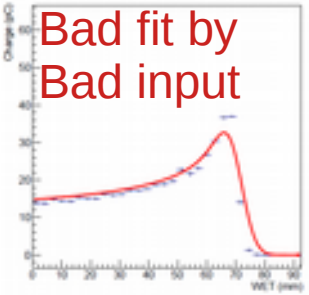
Strong dependence of initial fit parameters

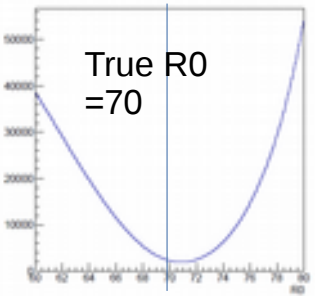
Carefully set initial value for the fit (not huge LL value, good parabola)

Initial likelihood distribution with bad parameter

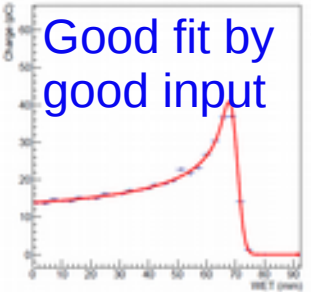


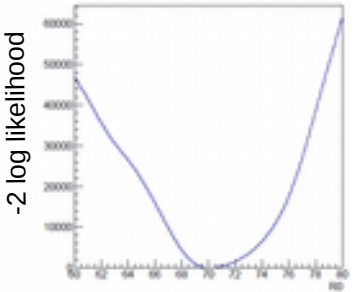
Bad fit by Bad input



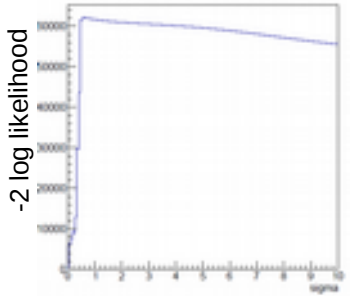


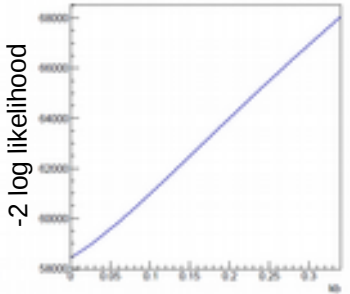
Good fit by good input

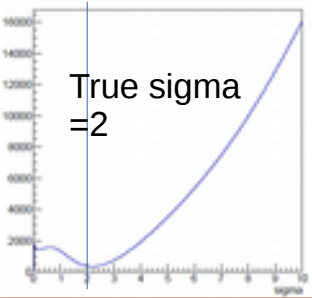


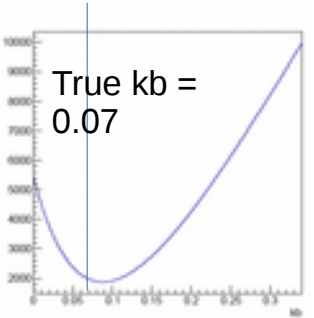


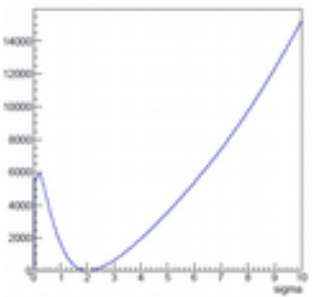
e.g. bad init parameter

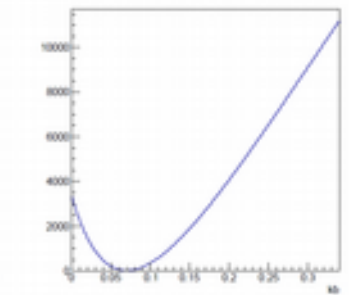






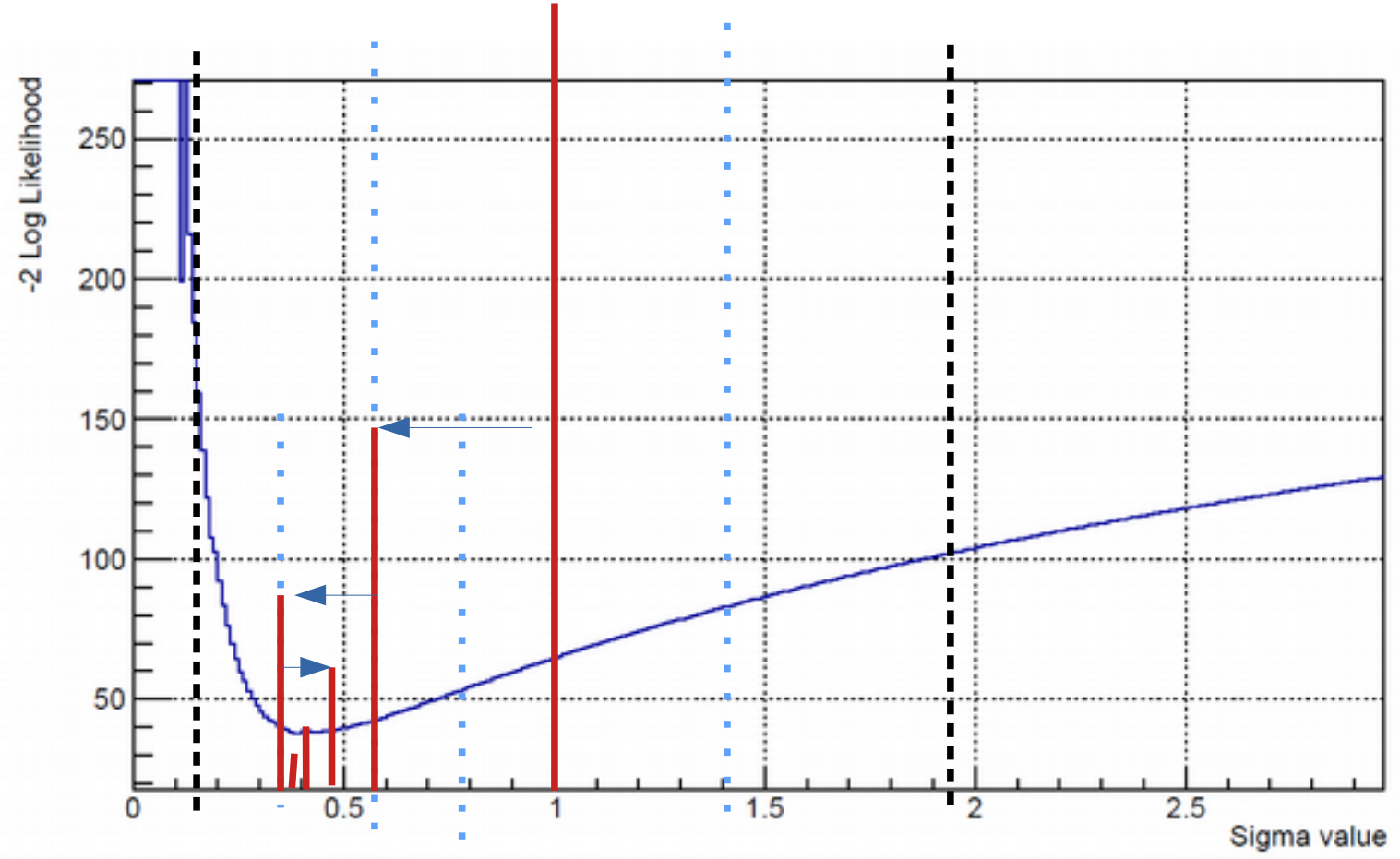






FW like
Minimizer

Minimizer algorithm



Fit regtion

Initial position

+/- 50% range scan

Find minimum position.

Repeat with double resolution and minimum position as initial.

Sequentially loop for each parameter

Simple and Robust

Example for minimization process

Minuit

Minuit
Find min by 227 scan
MinLL 109.2

```
                                CURRENT GUESS       STEP         FIRST
 NO.   NAME      VALUE            ERROR          SIZE      DERIVATIVE
  1  R0           8.16835e+01   1.00000e-02   0.00000e+00   6.24730e+05
  2  sigma        2.91094e+00   1.00000e-03   1.14555e+00  -3.23381e+02
  3  phi0         2.00000e-06   1.00000e-03   0.00000e+00   3.29254e+05
  4  birks        7.00000e-02   1.00000e-03   0.00000e+00  -2.27801e+04
MIGRAD MINIMIZATION HAS CONVERGED.
MIGRAD WILL VERIFY CONVERGENCE AND ERROR MATRIX.
COVARIANCE MATRIX CALCULATED SUCCESSFULLY
FCN=109.237 FROM MIGRAD    STATUS=CONVERGED     226 CALLS         227 TOTAL
                     EDM=7.67958e-05    STRATEGY= 1      ERROR MATRIX ACCURATE
 EXT PARAMETER                                           STEP         FIRST
 NO.   NAME      VALUE            ERROR          SIZE      DERIVATIVE
  1  R0           7.39791e+01   1.23702e-01   2.79376e-05   7.23652e-01
  2  sigma        2.12404e+00   1.41613e-01   6.72359e-04  -7.71264e-02
  3  phi0         6.08216e-07   1.43956e-08   1.98456e-05   1.80199e+00
  4  birks        7.12301e-02   1.36540e-02   9.40448e-04  -3.78831e-02
EXTERNAL ERROR MATRIX.    NDIM=  25    NPAR=  4    ERR DEF=1
 1.530e-02  7.073e-03  8.741e-10  8.624e-04
 7.073e-03  2.019e-02  4.464e-10  4.424e-04
 8.741e-10  4.464e-10  2.072e-16  1.881e-10
 8.624e-04  4.424e-04  1.881e-10  2.010e-04
```

FW alg

FW alg
Stop scan at **128**
MinLL 117.5

Start from huge LL value (problematic)

```
stage=  0, paran=1, tlv=   1, R0=  81.68, minR0=  81.68, sigma=     2, minsigma=     2, phi0=    20, minphi0=    20, birks=    0.07, minbirks=    0.07, logL=1.443e+05, MinLogL=   1e+07
stage=  0, paran=1, tlv=   2, R0=  81.68, minR0=  81.68, sigma=     2, minsigma=     2, phi0=    20, minphi0=    20, birks=   0.085, minbirks=    0.07, logL=1.329e+05, MinLogL=1.443e+05
stage=  0, paran=1, tlv=   3, R0=  81.68, minR0=  81.68, sigma=     2, minsigma=     2, phi0=    20, minphi0=    20, birks=   0.055, minbirks=   0.085, logL=1.575e+05, MinLogL=1.329e+05
stage=  0, paran=2, tlv=   4, R0=  91.68, minR0=  81.68, sigma=     2, minsigma=     2, phi0=    20, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=9.942e+05, MinLogL=1.329e+05
stage=  0, paran=2, tlv=   5, R0=  71.68, minR0=  81.68, sigma=     2, minsigma=     2, phi0=    20, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=6.656e+04, MinLogL=1.329e+05
stage=  0, paran=3, tlv=   6, R0=  71.68, minR0=  71.68, sigma=   2.5, minsigma=     2, phi0=    20, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=6.461e+04, MinLogL=6.656e+04
stage=  0, paran=3, tlv=   7, R0=  71.68, minR0=  71.68, sigma=   1.5, minsigma=   2.5, phi0=    20, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=6.837e+04, MinLogL=6.461e+04
stage=  0, paran=0, tlv=   8, R0=  71.68, minR0=  71.68, sigma=   2.5, minsigma=   2.5, phi0=    30, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=1.889e+05, MinLogL=6.461e+04
stage=  0, paran=0, tlv=   9, R0=  71.68, minR0=  71.68, sigma=   2.5, minsigma=   2.5, phi0=    10, minphi0=    20, birks=   0.085, minbirks=   0.085, logL=    5660, MinLogL=6.461e+04
stage=  1, paran=1, tlv=  10, R0=  71.68, minR0=  71.68, sigma=   2.5, minsigma=   2.5, phi0=    10, minphi0=    10, birks=  0.0925, minbirks=   0.085, logL=    5373, MinLogL=    5660
```

.....

```
stage= 14, paran=2, tlv= 117, R0=  73.91, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 14, paran=3, tlv= 118, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 14, paran=3, tlv= 119, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 14, paran=0, tlv= 120, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 14, paran=0, tlv= 121, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.226, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=1, tlv= 122, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=1, tlv= 123, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=2, tlv= 124, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=2, tlv= 125, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=3, tlv= 126, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=3, tlv= 127, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
stage= 15, paran=0, tlv= 128, R0=  73.92, minR0=  73.92, sigma=   2.5, minsigma=   2.5, phi0=  6.227, minphi0=  6.227, birks= 0.08781, minbirks= 0.08781, logL=   117.5, MinLogL=   117.5
```

Full test with pseudo data

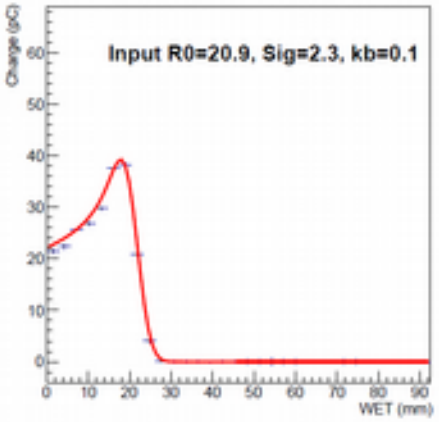
Pseudo data truth parameters and Fit parameters

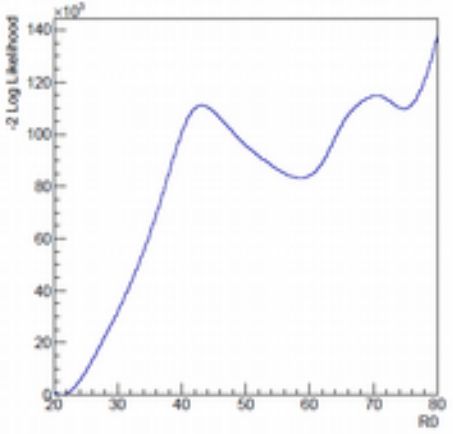
Pseudo data range
R0 20-80
Sigma 1-3
Phi0 6e-7
Kb 0.04-0.10

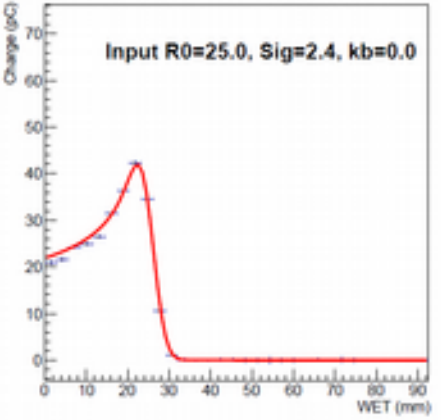
Fit parameter
Integration division = 16
N division for a bin average = 4
Minimization loop = 128

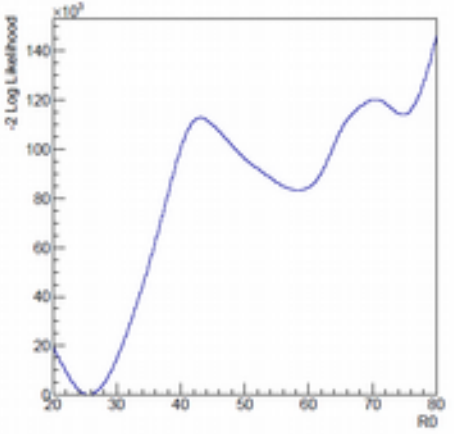
Initial value and fit region
R0 = maximum bin's x + 10 +/- 20
Sigma = 2 +/- 1
Phi0 = 20e-7 +/- 20e-7
Kb = 0.07 +/- 0.03

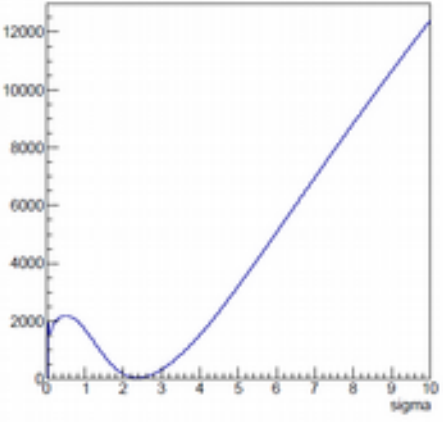
Example pseudo data fit

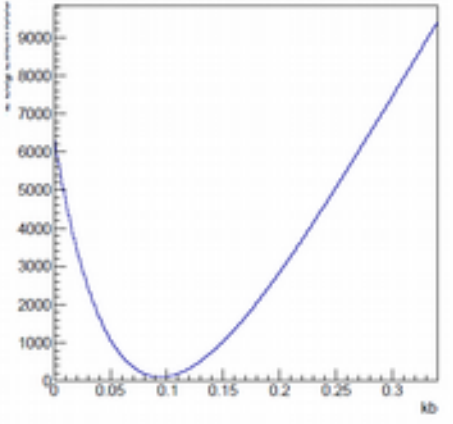


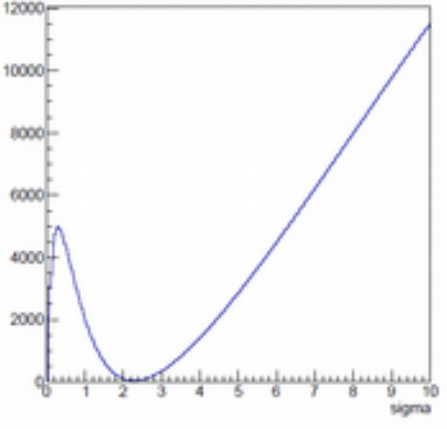


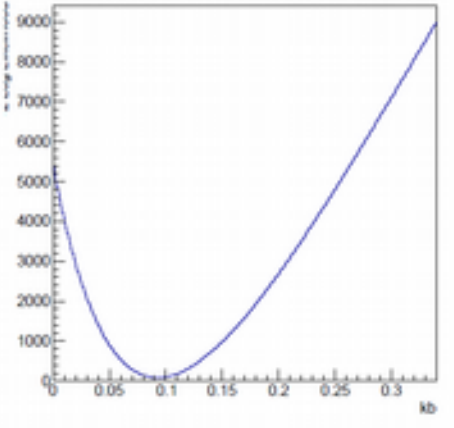




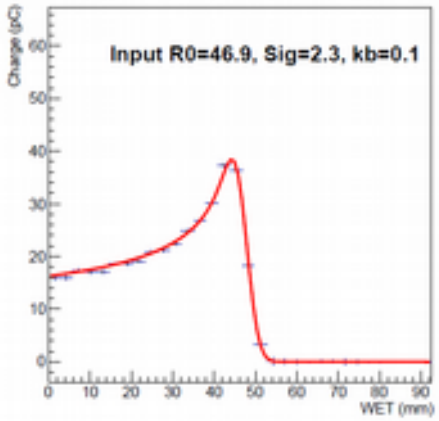


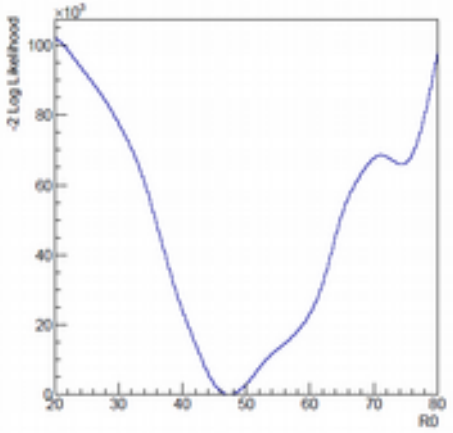


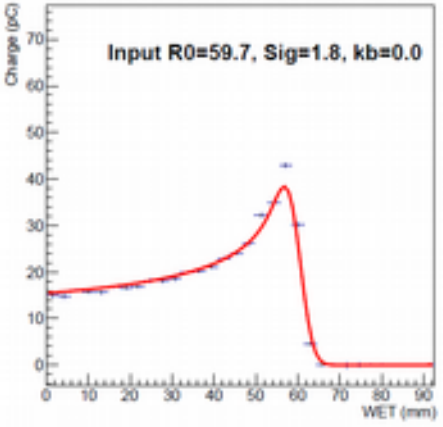


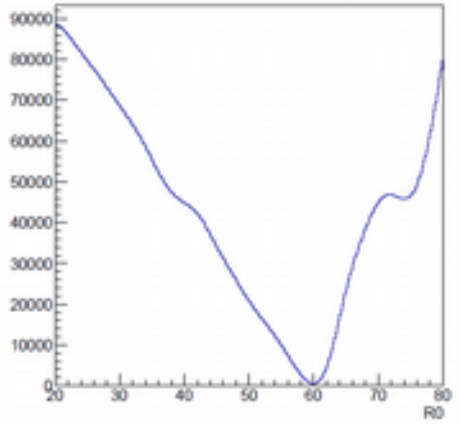


Example pseudo data fit

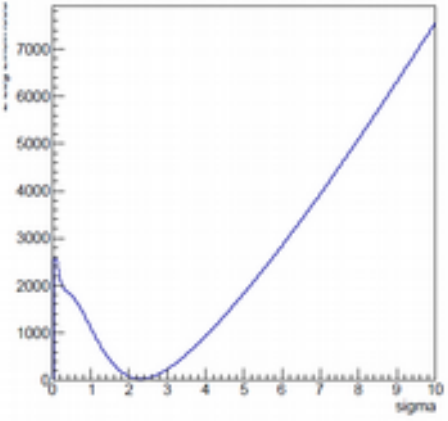


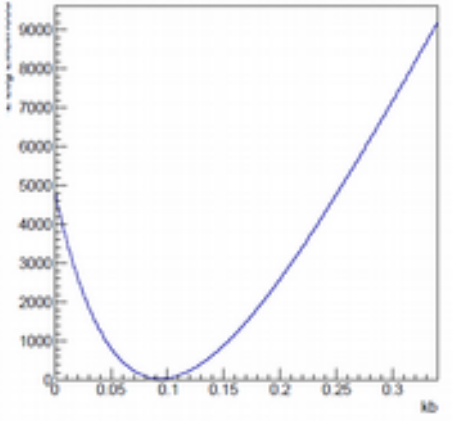


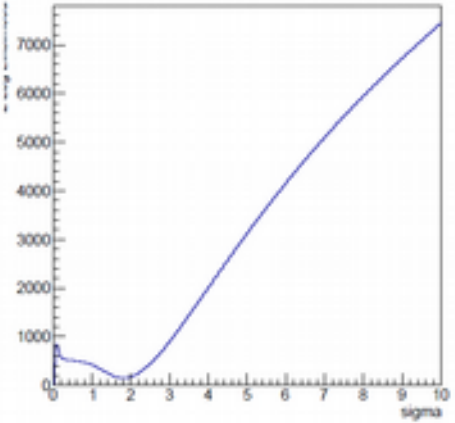


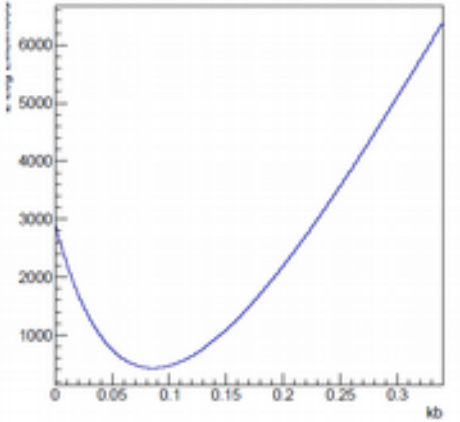


Miss Fit

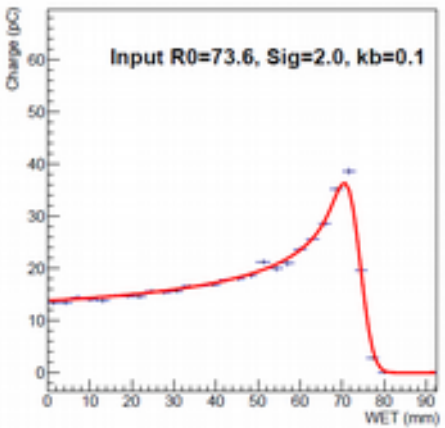


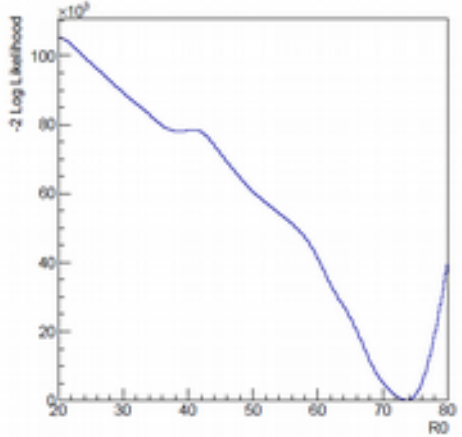


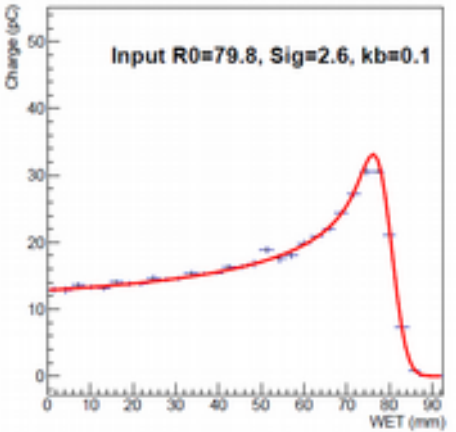


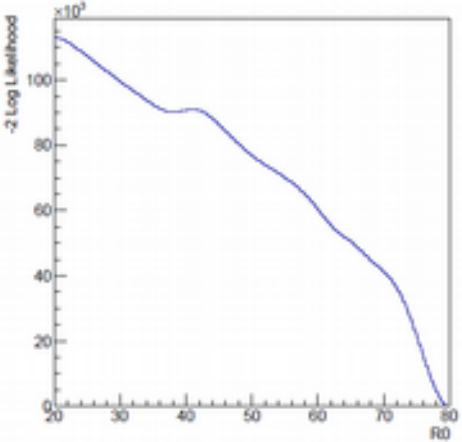


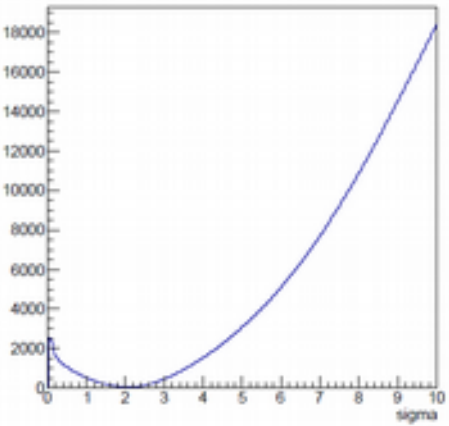
Example pseudo data fit

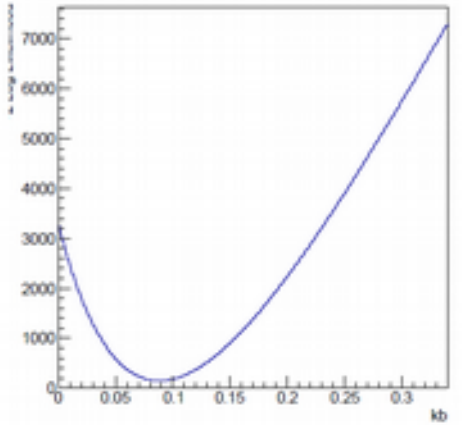


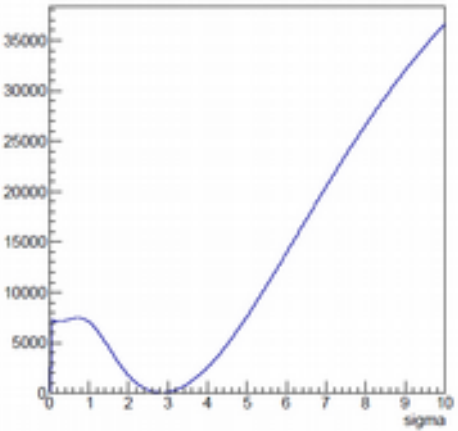


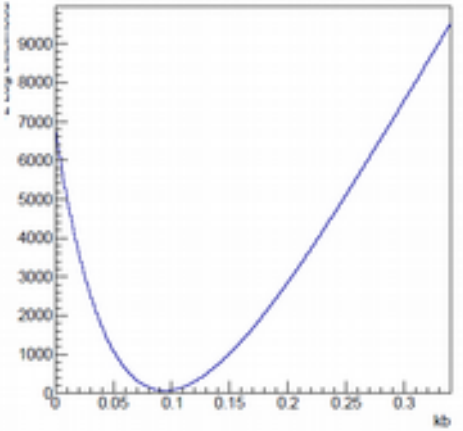






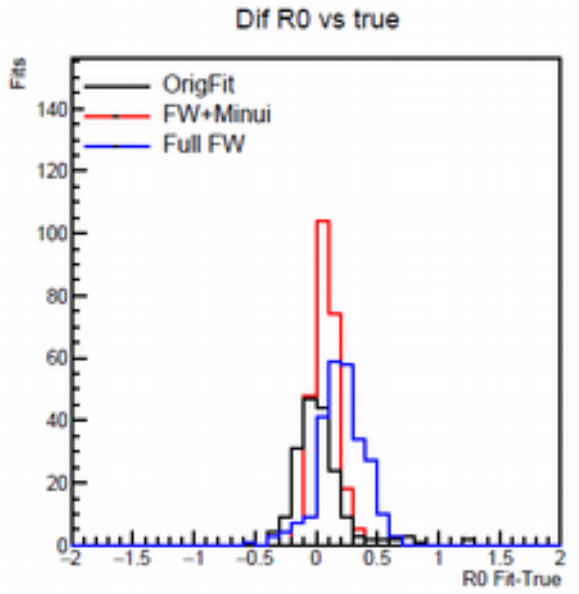






Pseudo ex results

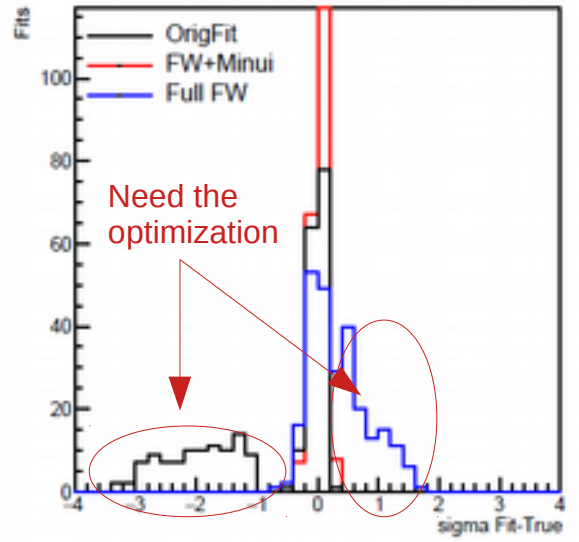
There are still small bias for the fit results from maybe initial and region for parameters.
FW func + Minuit looks best, but that is for just only this rough pseudo data.
It is better to optimize with more realistic data.



Speed check (w my local PC)

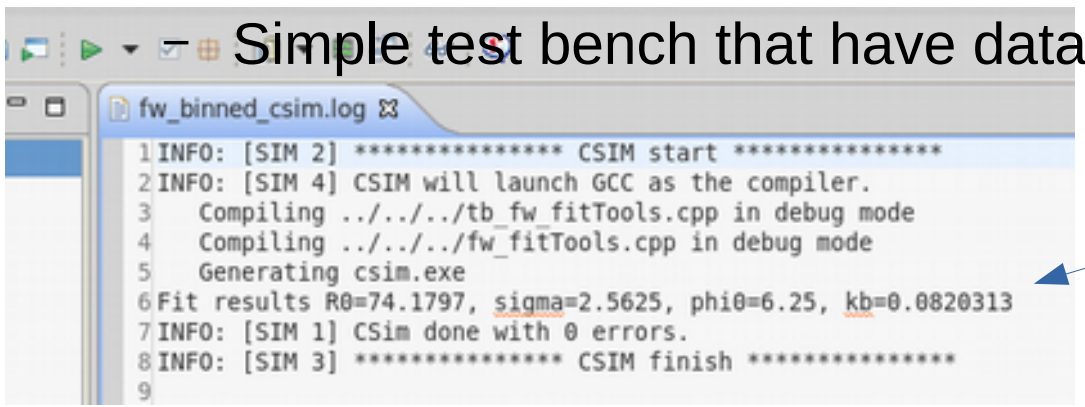
Original	:	5 Hz
FW func + Minuit	:	22 Hz
FW func + Fw Min	:	42 Hz

(not fair comparison. The fit function with limited integ division, limited loop for minimization)



FW implementation (only HLS)

- Simple usage of HLS
  - Remove all function that is not allowed to HLS
    - e.g. pow → exp(a+log(b))
    - Double to float
  - Input is ap_ufixed(16,8) for 32 bin's data and error and 4 input parameters and output parameters
  - Simple test bench that have data value and initial values



Vivado HLS
C simulation output

Similar results

FW implementation results

It is worst case

- **Just HLS, float calc, no parallelization**

Clock 100 MHz : ok
Fit frequency : 5-10 Hz
Resource usage : 0.4% FF and 5% LUT of xcvu37p

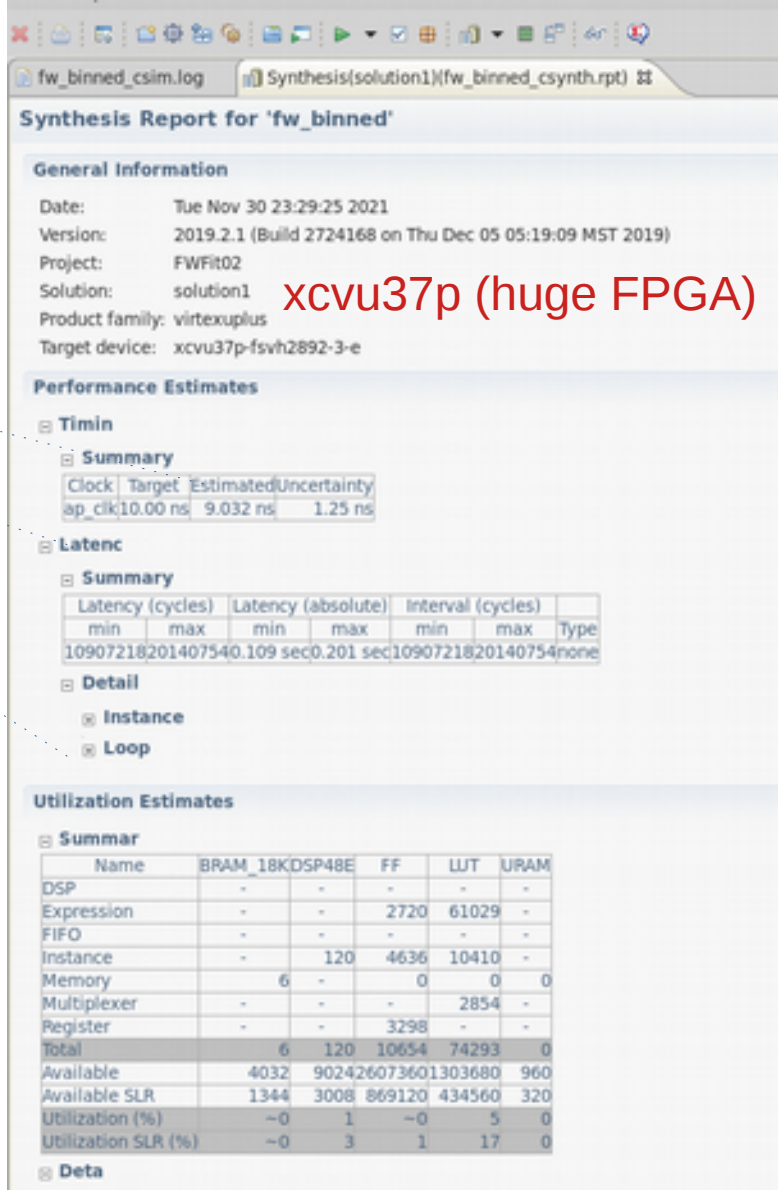
Expected improve point

- Float to fixed calc at least 50% resource (xilinx official)
- Each scan calc func 4 * 16 times, and that can parallelize
  64 time speed and resource

Fit parameter
Integration division = 16
N division for a bin average = 4
Minimization loop = 128

- Less # can loop? ½?
- VHDL code (no HLS) ~75% resource, and speed *2-4

Summary of rough expectation
1/3 resource from table at 15 Hz fits, and speed is linear func of resource usage up to ~1 kHz.
e.g 100 Hz fits with 7/3 resource of table


fw_binned_csim.log
Synthesis(solution1)(fw_binned_csynth.rpt)

Synthesis Report for 'fw_binned'

General Information

Date: Tue Nov 30 23:29:25 2021
Version: 2019.2.1 (Build 2724168 on Thu Dec 05 05:19:09 MST 2019)
Project: FWFit02
Solution: solution1
Product family: virtexuplus
Target device: xcvu37p-fsvh2892-3-e

xcvu37p (huge FPGA)

Performance Estimates

Timin

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	9.032 ns	1.25 ns

Latenc

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
109072182	014075402	0.109 sec	0.201 sec	109072182	014075402	none

Detail

Instance

Loop

Utilization Estimates

Summar

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	2720	61029	-
FIFO	-	-	-	-	-
Instance	-	120	4636	10410	-
Memory	6	-	0	0	0
Multiplexer	-	-	-	2854	-
Register	-	-	3298	-	-
Total	6	120	10654	74293	0
Available	4032	9024	2607360	1303680	960
Available SLR	1344	3008	869120	434560	320
Utilization (%)	~0	1	~0	5	0
Utilization SLR (%)	~0	3	1	17	0

Deta

Summary

3 options

- Keep software
  - ~40 Hz (FW like Func and Minimizer)
  - Only take average (“I” option) for max bin +/- 1 bin? 120 Hz?
  - Phi0 can fix? ¾ resource and time?

- HLS FW
  - Need float to fixed. Parallelization by IP core level.
  - Half resource. And double speed?.
  - Easy modification and maintenance

- Full vhdl optimized FW
  - Full controlled parallelization, and optimized calculaton (e.g. A*B = (A+B)^2 – A^2 -B^2 /2 with small LUT)
  - Very efficient. Hard development and maintenance. No scalability.

Backup

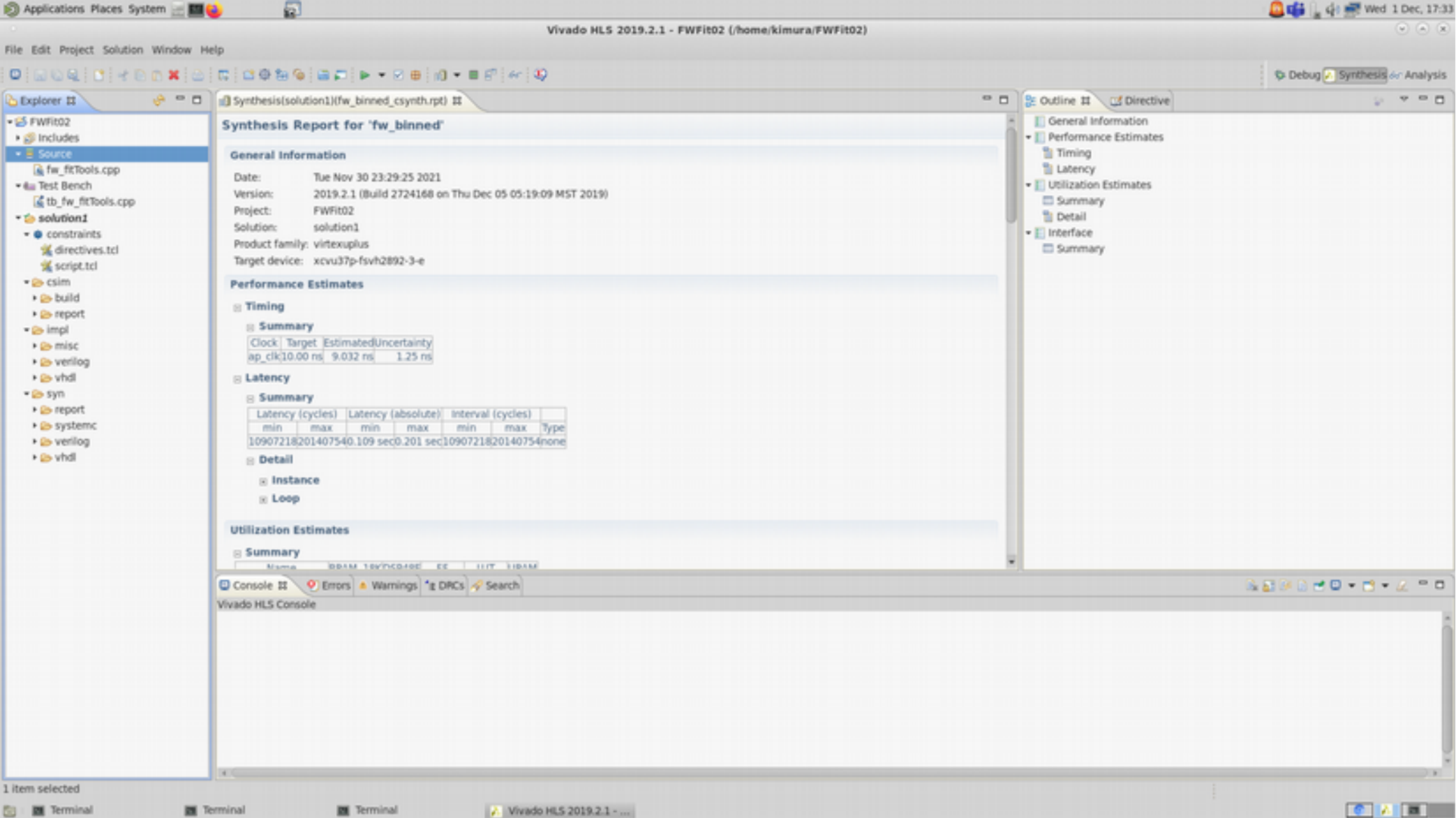
Code and usage

Files:
https://www.dropbox.com/s/g01lq0ssg35pmum/FitFPGA.tar.gz?dl=0

Origianl dir (Simeon/)
Added
my_FitTools.h :fit func for minuit w/o root lib
fw_FitTools.h : fit func with minimizer
In liveFit.cpp
-lMinuit was added to compile command.
int fitmethod=2; //0:original, 1:fwfunc+minuit 2:fwfunc_fwmini

FWFit02/
Codes are only fw_fitTools.cpp and tb_fw_fitTools.cpp
How to run:
Open vivado_hls -> new project (set name and FPGA) → add source(fw_fit...) → add test bench(tb_...) →project setting set fw_fit… as Top module → run C simulation (very slow) -> run C Synthesis ss in next page

Mytest/ (not usefull)
Pseudo.cc : pseudo data test
Mytest.cc : single event test


Applications Places System
Wed 1 Dec, 17:33
Vivado HLS 2019.2.1 - FWFit02 (/home/kimura/FWFit02)
File Edit Project Solution Window Help
Debug Synthesis Analysis
Explorer
FWFit02
Includes
Source
fw_fitTools.cpp
Test Bench
tb_fw_fitTools.cpp
solution1
constraints
directives.tcl
script.tcl
csim
build
report
impl
misc
verilog
vhdl
syn
report
systemc
verilog
vhdl
1 item selected
Synthesis(solution1)(fw_binned_csynth.rpt)
Synthesis Report for 'fw_binned'
General Information
Date: Tue Nov 30 23:29:25 2021
Version: 2019.2.1 (Build 2724168 on Thu Dec 05 05:19:09 MST 2019)
Project: FWFit02
Solution: solution1
Product family: virtexuplus
Target device: xcvu37p-fsvh2892-3-e
Performance Estimates
Timing
Summary
Clock Target Estimated Uncertainty
ap_clk 10.00 ns 9.032 ns 1.25 ns
Latency
Summary
Latency (cycles) Latency (absolute) Interval (cycles)
min max min max min max Type
1090721820140754 0.109 sec 0.201 sec 1090721820140754 none
Detail
Instance
Loop
Utilization Estimates
Summary
Outline
Directive
General Information
Performance Estimates
Timing
Latency
Utilization Estimates
Summary
Detail
Interface
Summary
Console
Errors
Warnings
DRCs
Search
Vivado HLS Console
Terminal
Terminal
Terminal
Vivado HLS 2019.2.1 - ...