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DEPARTMENT OF PHYSICS AND ASTRONOMY

PHD TRANSFER REPORT

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# A Quality Assurance Range Calorimeter for Proton Beam Therapy

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## Abstract

The goal of this project is to develop a scintillator-based range calorimeter for fast and accurate measurements of proton range. Such measurements are critical in proton beam therapy (PBT) to ensure accurate delivery of proton beams and minimise risk to patients. This report describes the detector prototype being developed by the UCL PBT group and the progress in upgrading its readout system from a CMOS image sensor-based system to a photodiode-based system that uses FPGA electronics for data processing. Details are also provided of the analytical proton depth-light model that is used to reconstruct proton ranges from calorimeter data and the evaluation of its current performance. Finally, plans for the next stages of development are provided, which consist of further FPGA design, detector characterisation and simulation, and extending the depth-light model.

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# 1 Introduction

Cancer is a disease where an abnormal growth of cells, caused by multiple changes in gene expression, creates an imbalance of cell proliferation and cell death [1]. It continues to be an incredibly challenging disease: each year there are around 367,000 new cases and around 165,000 cancer-related deaths in the UK [2]. 1 in 2 people in the UK born after 1960 will be diagnosed with some form of cancer in their lifetime.

Proton beam therapy (PBT) is a type of radiotherapy used to treat cancers with ionising radiation. The use of protons provides significant advantages over the conventional X-ray modality, namely due to the highly-localised dose (J/kg) delivered by protons [3], shown in Fig. 1. Localising dose allows healthy tissue to be spared, which is especially critical for treating tumours in paediatric patients and tumours near vital organs [4]. However, this requires accurate determination of the range of clinical proton beams, to ensure that planned treatments are delivered accurately and the risk to patients is minimised. This is known as daily quality assurance (QA), a legal requirement of every radiotherapy centre, which involves measuring the range of protons in water-equivalent material to sub-millimetre precision [5]. Water-equivalent material since water is used as an approximation of human tissue. Current methods of QA often have to choose between speed and accuracy, both of which are essential: slow measurements take time away from patient treatment and inaccurate measurements reduce confidence in treatment plans. PBT is becoming increasingly popular; while there are 90 facilities worldwide that are currently operational and another 58 under development or planning [6], these technical difficulties prevent PBT from reaching its full potential. The goal of this project is develop a detector for comprehensive daily QA that is both fast and accurate.

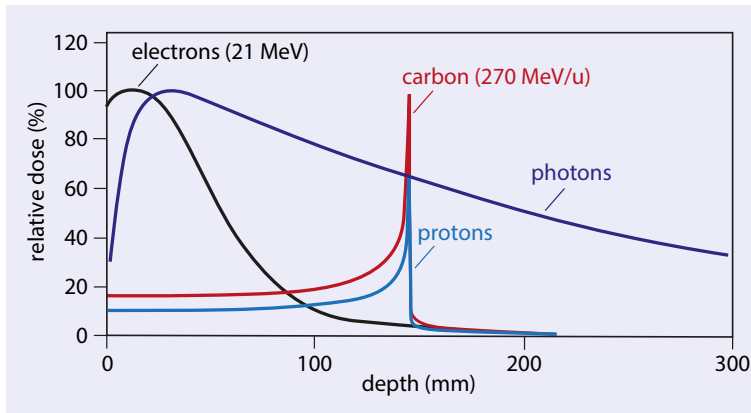


Figure 1: The variation of delivered dose with depth for several types of radiotherapy. The dose delivered by photons gradually decreases with depth, whereas the dose from protons culminates in a Bragg peak [7].

## 1.1 Current Methods of Quality Assurance

Most clinical methods of range QA use ionisation chambers submerged in water tanks, known as water phantoms. Such devices measure proton energy deposition from the current produced by liberated electron-ion pairs in the gas-filled chamber as ionising radiation passes through [8]. Such a device is the PTW (Freiburg, Germany) Peakfinder, which is a water column that can be sampled with an ionisation chamber

to measure proton depth-dose distributions with up to 10  $\mu\text{m}$  spatial resolution [9]. While accurate, the device is slow: measuring the depth-dose curve of a single proton energy takes several minutes and requires the beam to be delivered multiple times. A daily QA programme requires measurements of dose-depth curves of many (but not all) beam energies available at the facility [10], so QA is on the order of an hour with this device.



Figure 2: Detectors used for clinical daily QA.

Measurement times can be reduced through the use of multi-layer ionisation chambers (MLIC), where the dose-depth curve of a given proton energy can be measured with a single beam delivery. MLIC detectors, such as the IBA (Schwarzenbruck, Germany) Giraffe and Zebra, consist of a stack of ionisation chambers sandwiched between beam degrader plates [11, 12]. Both the Giraffe and Zebra have 180 ionisation chambers with pitch 2 mm but have 12 cm and 2.5 cm electrodes for measurements of small and large fields respectively. The spatial resolution is increased to 0.5 mm through fitting measurements to Thomas Bortfeld’s analytical approximation of the Bragg model [15]. The main issue with these detectors is the loss of water-equivalency from the use of degrader plates – calculating the water-equivalent thickness (WET) of the detector can become complicated due to WET being dependent on the beam energy and ion species [16]. Ionisation chamber detectors are also dependent on dose-rates and environmental conditions, and are subject to recombination [17]. Setup complexity is also an issue for both the Giraffe and Zebra.

Another detector for QA utilises the IBA Sphinx and Lynx together; the former is a custom set of absorbers while the latter is a scintillator-based detector used to measure the 2D beam profile perpendicular to the beam axis [13, 14]. This setup does not directly measure the depth-dose curve but instead infers proton range from comparison of the beam size after passing through the absorbers with previous, more accurate measurements made with other devices. All of these devices are expensive, ranging between £150-£250k, whereas the detector being developed in this project is estimated to have a production cost under £20k.

## 2 Prototype Detector for Fast Quality Assurance

A compact, inexpensive prototype detector for fast QA is under development by the PBT group at UCL. Comprehensive details about the detector concept, design, operation and analysis of test data to-date make up a recent publication [18]. A brief overview is provided here.

## 2.1 Detector Design

The main design goal for this detector is to allow direct WET measurements of proton range with only a single beam delivery, in a housing that can be mounted directly onto the beam nozzle for easy setup and measurement at every beam angle. The detector is made up of a stack of 49 2-3 mm thick,  $100 \times 100 \text{ mm}^2$  square plastic scintillator sheets, such that the beam direction is perpendicular to the planar surface of the sheet, as shown in Fig. 3a. The sheets are composed of a polystyrene-based scintillator (Nuvia a.s., Třebíč, Czech Republic) of density  $1.03 \pm 0.01 \text{ g/cm}^3$ , a decay constant of 2.5 ns and light output 56% that of anthracene [19]. The full stack has a thickness of 124.20 mm, making the average sheet thickness 2.53 mm. Despite quenching effects, where scintillation light output is non-linear under large rates of energy loss [20] (see section 2.2), the use of plastic scintillators for calorimetry is of interest due to their dose-rate independence, fast response times and water-equivalency [21]. The former is of particular interest for FLASH proton therapy, which uses large dose rates [22].

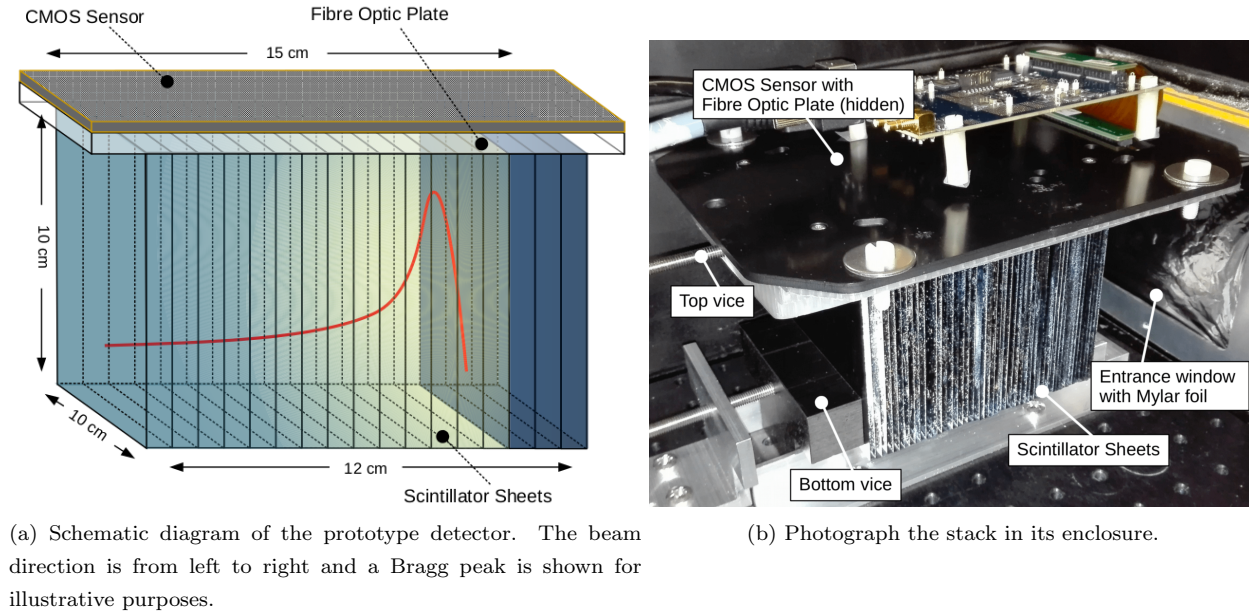
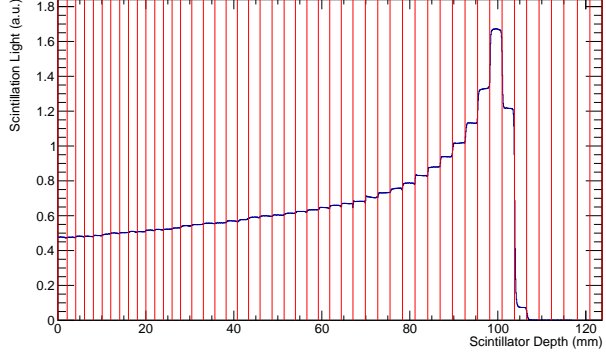
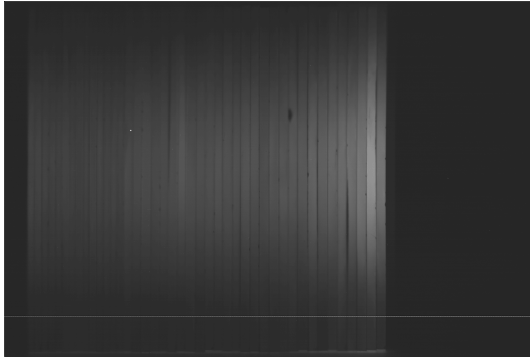


Figure 3: The Quality Assurance Range Calorimeter (QuARC). Images taken from [18].

Segmenting the active detector volume into sheets allows for a measurement of light in each sheet, to build a depth-light (PDL) curve, from which the energy deposited in each sheet can be calculated. The current version of the prototype uses a large flat-panel CMOS image sensor (ISDI, London, UK) of active area  $153.6 \times 103.0 \text{ mm}^2$  and pixel size  $0.1 \times 0.1 \text{ mm}^2$  [23] to take pictures of the entire stack, where the average light output in each sheet is reconstructed during data analysis. Directly coupling the sensor to the stack avoids the issue of having to correct for optical artefacts, which is necessary in other scintillator detectors read by DSLR cameras from a distance [24, 25]. The CMOS sensor is capable of taking 21 full-resolution images at a time (an acquisition time of 840 ms) – an example raw image of the stack with a 120 MeV proton beam taken at the Heidelberg Ion Therapy centre (HIT) is shown in Fig. 4a. The reconstructed PDL curve is shown in Fig. 4b. From this PDL, the average light output in each sheet is calculated and an analytical depth-light model is deployed to reconstruct the proton Bragg curve and recover the range.



(a) Raw TIF image taken by the CMOS sensor. The proton beam enters from the left and shows the sharp stop of protons after the brightest point (Bragg peak). (b) Reconstructed PDL curve from Fig. 4a. The vertical red lines represent the edges of each scintillator sheet. The average light output in each sheet is calculated and then fitted to an analytical model.

Figure 4: RAW TIFF image (left) and reconstructed PDL (right) of the detector taken by the CMOS image sensor with a 120 MeV proton beam at HIT.

## 2.2 Analytical Depth-light Model

In order to recover the proton range, the depth-light data is fitted to an analytical model developed by previous UCL PBT PhD student, Laurent Kelleter. The details of this model and its performance with both GEANT4 simulated data and real data make up a recent publication [26]. Again, only a brief overview is provided here. This so-called “quenched Bragg (QB) model” takes Thomas Bortfeld’s analytical approximation of the proton Bragg curve [15] (the blue curve in Fig. 1) and applies Birks’ law for scintillation light quenching [20] (which is significant in the Bragg peak) such that a PDL can be fitted using only a few free-parameters, one of which being the proton range. The final mathematical expression for the QB model is given in equation 1.

$$Q(z) = \int_0^{R_0} \frac{1}{\rho} \left[ \Phi_0 \frac{1 + \beta(R_0 - z')}{1 + \beta R_0} \frac{S}{\left( \frac{1}{p\alpha^{1/p}} (R_0 - z')^{1/p-1} \right)^{-1} + kB} + \gamma \Phi_0 \frac{\beta}{1 + \beta R_0} \times \right. \\ \left. \int_{z'}^{R_0} \frac{S}{\left( \frac{1}{p\alpha^{1/p}} (R_0 - z'')^{1/p-1} \right)^{-1} + kB} dz'' \right] \frac{1}{\sqrt{2\pi}\sigma} \exp \left( -(z - z')^2 / 2\sigma^2 \right) dz' \quad (1)$$

Where  $Q(z)$  is the light output,  $R_0^*$  is the proton range,  $\rho$  is the density of water,  $\Phi_0^*$  is the proton fluence factor,  $\beta$  is a slope parameter for fluence reduction,  $S$  is the scintillation light constant,  $\alpha$  and  $p$  are the proportionality factor and exponent of the range-energy relation respectively [27],  $\sigma^*$  is the width of Gaussian range straggling and  $kB^*$  is Birks’ constant, a measure of the amount of quenching. Terms marked with an asterisk are free-parameters in the fit. Setting  $S = 1$  and  $kB = 0$  recovers Bortfeld’s description of the Bragg curve, allowing for the non-quenched Bragg curve to be reconstructed from the fit result. The QB model is implemented using the data analysis framework ROOT and numerical integration is carried

out using the function `TF1::Integral()` [28]. An example fit after sheet light averaging is shown in Fig. 5.

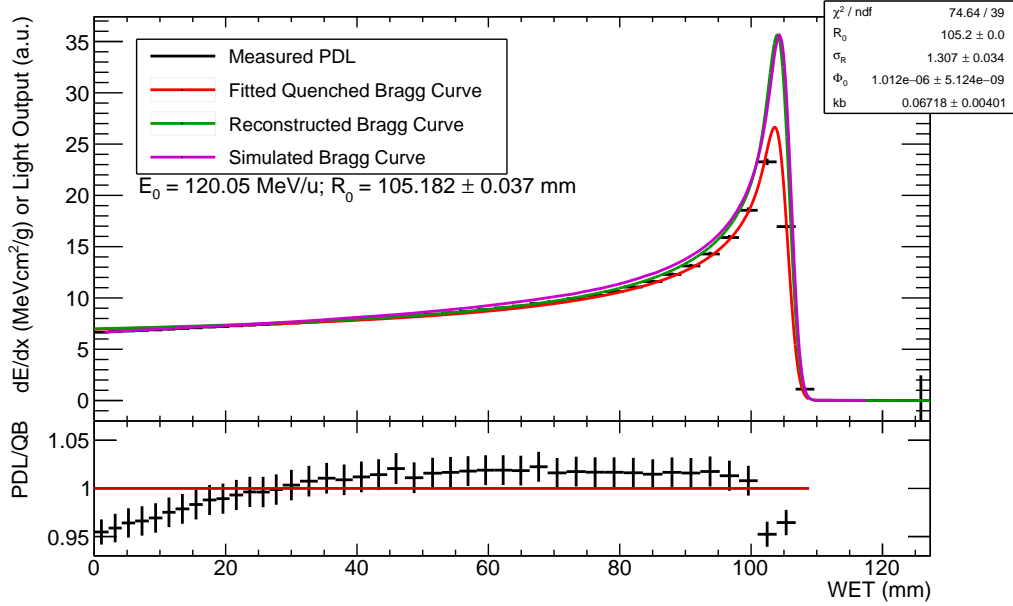


Figure 5: Fit result of sheet-averaged light output from Fig. 4b. The red curve represents equation 1, the green curve represents reconstructed Bortfeld curve (i.e. the red curve with  $S = 1$  and  $kB = 0$ ) and the magenta curve represents the benchmarked HIT reference curve for the delivered beam [29]. The residual plot shows the ratio between the red curve and the measured PDL. Only the fit uncertainty is shown.

### 2.2.1 Evaluating Model Performance

As an exercise to become familiar with the existing data analysis procedure, which will form the bulk of analysis for future tests, select data taken at HIT in April 2019 was reanalysed in an effort to corroborate the previous analysis discussed in [18]. Fig. 5 shows a typical result for a proton pencil (single-energy) beam, where the depth in scintillator was converted to WET (a small correction). As found before, there is generally an excellent agreement between the PDL and the QB model (within 5%) and between the reconstructed Bragg curve and facility reference. For a given energy, analysis of the effects of beam spot size (transverse size) on the reconstructed range was also repeated: the reconstructed ranges for a 120 MeV proton beam with a selection of different beam spot sizes is shown in Fig. 6, with a maximum variation in range of approximately 0.04 mm. Similar results were found in [18], where it was concluded that the reconstructed range is largely independent of the beam spot size due to the total uncertainty on the range being on the order of 0.2-0.5 mm.

An aspect that was not covered previously in the analysis of the HIT April 2019 data was the reconstruction of spread-out Bragg peaks (SOBP). An SOBP is a method of beam delivery in which several proton pencil beams of different intensities and energies are superimposed (delivered consecutively) to create a large, relatively flat region of consistently high dose [30]. Following the prescription of creating a spread-out Bragg peak [31] and using the beam delivery settings (i.e. the position, energy and number of protons delivered in

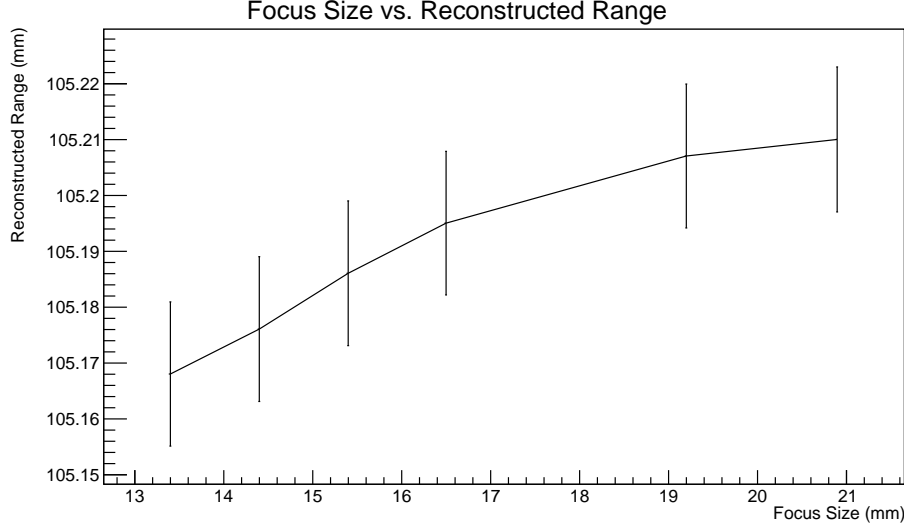


Figure 6: Variation of reconstructed range with beam spot size for a 120 MeV proton beam. The maximum range variation is approximately 0.04 mm. Error bars represent the fit uncertainty only – the full range uncertainty is on the order of 0.2-0.5 mm.

each beam), the benchmarked HIT reference pencil beam curves [29] were used to create a reference SOBP. A relatively straightforward extension of the QB model following the same guidelines allowed for a quenched SOBP fit, shown in Fig. 7.

There is a good match between the measured PDL and the QB curve, again agreeing within 5%. However, the plateau of the reconstructed SOBP is too narrow compared to the reference and is slightly tilted. The discrepancy in plateau width was attributed to a measurement error, where the CMOS sensor was not triggered at the correct time and so missed some of the lower energy proton beams. The tilt of the plateau is likely due to quenching: the deeper side of the plateau is primarily made up of the dose in the peak of higher energy beams, whereas the dose on the shallower side of the plateau is made up of several Bragg curve plateaus, which experience less quenching due to the smaller  $\frac{dE}{dz}$ . This then produces a tilt in a region where there should be consistent light output and it is currently unclear whether removal of the quenching parameters to reconstruct the non-quenched SOBP will eliminate the tilt entirely. Nevertheless, the fit result is promising and will be tested with better quality data in future experiments.

While the detector is primarily intended for use in proton therapy, investigations have been made in its use for other ion therapy modalities, namely helium and carbon. Helium and carbon ions are more ionising than protons due to their greater electric charge and so exhibit sharper Bragg peaks than protons (carbon more so than helium) [32], as shown in Fig. 1. This has the potential for an even more localised dose, however there is a non-negligible dose delivered beyond the peak, especially with carbon [33]. There are currently 12 facilities that provide clinical carbon therapy [6] and there is interest in helium ions being an optimal middle-ground between protons and carbon [34]. It is expected that the QB model will perform reasonably well with helium ions but not be a good description of the depth-dose relation for carbon. This is primarily due to Bortfeld’s model not taking into account nuclear fragmentation [35].



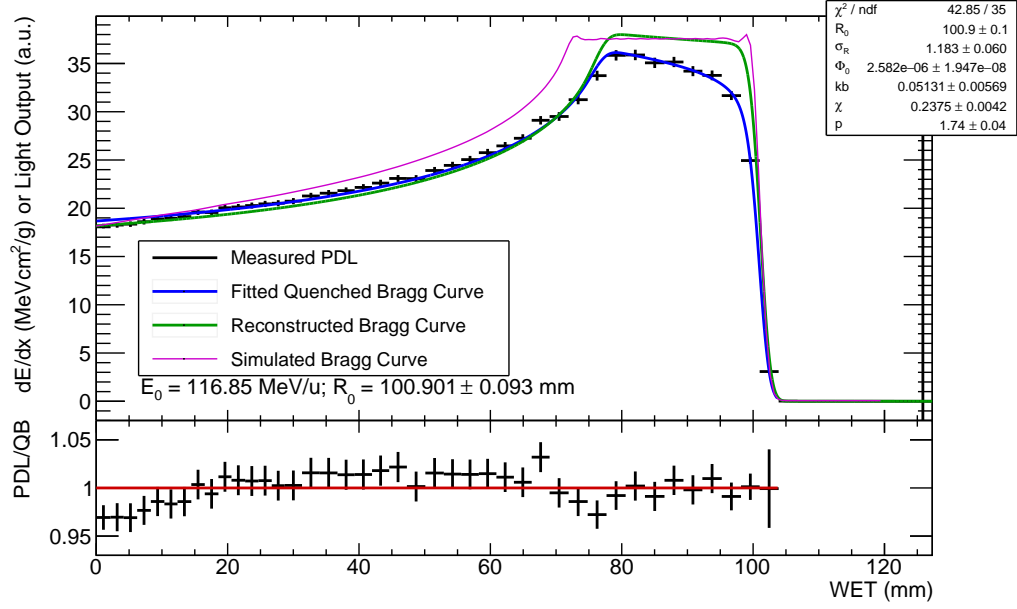


Figure 7: Fit result of an SOBP made up of 15 proton pencil beams, ranging from 98.27 MeV to 116.85 MeV. The magenta curve is a reference SOBP constructed from reference pencil beam data weighted according to the number of particles delivered in each beam. Only the fit uncertainty is shown.

Helium and carbon pencil beam data from HIT taken in April 2019 was analysed to test the performance of the QB model with ions. At the time of writing, reference helium and carbon data for HIT is unavailable, so any analysis could not be verified as has been done thus far. Efforts are being made to obtain this data. To assist in the fitting procedure, reference continuous slowing-down approximation ranges from the library “libdEdx” [36, 37] were used as initial estimates of  $R_0$  and the fit range was limited to avoid the fragmentation tail after the Bragg peak. The parameters  $\alpha$  and  $p$  were adjusted appropriately from GEANT4 simulations of the range-energy relation for helium and carbon. The results of the fit are shown in Fig. 8. It can be seen that the QB model is able to fit the PDL data well however, no conclusive statements can be made about the quality of the fit due to the unavailability of reference dose-depth curves for comparison. The close match between the PDL and QB model for carbon is suspect, as the QB model is expected to behave worse (indeed, the peak of the carbon PDL is missed by the model) and the values of  $\sigma$ , which is smaller for sharper Bragg peaks, is greater for both helium and carbon than for protons where the opposite is expected. The planned steps to improve the fitting are discussed in section 4.2.

## 2.3 New Prototype Design

So far the range telescope has demonstrated excellent performance with proton beams, being able to consistently reconstruct proton ranges to sub-mm precision, the core requirement for a daily-QA device, and has even shown potential for online treatment monitoring [38]. The device is compact, inexpensive and has shown excellent radiation hardness [18]. The next objective of the prototype design is to increase the speed

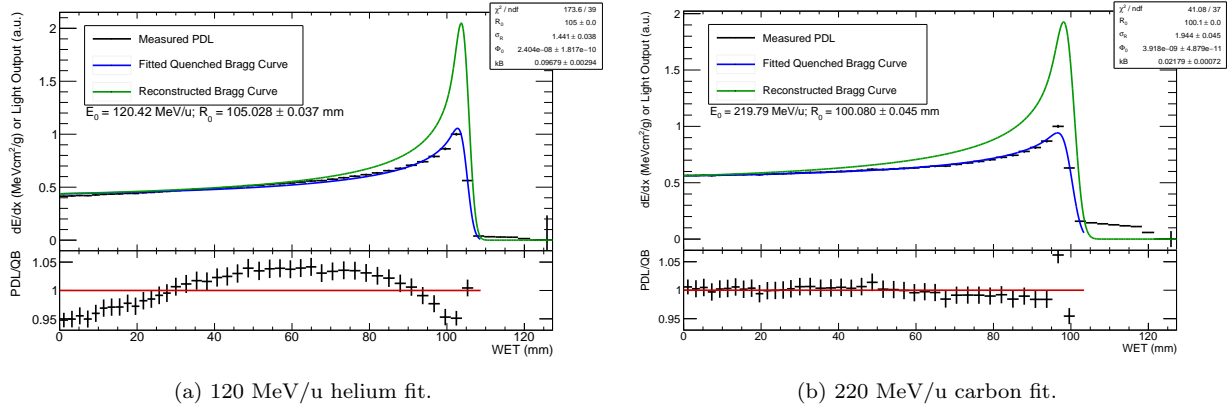


Figure 8: Fit result of helium and carbon pencil beams. At the time of writing, reference curves from HIT are unavailable. Only the fit uncertainty is shown.

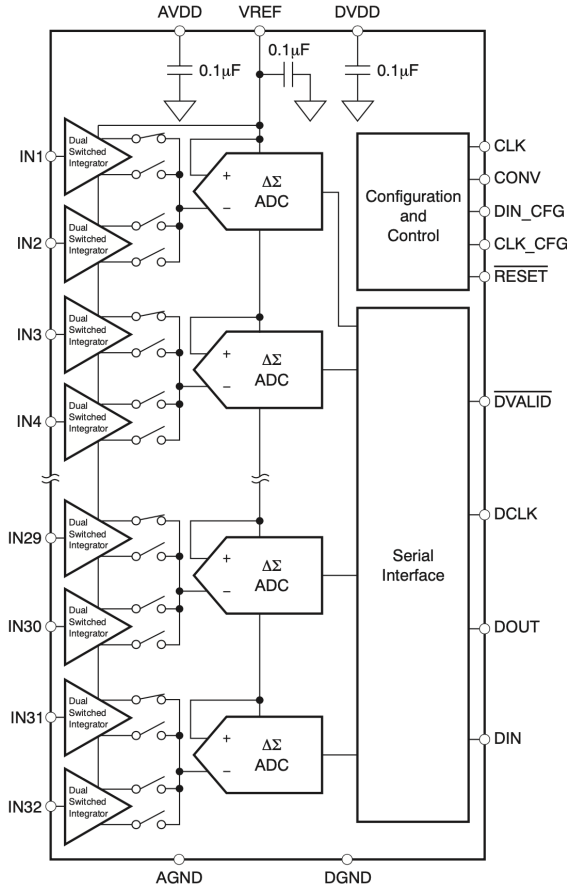
of measurements and move away from the CMOS-sensor based readout system. The CMOS sensor is delicate to handle, requires involved image analysis to find the average light output in each scintillator sheet and goes against the modular design goals of the detector, since the number of sheets is dictated by the size of the sensor. A photodiode-based readout system has been chosen, where each scintillator sheet is coupled to a photodiode to allow direct measurement of the light output in each sheet without the need for any image analysis. The photodiodes are connected to an analogue-to-digital converter that is configured and read by an FPGA, which then sends data to a PC.

### 3 FPGA Design

A Texas Instruments (Dallas, Texas, United States) DDC232CK (DDC) [39] was chosen as the current-input analogue-to-digital converter for its speed, large dynamic range and low power requirements. It is capable of measuring the currents of up to 32 photodiodes with an adjustable integration time ( $160 \mu\text{s} - 1 \text{ s}$ ) and full-scale range (FSR,  $12 \text{ pC} - 350 \text{ pC}$ ). Each of the 32 inputs on the DDC has two integrators, allowing for zero-deadtime measurements: while one integrator digitises and transfers data, the other measures the input current. The DDC is housed on a compact custom circuit board manufactured by CosyLab (Ljubljana, Slovenia), where the charge collected by a photodiode is split across two DDC inputs to give 16 photodiodes per DDC, shown in Fig. 9b. The circuit diagram illustrating the basic design of the DDC and required input and output signals is shown in Fig. 9a. The role of each digital signal is described below:

- *CLK* (input): 10 MHz clocking signal that is used to time the internal operations of the DDC, including generation of  $\overline{DVALID}$ .
- *CONV* (input): signal that controls integration, the time period of which is equal to the integration time. When this signal toggles, the integrator of each input switches.

- *DIN\_CFG* (input): serial data stream of the 12-bit sequence used to set key parameters of the DDC, namely the FSR and measurement precision (16-bit or 20-bit).
- *CLK\_CFG* (input): 20 MHz clocking signal used to time sending and reading of *DIN\_CFG*.
- $\overline{RESET}$  (input): Asynchronous active-low reset signal for the DDC to revert it to its power-up state.
- *DCLK* (input): 20 MHz clocking signal used to time sending and reading of *DOUT*.
- $\overline{DVALID}$  (output): active-low signal used to indicate that data is ready to be read on *DOUT*.
- *DOUT* (output): serial data stream of the 640-bit sequence (when in 20-bit precision mode) containing measurements of the 32 inputs.
- *DIN* (input): serial data input to the DDC used to daisy-chain other DDCs (see section 3.4).



(a) Circuit diagram for the DDC [39].



(b) Custom circuit board housing the DDC

Figure 9: Circuit diagram and board for the DDC232CK. Required signals from the FPGA are: *CLK*, *CONV*, *DIN\_CFG*, *CLK\_CFG*,  $\overline{RESET}$  and *DCLK*. Signals sent to the FPGA are:  $\overline{DVALID}$  and *DOUT*. The board houses 16 photodiodes since the charge of each is split across two inputs of the DDC.

The FPGA used to communicate with the DDC is a Xilinx (San Jose, California, United States) Zynq-7000 [40] on a Digilent (Pullman, Washington, United States) Zybo Z7-10 [41] development board, which

features a built-in ARM Cortex-A9 processor and a host of peripheral connections. The board and the key user-features of the design to communicate with the DDC and PC are shown in Fig. 10. The FPGA design was written in VHDL using Xilinx Vivado Design Suite 2020 [42]. Further details of the design-assigned purpose of the on-board buttons, switches and LEDs are provided below:

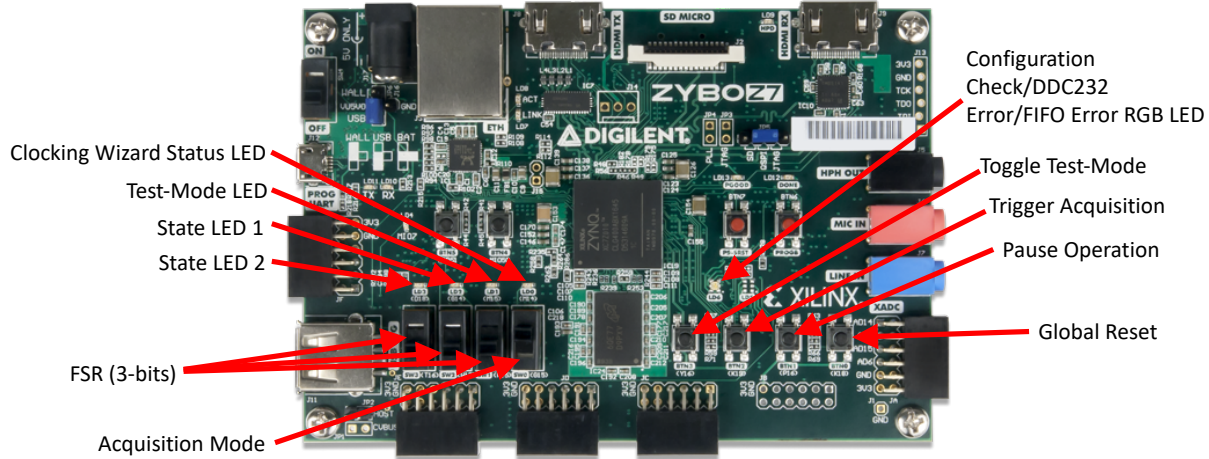


Figure 10: The Zybo Z7-10 [41]. Labelled are the assigned functions of the on-board buttons (right), switches (bottom-left) and LEDs (top-left and top-right).

- **Clocking Wizard Status LED:** the 125 MHz FPGA master clock is converted to a 120 MHz clock using the Xilinx Clocking Wizard intellectual property (IP) [43], to allow for easier generation of the 10 and 20 MHz signals required by the DDC. This LED is on when the Clocking Wizard component of the design is generating a stable clock. All FPGA operations are timed using this clock.
- **Test-mode LED:** the DDC can be configured into a test diagnostic mode for debugging, in which all the inputs give a zero signal (slightly above zero due to noise and a negative current offset). This LED is on when the user has enabled the test mode, which can be toggled using the Toggle Test-Mode button and becomes active after a Global Reset press.
- **State LED 1:** this LED is on whenever the DDC in the power-up, idle, or configuration state.
- **State LED 2:** this LED is on whenever the DDC is measuring or shifting out data.
- **Acquisition mode:** this switch toggles between the continuous and triggered acquisition modes. In continuous mode, data will be output to the PC as fast as possible, the rate of which is dependent on the chosen integration time and the speed of the data transfer (see section 3.3). When in triggered mode, the next measurement after the Trigger Acquisition button is pressed is sent to the PC.
- **FSR Switches:** these 3 switches control the 3-bit FSR code, which allows the user to choose between the 8 different dynamic ranges (see section 3.1).
- **Global Reset:** this button resets all aspects of the FPGA and DDC. Any changes since the last reset in the FSR, acquisition mode or test-mode settings are applied. The DDC returns to its power-up state and reconfigures before resuming operation.

- Pause Operation: this button idles the FPGA and DDC, all signals are held at their default value apart from the 120 MHz master clock. Pressing Global Reset restarts operation.
- RGB LED: this LED will be green if the DDC is configured correctly (see section 3.1), red if configuration is incorrect or if too short an integration time is chosen, or blue if the first-in first-out (FIFO) interface is read when empty or is written to when full (see section 3.3).

### 3.1 Configuration

The DDC must first be configured with a 12-bit sequence of data sent on *DIN\_CFG*, where:

- Bits 11-9 correspond to the 3 FSR bits, allowing for 8 different dynamic ranges; 000 = 12.5 pC, 001 = 50 pC, 010 = 100 pC, 011 = 150 pC, 100 = 200 pC, 101 = 250 pC, 110 = 300 pC, 111 = 350 pC. These correspond to the maximum charge that can be integrated in the photodiodes. 350 pC is typically chosen to minimise risk of saturation of inputs.
- Bit 8 corresponds to the resolution of output data: 0 = 16-bits, 1 = 20-bits. 20-bit resolution is chosen for better precision, at the price of slower readout (due to more bits of data requiring shifting out).
- Bit 7 corresponds to the device version. For the DDC232CK, this bit is set to 1.
- Bit 6 corresponds to a DDC internal divider of the *CLK* signal. This is set to 0 for no division.
- Bits 5-1 are empty bits set to 0.
- Bit 0 corresponds to the diagnostic test mode setting: 1 = on, 0 = off.

This gives a configuration input for normal operation of: 111110000000. Note that all vectors of data in this design are “little-endian”, in which the bits are labelled from the most-significant bit (MSB) to the least-significant bit (LSB) and are sent to and from devices MSB first. For the configuration input, this means bit 11 is sent first and bit 0 is sent last. After the configuration data is sent, a 640-bit (when in 20-bit mode, which is equal to the number of bits sent during a measurement readout cycle) read-back is sent to confirm configuration settings and test data output. The 640-bits are a 320-bit sequence sent twice, which contains the 12 configuration bits that the DDC received, a 4-bit revision ID (0001), 244 zeros and then a 70-bit test pattern, used as an extra check. In hexadecimal, the test pattern is: 30F066012480F69055. The timing diagram for configuration is shown in Fig. 11.

After the DDC is powered up and power supplies have stabilised, a reset pulse of width  $t_{RST} = 1 \mu s$  must be sent and after  $t_{WTRST} = 2 \mu s$ , the configuration data is sent through *DIN\_CFG* on the rising edges of *CLK\_CFG*, to be read by the DDC on the falling edges of *CLK\_CFG*.  $t_{STCF}$  and  $t_{HDCF}$  (both 10 ns) are the minimum times required for *DIN\_CFG* to be valid before and after falling edges of *CLK\_CFG* respectively.  $t_{WTWR} = 2 \mu s$  later, configuration read-back begins on *DOUT* where the pattern is read on the rising edges of *DCLK*, after which *CONV* is strobed (i.e. high for one *CLK* cycle) to begin integration.

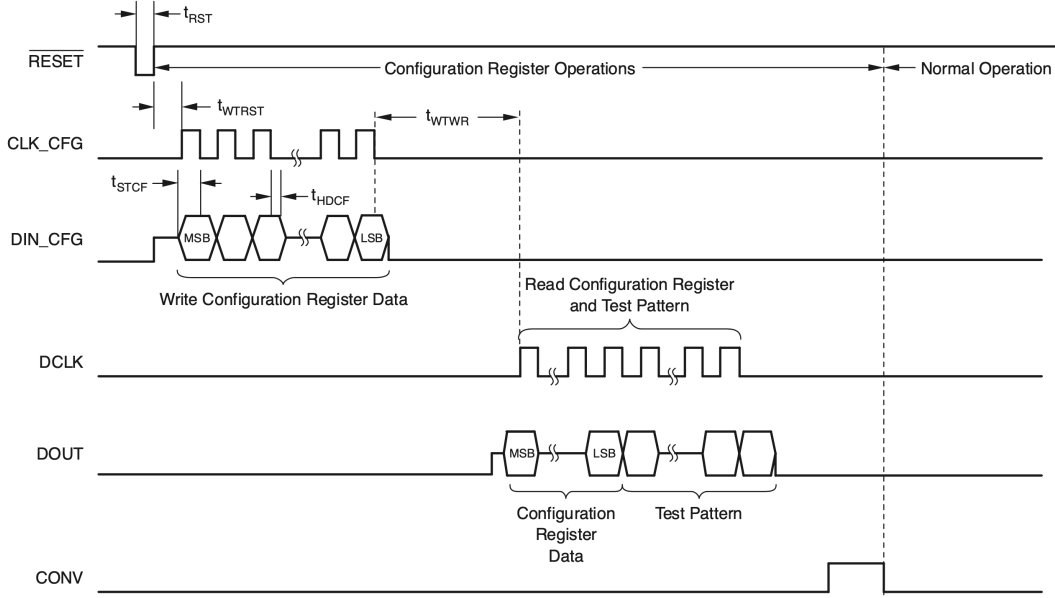


Figure 11: Timing diagram for configuration input and read-back [39].

To monitor signals on the FPGA for debugging purposes, the Xilinx Integrated Logic Analyser (ILA) IP [44] was used as a debug core for the design. This component allows for a pre-specified number of samples of a user-defined selection of signals to be displayed in a waveform diagram entirely within Vivado on user-defined trigger conditions. A trigger on the falling edge of  $\overline{RESET}$  was used to show the results of the configuration process, giving the waveform diagram shown in Fig. 12, confirming correct operation. Zoomed-in sections of Fig. 12 showing the configuration write and the start of the read-back process can be seen in Fig. 13a and Fig. 13b respectively. As mentioned earlier, the RGB LED on the Zybo will shine green for quick visual confirmation if the correct configuration pattern is received: this was achieved by storing the correct 640-bit pattern on the FPGA for comparison purposes.

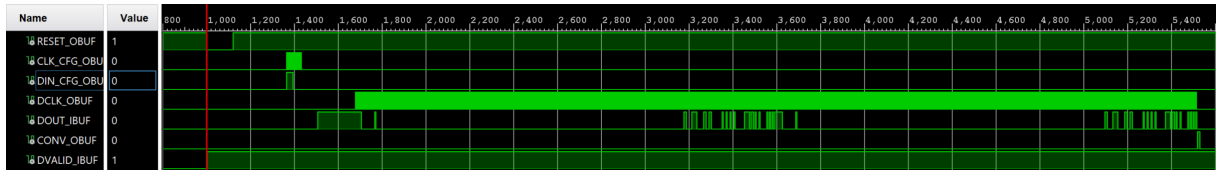
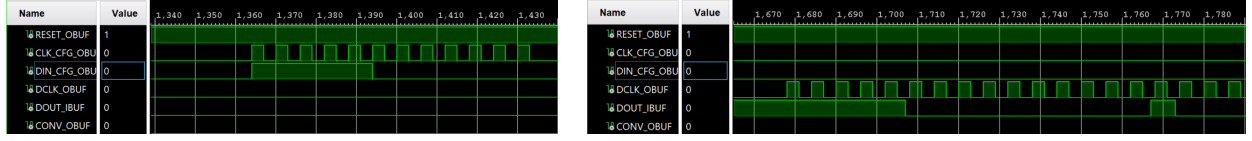


Figure 12: Overview of the real FPGA signals during the configuration process, captured using the ILA IP and triggered on the falling edge of  $\overline{RESET}$  (red line). Solid bright green bars are signals switching too fast to display at the current level of zoom.

### 3.2 Integration

After  $CONV$  is strobed at the end of the configuration read-back, it begins alternating with a time period  $t_{INT}$ , which is the integration time set by the user. Toggles in  $CONV$  represent transitions in the dual-integrators, where one side completes integration and begins measurement, reset and auto-zeroing while the



(a) Configuration write. The bits 111110000000 are written to the configuration register of the DDC on the falling edges of  $CLK\_CFG$ .

(b) Start of configuration read-back. Bits are read by the FPGA on rising edges of  $DCLK$ . The first 12 bits read are the configuration data, matching those sent during the configuration write.

Figure 13: Zoomed-in sections of Fig. 12 showing configuration write and read processes.

other side, currently idling after having finished these three tasks, begins integration. Measurement, reset and auto-zeroing take  $t_{MRAZ} = 1612 \pm 2 \text{ CLK}$  cycles and  $\overline{DVALID}$  is asserted after  $t_{CMDR} = 1382 \pm 2 \text{ CLK}$  cycles, signalling that data ready to be shifted out on  $DOUT$ . This is depicted in the timing diagram for integration, shown in Fig. 14.

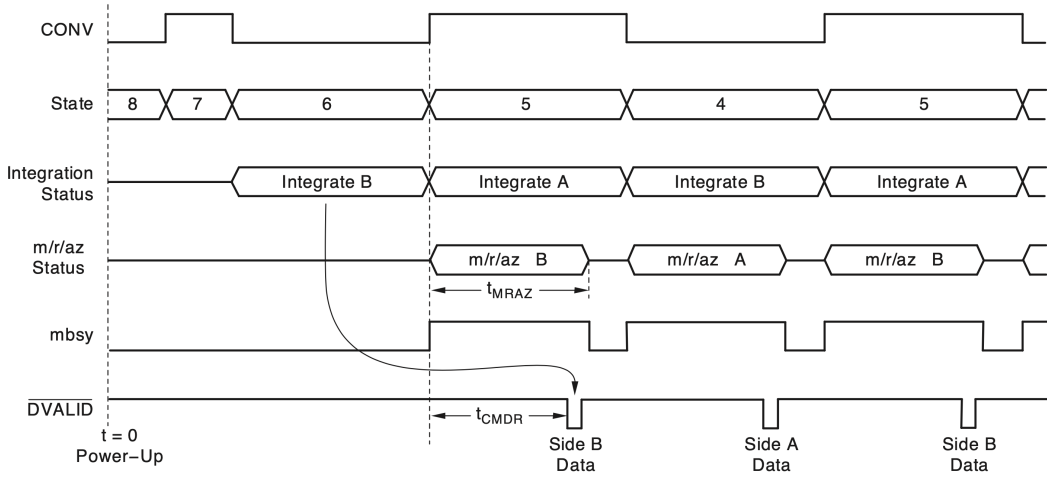


Figure 14: Timing diagram for integration [39].  $mbsy$  is an internal DDC signal not available to the user that is high whenever measurement, reset and auto-zeroing are taking place.

### 3.3 Data Transfer

Once  $\overline{DVALID}$  is asserted, photodiode data can be shifted out to the FPGA on the rising edges of  $DCLK$ . Each of the 32 DDC inputs is represented by a 20-bit number, which can then be converted to a charge in pC. The simplest method of data retrieval is after  $\overline{DVALID}$  goes low and before the next  $CONV$  toggle, as shown in Fig. 15. A key requirement for the DDC to be operated in continuous mode with this method, i.e. with zero dead-time between measurements (not to be confused with the FPGA continuous/triggered acquisition settings), is that the integration time must be sufficient to complete measurement, reset, auto-zero and shifting out of data before the next  $CONV$  toggle. Otherwise, the DDC enters a non-continuous mode where integration stops until the aforementioned processes have finished on both input integrators.



This mode of data retrieval gives a minimum integration time of:

$$t_{INT} = t_{CMDR} + t_{SDCV} + \frac{n_{bits}}{f_{DCLK}} = \frac{1382}{10\text{MHz}} + 10\mu s + \frac{32 \times 20}{20\text{MHz}} \approx 181\mu s \quad (2)$$

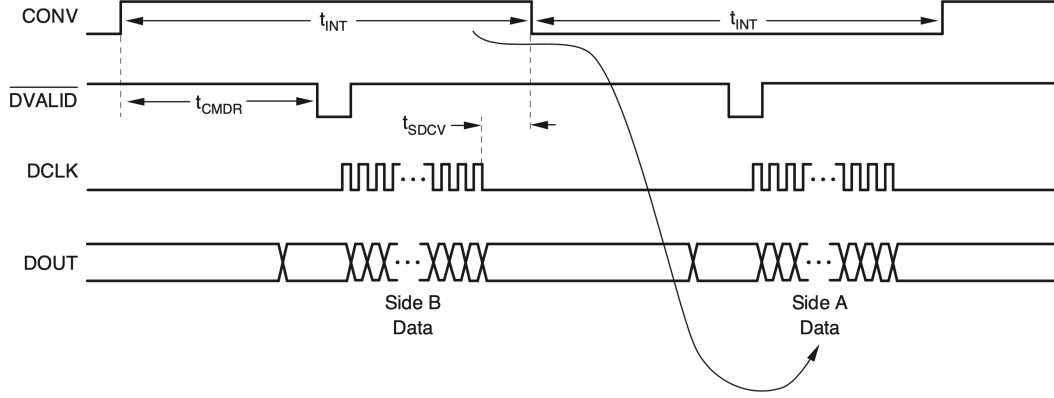


Figure 15: Timing diagram for data retrieval before *CONV* toggles [39]. Activity in *DCLK* must not occur within  $t_{SDCV} = \pm 10 \mu s$  of a *CONV* toggle.

Regardless of whether the FPGA is in continuous or triggered acquisition modes, each measurement sent by the DDC is read, though they are not always sent to the PC (see below). The FPGA has a 640-bit register that is overwritten every time new data arrives. Before being sent to the PC, a measurement is first sent to a FIFO interface on the FPGA. The FIFO was added to the design using the Xilinx FIFO Generator [45] and has the following signals:

- *WR\_EN*: FIFO write enable. When high, a byte is written to the FIFO on clock rising edges.
- *RD\_EN*: FIFO read enable. When high, the oldest byte in the FIFO is read on clock rising edges.
- *FULL*: High when the FIFO is full.
- *EMPTY*: High when the FIFO is empty.
- *WR\_ACK*: High when a byte has been written successfully.
- *VALID*: High when a byte has been read successfully.
- *OVERFLOW*: High if FIFO is written to when full and causes the Zybo RGB LED to turn blue.
- *UNDERFLOW*: High if FIFO is read when empty and causes the Zybo RGB LED to turn blue.

A 640-bit measurement received by the FPGA is written to the FIFO in byte-sized pieces, such that the FPGA is quickly ready again to read new data. The measurement is then sent from the FIFO to the PC over the universal asynchronous receiver-transmitter (UART) protocol, which sends data a byte at a time (hence the storage of a measurement in bytes in the FIFO). The principle of the UART protocol is shown in Fig. 16 and the key user settings are:



- Baud rate: the number of bits transferred per second (including start and stop bits). This is set to 921600, which is often the maximum standard baud rate for serial ports.
- Data bits: the number of bits of data sent in a packet. This is set to the maximum number, 8.
- Stop bit: the number of bits at the end of the data bits to denote the end of data. This is set to the minimum, 1.

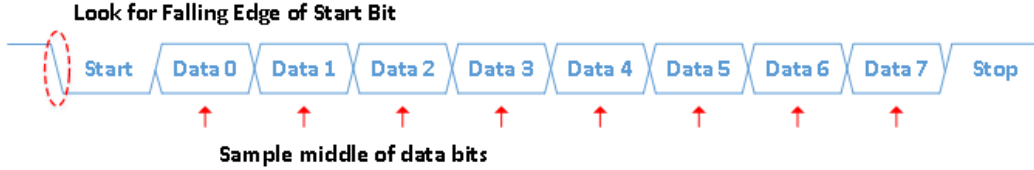


Figure 16: Basic principle of the UART protocol for data transfer [46]. The device receiving data looks for the falling edge of the start bit, which is logic 0 (the line is driven high when inactive), and then samples the middle of each data bit, which is calculated using the clock and baud rates. The stop bit is logic 1.

Key signals for the UART transmitter used to send data from the FPGA to the PC:

- *TX\_DV*: Data valid signal sent to the UART transmitter to state that data is ready for transmission. Functionally, this serves the same purpose as the *FIFO\_VALID* signal.
- *TX\_ACTIVE*: High when the UART transmitter is sending data to the PC.
- *TX\_DONE*: High for one clock cycle after a byte is sent.
- *TX\_SERIAL*: Actual data stream sent to the PC.

Putting together the integration, FIFO storage and UART transmission gives the waveform diagram shown in Fig. 17 and Fig. 18. The trigger was set on the falling edge of the Trigger Acquisition button signal (the FPGA was in triggered mode), after which the next measurement read by the FPGA is stored into the FIFO and then sent over UART. Subsequent measurements are only read, to be overwritten by the next (until the button is pressed again). At the falling edge of  $\overline{DVALID}$ ,  $DCLK$  begins to shift in data on  $DOUT$ , after which the measurement is stored in bytes into the FIFO. The UART transmitter then sends data one byte at time. Note that a 32-bit custom end-of-line sequence is added to the end of each measurement, used to separate measurements when saved to a text file on a PC. Since each byte sent over UART contains a start and stop bit, there are actually  $640 + 32 + 84(2) = 840$  bits to be sent over UART for the  $\frac{640+32}{8} = 84$  bytes of data saved in the FIFO per measurement.

When the FPGA is in continuous mode, the next read measurement is sent to the FIFO as soon as the UART transmitter has finished sending the last measurement (i.e. when the FIFO becomes empty again). This was chosen so that the FIFO does not fill up over time if the UART transmitter cannot keep up and practically means that the FIFO will only ever contain a maximum of one measurement at any given time. While not the most conventional use of a FIFO, it allows for the DDC integration time to be independent of

the data transmission speed: the shortest integration times, calculated in equation 2, are still available as the time taken for a measurement to be stored into the FIFO is negligible compared to the UART transmission rate. The FIFO will also prove essential in the future design plans, discussed in section 3.4. The minimum time taken for a measurement to be read from one DDC, saved to the FIFO and then sent using the UART protocol is given in equation 3.

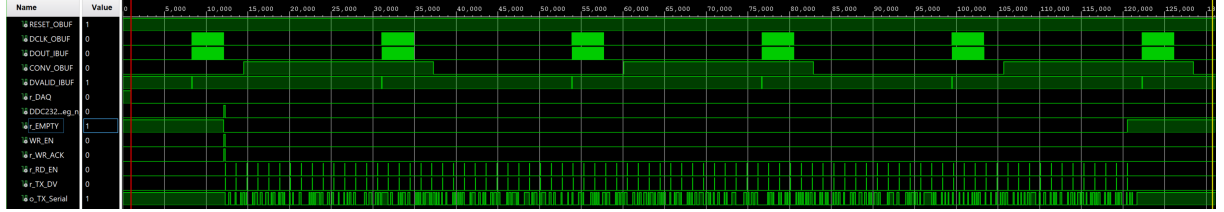
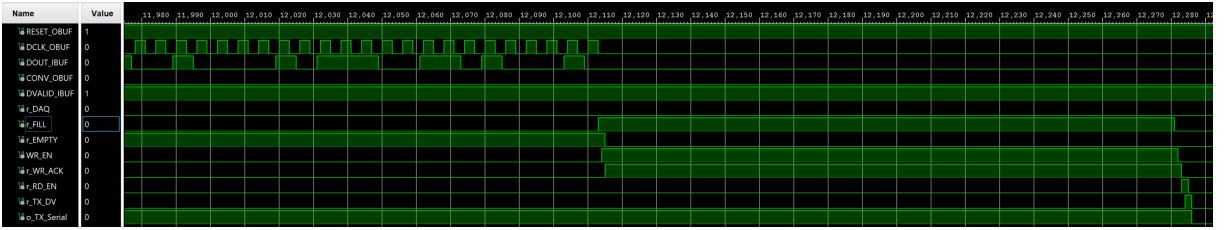
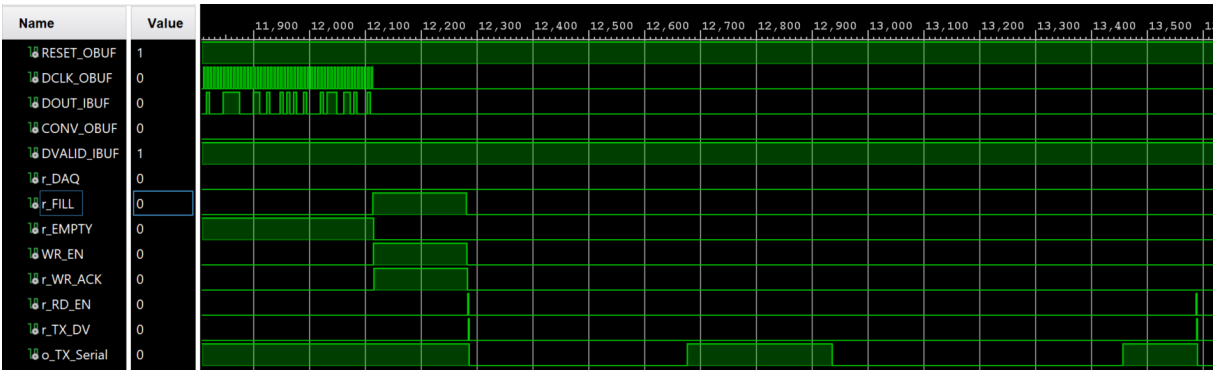


Figure 17: Overview of the FPGA signals during a readout cycle. While the UART transmitter sends data, new measurements are read but are not sent to the FIFO. The time taken for the measurement to be stored in the FIFO is represented by the duration that  $WR\_EN$  is high. The UART starts working when  $RD\_EN$  first goes high and finishes when  $EMPTY$  has been reasserted.



(a) The end of data being shifted in on  $DOUT$  and the period where data is being written to the FIFO.  $FILL$  indicates that a measurement for transmission has been received.  $WR\_EN$  and  $WR\_ACK$  are offset by one clock cycle as expected.



(b) Transmission of the first byte, which was 00001100, sent LSB first and book-ended by a low start bit and high stop bit.

Figure 18: Zoomed-in sections of Fig. 17 showing aspects of the data transfer process.

$$\tau_{\text{DATA}} = \frac{n_{\text{bits}}}{f_{\text{DCLK}}} + \frac{n_{\text{bytes}}}{f_{\text{Zybo}}} + \frac{n_{\text{UART Bits}}}{\text{Baud Rate}} = \frac{640}{20\text{MHz}} + \frac{84}{120\text{MHz}} + \frac{840}{921600 \times 10^{-6}} \approx 945\mu\text{s} \quad (3)$$

Data sent over UART is saved to a text file using the CoolTerm [47] serial terminal emulator. This program was chosen for its ability to view and save incoming data as hexadecimal (instead of ASCII), accept

the 921600 baud rate and accept custom end-of-line strings such that each measurement is timestamped and saved to a new line in the text file, discarding the end-of-line string. While the application saves data, a C++ script is run that reads the latest measurement, converts it to charge values in pC and then plots the result live in a graph using ROOT, as shown in Fig. 19. ASCII commands can also be sent from the PC to a UART receiver in the design, which is similar to the transmitter, to reset, pause and trigger acquisitions.

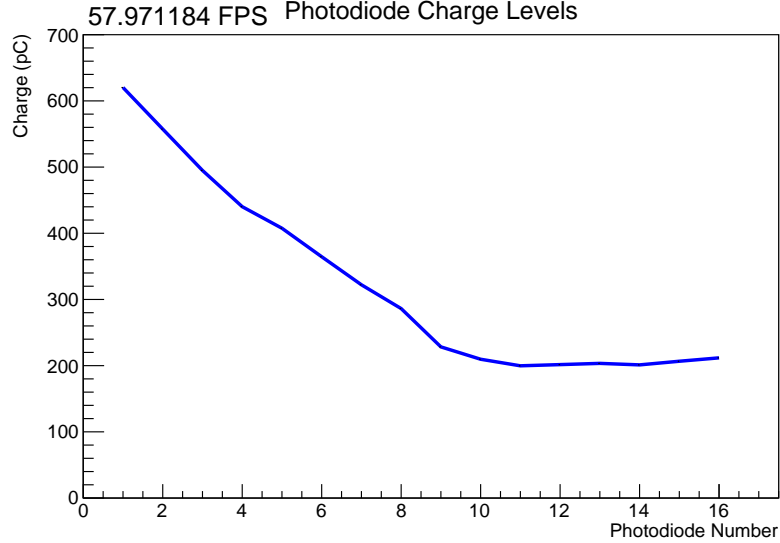
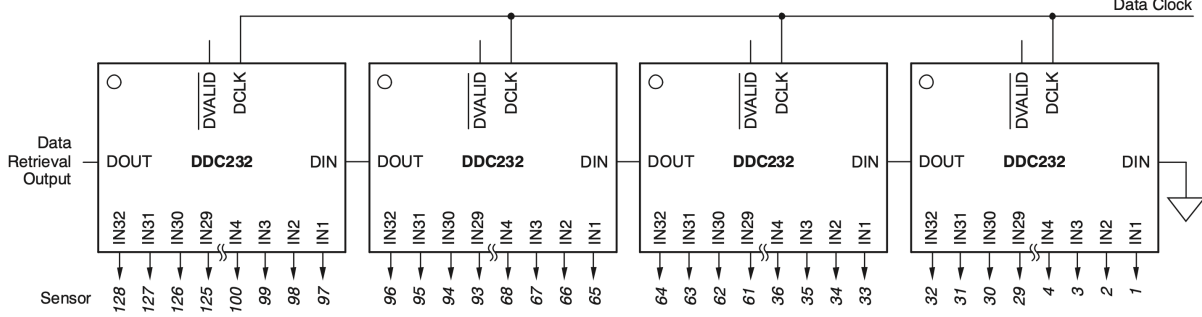


Figure 19: Live photodiode plot with 58 Hz refresh rate. The first few photodiodes are exposed to a torch.

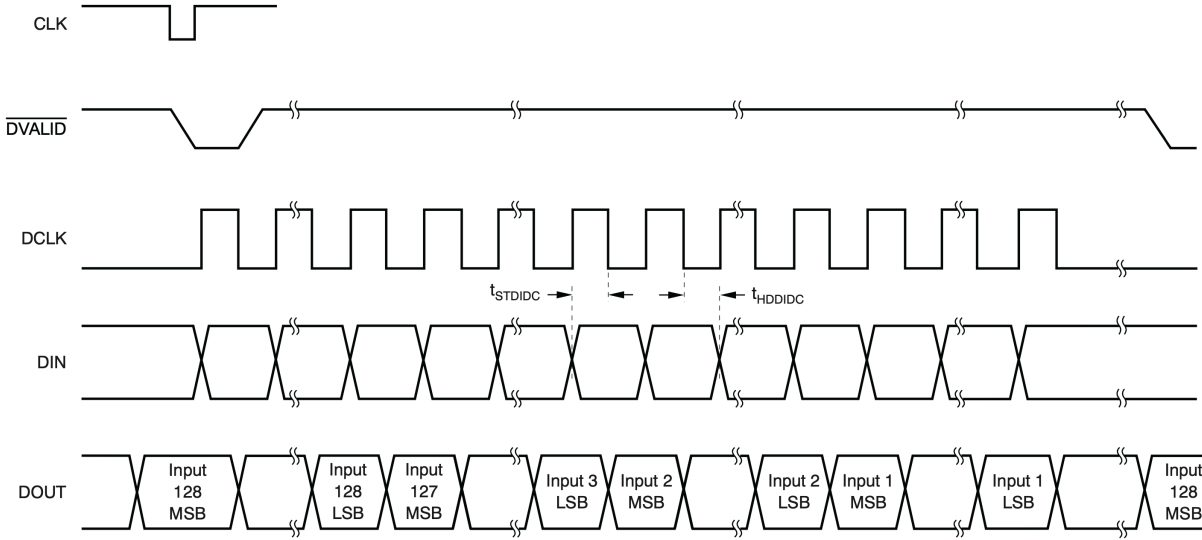
### 3.4 Next Steps

DDCs can be easily daisy-chained for applications that require more inputs. A full clinical-ready range detector would require 160 scintillator sheets (10 daisy-chained DDC boards) to give a WET of approximately 450 mm – though the detector can offer any multiple of 16 sheets. To daisy-chain DDCs, *CLK*, *CONV*, *DIN\_CFG*, *CLK\_CFG*, *RESET* and *DCLK* are sent to all boards as usual, however *DOUT* of boards in the chain are connected to *DIN* of the board next along the chain. The last board in the chain has *DIN* connected to ground and *DOUT* of the first board is connected to the FPGA as normal. *DVALID* is cascaded through OR logic gates on the circuit boards to indicate that all DDCs are ready to shifted data out to the FPGA. The daisy-chaining setup is summarised in Fig. 20. The custom circuit board in Fig. 9b is designed to allow daisy-chaining through the shown PMOD connections (pending modifications).

Adding more boards to a chain increases the number of data bits to be read out each cycle, which increases the integration time, recalling from Fig. 15 that data must be read out completely at least 10  $\mu$ s before the next *CONV* toggle. Using the method of data retrieval in Fig. 15, the shortest integration time with one DDC was calculated in equation 2 to be approximately 181  $\mu$ s. In order to daisy-chain 10 modules, the minimum integration time required is approximately 469  $\mu$ s. To increase the time available for shifting out data, one is able to read out data before *and* after *CONV* toggles as shown in Fig. 21, which gives the minimum integration time possible with 10 DDCs in equation 4.



(a) Basic principle of daisy-chaining DDCs. The board connected to the FPGA is on the left.



(b) Timing diagram for daisy-chaining DDCs. As data is shifted out of *DOUT*, data is shifted in from *DIN*.  $t_{STDIDC}$  and  $t_{HDDIDC}$  are the minimum times that *DIN* is valid before and after falling edges of *DCLK* and are equal to 10 ns.

Figure 20: Schematic and timing diagrams for daisy-chaining DDCs [39].

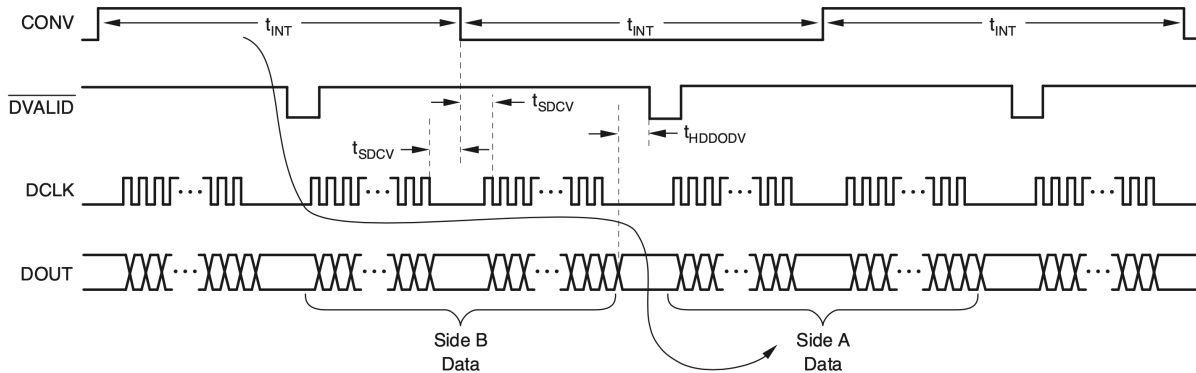


Figure 21: Timing diagram for data retrieval before and after *CONV* toggles [39]. This involves pausing *DCLK* for a total of at least  $2 \times t_{SDCV} = 20\mu s$  around the *CONV* toggle. *DCLK* must be stopped  $t_{HDDODV} = 400$  ns before the next  $\overline{DVALID}$  arrives, which is the time that *DOUT* is valid with data from the next measurement cycle.

$$t_{INT} = 2 \times t_{SDCV} + t_{HDDODV} + \frac{n_{bits}}{f_{DCLK}} = 2 \times 10\mu s + 400ns + \frac{32 \times 20 \times 10}{20MHz} \approx 341\mu s \quad (4)$$

Using equation 3 with  $(32 \times 20 \times 10) + 32 = 6432$  bits of data per measurement cycle gives a minimum time between measurements of approximately  $1420 \mu s$ , or a data rate of  $0.71 \text{ kHz}$ . The goal of the design is to achieve a data rate of at least  $1 \text{ kHz}$ . Here, the limiting factor is the speed of data transfer to the PC, since the integration rate is already at  $3 \text{ kHz}$ . While the most appropriate combination of integration time and dynamic range to avoid saturation with proton beams is currently unknown, the shortest possible integration time is chosen to be able to see fast changes in the light output of the scintillator. The dynamic range can always be reduced if the light output is too low. Therefore, it is planned that the UART interface be upgraded to a full USB 2.0 interface, which will require use of the Zybo's on-board ARM processor but could offer up to 480 times faster transfer speeds. Additionally, it is planned that data be transferred to a Raspberry Pi (Raspberry Pi Foundation, Cambridge, England) instead of a PC, for a compact solution which will host a web-page to allow live photodiode data to be viewed in any web browser at a refresh rate of  $50\text{Hz}$ . A PC-based version of the live web-based plot will be developed first.

## 4 Future Plans

### 4.1 Detector Characterisation and Simulation

There are currently 2 prototype DDC boards, which have been tested individually but not in daisy-chain mode. Once this has been tested and further prototype boards have been manufactured (to address any issues), the detector will be tested with a proton beam to evaluate performance with the new readout system. Photodiode data will be fitted to the QB model and further experiments will be designed to test the speed of measurement and determine the most useful way to acquire data for clinical applications (beyond a live plot). A long term goal will be to eventually deploy fitting routines either on the Raspberry Pi or the Zybo for fast online fit results, though the feasibility of this has not yet been investigated.

GEANT4 simulations exist of the scintillator stack detector setup [26], however improvements are required to accurately model the optical properties of the detector and to represent the geometry of the latest detector prototype. The existing simulation will be rebuilt from the ground-up as a learning exercise, to fix technical issues (e.g. to enable multi-threading support) and to implement these improvements.

### 4.2 Extending the Quenched Bragg Model

In order to improve the fitting of helium and carbon data, there are two areas to be addressed: the descriptions of light quenching and nuclear fragment interactions. The QB model uses Birks' law to describe scintillation quenching, however it is a semi-empirical model that fails under regions of high linear energy transfer (LET) [48]. The Bragg peak of helium and carbon are sharper than that of protons due to their increased LET, so a better description of quenching may be necessary to fit ion PDL data properly. Fortunately, a simple

extension of Birks’ law to second-order proposed by Chou [49] has been found to perform better under high-LET [50] and only introduces an additional proportionality constant,  $C$ , which is treated the same way as Birks’ constant,  $kB$ . Birks’ law to second order is given in equation 5 and has already been implemented into the QB model, but will be tested more thoroughly once reference curves have been obtained from HIT. The results of this analysis could form the basis of a future publication.

$$\frac{dL}{dz} = - \frac{S \cdot \frac{dE}{dz}}{1 + kB \cdot \frac{dE}{dz} + C \cdot \left(\frac{dE}{dz}\right)^2} \quad (5)$$

Addressing the coarse description of nuclear interactions in Bortfeld’s model requires shifting from Bortfeld’s analytical model to a numerical implementation of the depth-dose curves of ions developed by Krämer [51], which uses nuclear cross-section libraries to describe material-projectile nuclear interaction and is core to the treatment planning software at HIT. Implementing this framework is non-trivial, however it could be used to fit data for all ions used in clinical beams. Once implemented, quenching corrections will be applied using equation 5, which would be entirely novel and could also form the basis of another publication.

## 5 COVID-19 Statement

The COVID-19 restrictions that came into place at the end of March 2020 have left progress in this project largely unaffected. Since then, most of the work has been dedicated to FPGA design, which could be done while working from home. However, the project is rapidly approaching the stage where experimental data with a proton beam is required to further development and it is currently unclear how COVID-19 will affect the group’s ability to acquire beam time in the near future at a facility like UCLH, whose opening has been delayed, and HIT, which is blocked by travel restrictions.

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