# Electrical Tests of the ATLAS Phase-II Strip Tracker Upgrade

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**Abstract**

The High Luminosity Large Hadron Collider (HL-LHC) is the last planned upgrade of the LHC and it will increase the instantaneous luminosity by a factor of 10. To cope with the predicted high particle rates and the extreme radiation dosage, the ATLAS detector will require substantial modifications and in particular a new all-silicon inner tracking detector will be constructed. The thesis reviews the design of the new tracking detector and identifies the design choices that need to be made. It presents the digital design of the new ATLAS ABC130 readout chip which will be deployed in the new tracking detector and tests of the associated readout modules. Results on the electromagnetic compatibility of the readout modules are presented along with characterization and electrical modelling of the new ATLAS silicon strip sensors.

I, Samer Al-Kilani, confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

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**To my grandmother...**

# Acknowledgements

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# Contents

# 1 Introduction

The High-Luminosity Large Hardron Collider (HL-LHC) will begin collisions around 2024. The changes to the proton-proton collider will increase the average number of interactions per bunch crossings to upto five times the current value. This requires a new design for the current detectors to withstand the harsh conditions of the HL-LHC, such that they are able to exploit the new physics frontiers the HL-LHC might bring. One of the major changes to the new ATLAS detector, the so called ATLAS Upgrade, is the all-silicon inner detector. The new inner detector consists of a pixel and a strip detector. Both of these, will have new and improved sensor designs, readout electronics and powering schemes. This thesis will describe some of the designs and tests performed on prototypes of the new strip detector. The work presented in this thesis is a collaborative work of a large team of people. Here I will describe my personal contribution which are divided into three parts:

1. **Laser charge injection into strip sensors**:

   The operating conditions of the new ATLAS detector, particularly the high particle fluences, requires new designs of the strip sensors. A sensor is required that will perform well after long periods of irradiation and can withstand high charge doses. The latter can occur in the rare event of a beam loss when the beam becomes misaligned and hits the beam pipe or collimator resulting in a large flux of secondary particles hitting the detector

elements. This thesis will describe the investigation of injecting large charges into the new ATLAS strip sensor.

2. **Tests of the inner detector powering schemes**:

   The upgrade inner detector has two proposed low voltage powering schemes: the first uses DC-DC converters and the other uses Serial Powering to provide low voltage to the electronics. Introducing converters or control boards to the readout module can have implications on the general performance of the electronics, notably the noise. The powering boards can either influence the noise internally via the power supply rails or could be an external influence via the electromagnetic (EM) emissions. Both have been investigated in this thesis with particular emphasis on the EM emissions. The EM compatibility tests have been exclusively performed on the DC-DC converters, since the coils in the converters are a source of EM emissions. The readout module susceptibility to EM fields have been tested and the use of shields and novel coil designs to minimize or fully attenuate the emissions have also been investigated.

3. **Digital design of the ABC130 (strip readout chip)**:

   The high number of proton-proton interactions expected at the HL-LHC and the more stringent physics requirements necessitates an improved and new triggering system for the ATLAS detector. New readout chips are required to facilitate the new trigger requirements. This thesis outlines the digital design of the new ABC130 chip with emphasis on the design of the digital compression logic of the chip for which I was responsible.

# 2 The LHC and its experiments

The Large Hadron Collider (LHC) is a two ring hadron accelerator installed in a 26.7 km circular tunnel that sits between the Jura mountains in France and Lake Geneva in Switzerland. The tunnel was originally constructed in the late 1980s for the Large Electron Positron (LEP) accelerator. The tunnel has 8 straight sections and 8 curved sections and lies at a depth between 45 m and 170 m underground. As a proton-proton collider, the LHC was designed for a centre-of-mass energy of 14 TeV which is achieved from a 450 GeV beam injected from the Super Proton Synchrotron (SPS). Unlike the particle-antiparticle colliders, the LHC must have two separate rings for the counter rotating beams. Due to the lack of space in the LEP tunnel, the LHC had to use the two-in-one superconducting magnet design[1]. The LHC relies on the superconducting dipoles to steer the beams and keep them on the required trajectory. The magnetic field of the dipoles are generated by passing 12 kA through niobium-titanium cables which become superconductive at 10 K. The use of super-fluid helium, as a coolant, brings the temperature of the magnets further down to 1.9 K. The 1232 dipole magnets make up to 80% of the LHC circumference. The 392 quadrupole magnets on the other hand, are used to focus the beams just before the interaction points in order to maximise the rate of collisions.

For the other sections, as shown in Figure 2.1, one straight section is used for the Radio Frequency (RF) cavities, one for the beam dump, two for cleaning the beam halo[1] and the other four

[1] Stray particles travelling alongside the beam

are used by the detectors as interaction points. The LHC depends on (RF) cavities to increase the energy of the two beams, only 16 RF cavities in total are used, eight for each beam. At the other sections, the LHC uses superconducting magnets to steer and focus the beam.

For a particle collider to achieve precision measurements of interesting physics events (events with a cross section in the order of pico-barn, such as the Higgs production), the collider must operate with a high luminosity. The luminosity determines the number of events per second for a certain process and is given as

$$L = \frac{N_1 N_2 k f}{4\pi\sigma}$$

where $N_1$ and $N_2$ are the number of particle per bunch for every beam, $k$ is the number of bunches per beam and $\sigma$ is the effective cross-sectional area of the beam. By using 2808 bunches of $10^{11}$ protons with a 25 ns spacing, the LHC can achieve an instantaneous peak luminosity of $10^{34}$ $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The number of events per second for an interaction with a cross section $\sigma_I$ is $L\sigma_I$.

At four of the eight interaction points there are four different experiments. At the new Point 1 and 5, sit ATLAS and CMS, respectively. While ALICE and LHCb are at Point 2 and Point 8, respectively, which were previously used by the LEP experiments.

Both ATLAS and CMS are multi-purpose detectors designed to exploit the full potential of the LHC. Both experiments offer diverse physics programmes such as the search for supersymmetry, extra dimensions in space and evidence of dark matter but they have a strong emphasis on electroweak symmetry breaking with a specific focus on the Higgs Boson. The two experiments complement each other where each can be used to validate the results of the other.

LHCb uses proton-proton collisions to focus on researching the CP (Charge Parity) violation. It can be used to study the rare decay of B flavoured hadrons that can help understand the asymmetry between matter and antimatter and to understand why only mostly matter can be observed in our universe.

One month a year heavy lead ions (lead nuclei) are accelerated. ALICE uses this beam that provides an extreme energy density which can be used to study the properties of strongly interacting matter. This includes the possibility of creating a phase of matter known as the quark gluon plasma. The plasma can be studied to understand the phenomena of quark-confinement. ATLAS and CMS also take advantage of the ion beam and study the full range of observables which characterize the hot and dense collisions of the heavy lead ions.

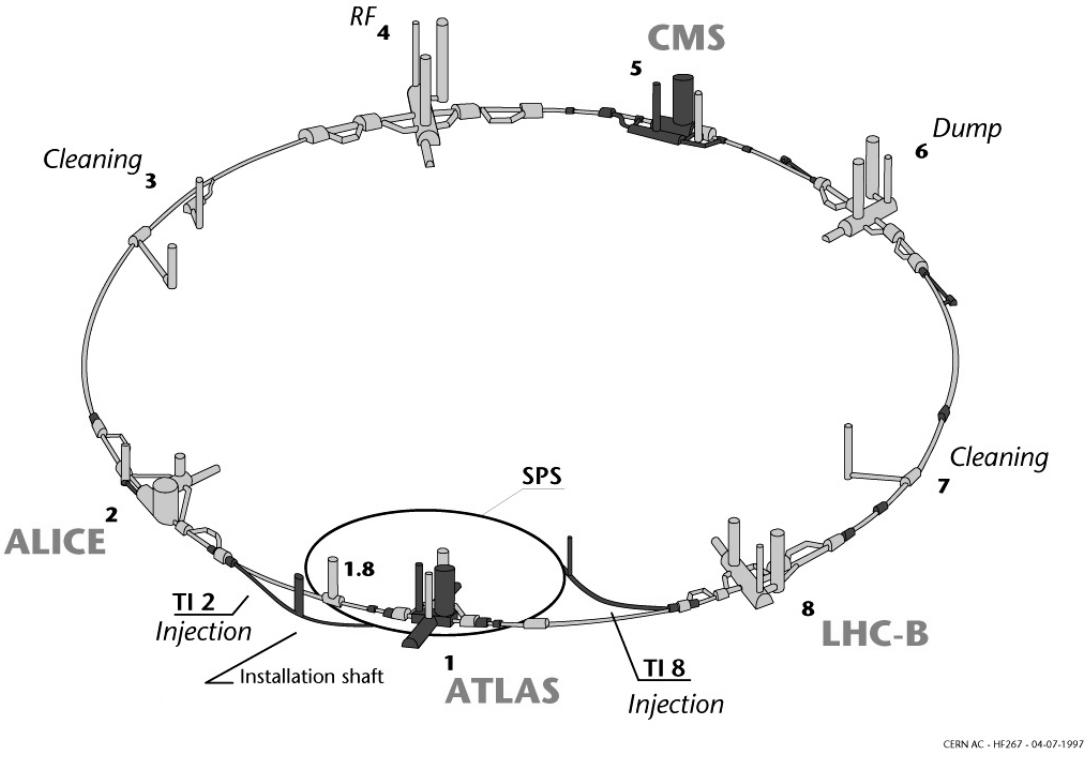



Figure 2.1: The LHC layout[2].

# 3 The ATLAS detector

ATLAS (A Toroidal LHC Apparatus) is a particle physics detector designed to take full advantage of the physics potential of the LHC. It is a multi-purpose detector designed to primarily probe proton-proton collisions. ATLAS is designed to make precision measurements in an environment of high interaction rates and radiation doses. The design is highly granular to cope with the high particle fluxes arising from multiple interactions and overlapping events.
While providing a large pseudorapidity[1] acceptance and an almost full azimuthal angle coverage, ATLAS has been designed to achieve the following requirements:

- High efficiency in track reconstruction which provides good charged particle momentum resolution.
- Electromagnetic calorimetry to provide electron and photon identification, energy measurements and missing transverse energy measurements.
- Hadronic calorimetry to provide accurate jet and missing transverse energy measurements.
- Good muon identification and momentum measurements for high $P_T$ muons.
- Efficient triggering with a low $P_T$ threshold.
- High resolution at the inner tracker to allow precise measurement of the impact parameter.

[1] See section 3.2

## 3.1 Physics goals

The ATLAS detector's design was mostly driven by the search of the Standard Model Higgs boson and other possible extensions at the TeV scale. The discovery of the Higgs boson in 2012 [3, 4] with a mass of 125.5 ± 0.2 GeV/$c^2$[5] vindicated the design. The challenge now is to measure the properties of the Higgs boson as precisely as possible. Particularly, to provide precise measurement of its mass, width and decay branching fractions, in a variety of channels ($ZZ, \gamma\gamma, WW, b\bar{b}, \tau^+\tau^-$).

The detector must be able to identify and measure many decay modes. For instance, in the $h \to \gamma\gamma$ case the photons are identified by having high energy deposits in the calorimeter without a preceding track. A constraint on the mass comes from the origin of the two photons and so it is important to know from which primary vertex the photons originated from, which requires high granularity tracking.

In addition, the detector must be able to search for physics beyond the Standard Model. The Standard Model is very successful in describing most of nature's particles and forces with great precision. However, it doesn't explain aspects of physics such as the matter-antimatter asymmetry of the universe, dark matter and gravity. A detector is therefore required that has the broadest sensitivity to the many possible extensions of the Standard Model.

## 3.2 The structure of the detector

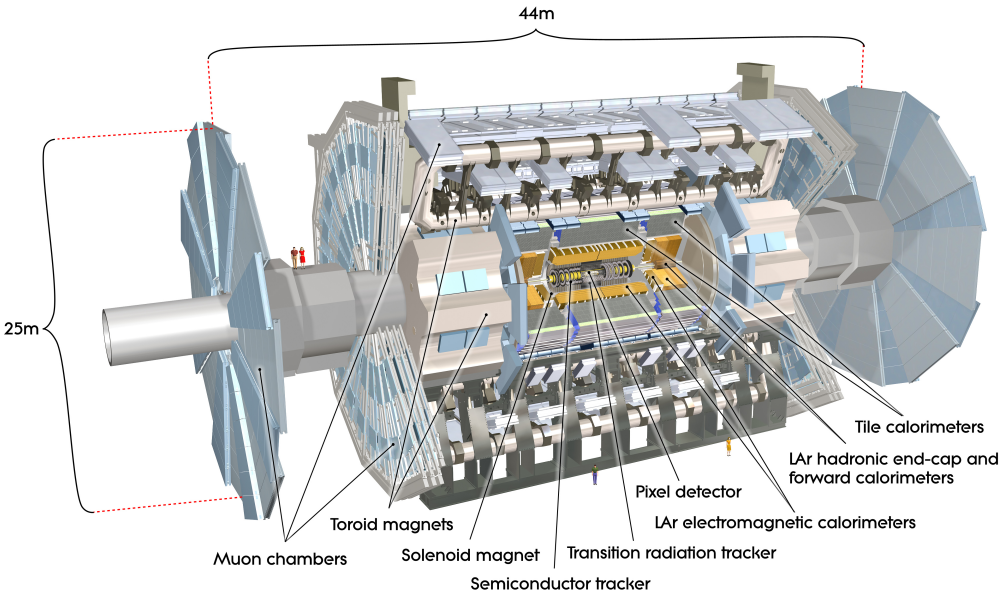



Figure 3.1: A schematic of the ATLAS detector[7].

Standing at 44 m long with a height of 25 m, the ATLAS detector is the largest particle detector at CERN. It is situated near the CERN main campus and is placed in a cavern 93 m underground. The ATLAS detector uses special cylindrical coordinate system with the notations $(r, \phi, \theta)$. The Interaction Point (IP) is the origin of this coordinate system, $r$ is the transverse radius from the beam pipe, $\phi$ is the rotational angle in the transverse plane and $\theta$ is the polar angle with respect to beam axis. The pseudo-rapidity $\eta$ is defined as:

$$\eta = -\ln\left(\tan\left(\frac{\theta}{2}\right)\right). \tag{3.1}$$

Pseudorapidity differences are invariant under boosts along the beam axis. This is particularly of importance with hadron collisions, as it is often the case that one of the colliding quarks or

gluons may have a lot more momentum than the other, so the particles produced come out near one end of the detector. When the detected particles are plotted against $\eta$ , they are effectively shifted to the center of the collision, where the particles come out symmetrically distributed, thus simplifying the analysis.

The ATLAS detector covers the region $|\eta| < 4.9$[6]. It is made of a central region "barrel" (concentric cylinders surround the beam line) and the region on the sides "end-caps" (disks on the two ends of the barrel). Within these regions, there are 4 sub-detectors. From the IP outwards, there is the inner detector (comprising three different layers Pixel, Semiconductor tracker (SCT), Transition radiation tracker (TRT)), the electromagnetic calorimeter, the hadronic calorimeter and finally the muon spectrometer. This can be seen in Figure 3.1.

## 3.3 Inner detector

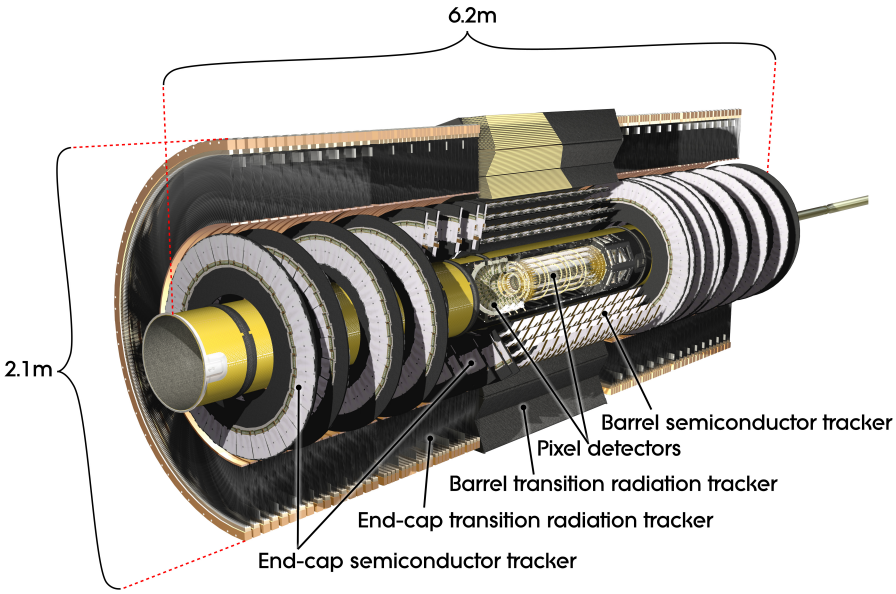



Figure 3.2: A schematic of the ATLAS inner detector[7].

The Inner Detector (ID) is designed to track the trajectories of charged particles originating from the IP. Particles are measured as individual hits then the hits are connected together with a helical function to reconstruct the tracks; as most interesting particles leave the magnetic field of the ID after being slightly bent. Thus, tracks are just helix segments. The ID is designed to provide high granularity tracking information and excellent measurement of momenta over a wide range and coverage of $|\eta| \leq 2.5$[8]. All of which must withstand and operate in environment with high radiation and high magnetic fields.

The ID has a cylindrical shape with a length of 6.2 m and a radius of 2.1 m. It is also made of three different layers with different particle detection technologies. From the IP outwards, there is the Pixel detector, then the Semiconductor Tracker (SCT) and lastly the Transition Radiation Tracker (TRT). This ensures very high resolution tracking at the inner radii and continuous tracking at the outer radii. On average, the trajectory of a charged particle is reconstructed from 37 hits, three in the Pixel detector, four in the SCT and 30 in the TRT.

The entire ID is also immersed in a magnetic field generated by a superconducting solenoid magnet. The magnet produces 2 T but the field intensity varies along the beam line within the ID. This magnetic field facilitates the measurement of the particles' momenta, by measuring the curvature of the charged particles as they travel through the magnetic field within the ID.

Another crucial aspect of the ID is the mechanical design, which affects the coverage and the rigidity of the detector. In the latter, there was a compromise between the rigidity of the detector and the material budget, a minimization of material is always favoured but not at the price of rigidity. To achieve the $|\eta| \leq 2.5$ coverage the detector was designed with a barrel and an end-cap region. In the barrel region, the sensors are arranged in concentric cylinders around the beam line. While in the end-cap, the detectors are arranged as disks perpendicular to the beam line. The different layers of the inner detector can be seen in Figures 3.2 and 3.3.

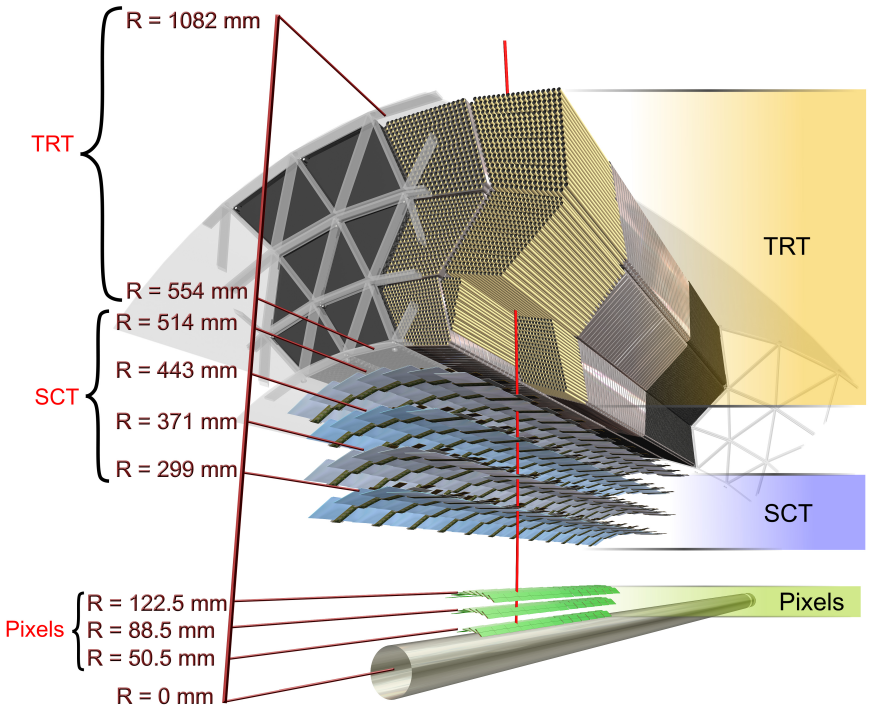



Figure 3.3: A schematic of the ATLAS inner detector (barrel region)[60].

### 3.3.1 Pixel detector

The pixel detector, as the innermost layer, is subject to a very high density of particles and radiation damage. This requires it to have the highest granularity of all the detectors. The use of pixels as opposed to silicon strips as in the SCT, improves the resolution and removes the ambiguity of the hit position. Each active device, shown in Figure 3.4 and known as module, is 6.3 cm $\times$ 2 cm with 46,080 pixels. The pitch around the beamline is 50 µm and 400 µm along the beam line. Each module requires 16 readout chips servicing 2,880 readout channels. The pixel

layer has a total of 1744 modules serviced by more than 80 million readout channels, which is dominating most of the ATLAS readout channels. The pixel detector measures the amount of charge deposited in a single pixel by recording the Time Over Threshold (TOT). By looking at the charge distribution over adjacent pixels the hit position can be determined.

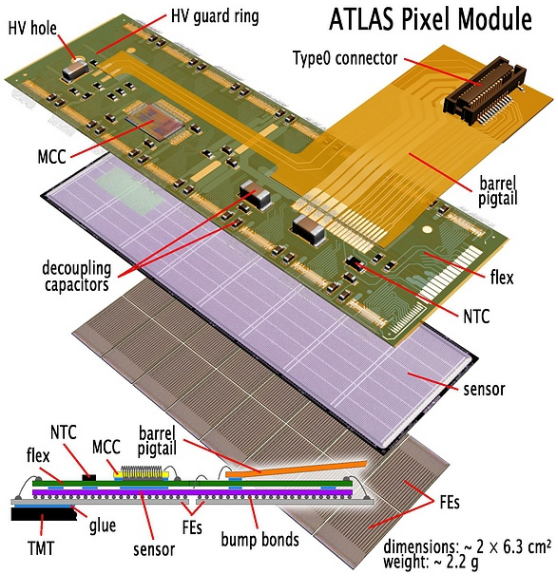



Figure 3.4: The layers of the pixel barrel module[60].

The pixel detector is designed to have a coverage of $|\eta| < 1.7$ at the barrel region and $1.7 < |\eta| < 2.5$ at the end-cap. This is achieved by having three cylindrical sub-layers placed at 50.5 mm, 88.5 mm and 122.5 mm away from the beam line. While the end-cap has six disks, three on either sides of the IP at distances 49.5 cm, 58.0 cm and 65.0 cm[9] from the IP. Both the barrel and end-cap modules are identical to each other. The pixel detector layer arrangement can be seen in Figure 3.5.

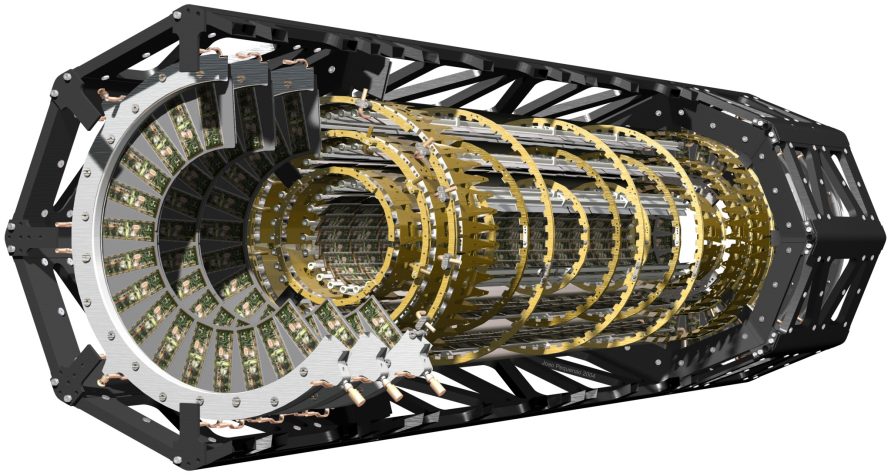


Figure 3.5: 3D model of the pixel detector consisting of barrel and end-cap layers[60].

### 3.3.2 Semiconductor tracker (SCT)

Surrounding the pixel detector is the second layer of the ID, the SCT. With four layers at the barrel region, two in the forward region and two end-caps each with nine disks. The SCT covers the range $|\eta| < 2.5$, it uses 62 $m^2$ of silicon sensors. These micro-strip sensors have a mean pitch of 80 μm and are 6.4 cm in length. Each two sensors are wire-bonded together to have an effective length of 12.8 cm. The modules consist of two wire-bonded sensors glued back to back with a stereo angle of 40 mrad, as shown in Figure 3.6. Without such alignment, the modules would only allow the measurement of two coordinates $r$ and $\phi$, however the stereo angle adds another spatial measurement determining the trajectory of the particles in the $z$ direction. The readout electronics for each module is mounted on a hybrid. The electronics mainly consists of a front-end amplifier, discriminator, followed by binary pipelines which holds the data until a trigger signal is received. Each module with a 6.36 cm wide sensor, has 1,536 readout channels. With 4,088 SCT modules this results in excess of 6.2 million readout channels for the SCT detector.

Unlike the pixel detector, the SCT has different modules for the end-caps and the barrel region. They both have the same electronics but the sensors themselves are different. While the barrel modules are rectangular, the end-cap modules are trapezoidal and are built with radial strips of constant azimuth. The operation of strip silicon sensors are thoroughly explained in Chapter 5 and the readout chip operation is explained in Chapter 10.

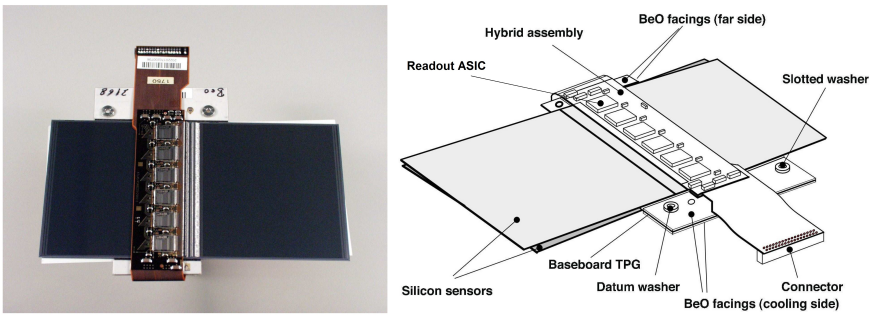



Figure 3.6: The SCT barrel module consisting of a hybrid with 12 readout chips (6 on each side) wire-bonded to two silicon strip sensors glued back to back with a 40 mrad stereo angle[9].

In the barrel region, 2,112 modules are mounted on four layers, each row is associated with 12 modules. To maintain the hermetic nature of the detector, the modules are overlapped with an air gap of around 1 mm, this insures isolation between the high voltage supplies. The four concentric layers have a radii of 29.9 cm, 37.1 cm, 44.3 cm and 51.4 cm[9].

As for the forward region, the 18 end-cap disks use 1976 trapezoidal modules, with three rings per disk. The number of modules per disk is 52, 40, 40 for outer,middle and inner rings, respectively. Not all disks use all three rings, for instance the first disk only uses the outer and middle rings. Thus the total number of modules per end-cap is 988. As in the barrel region, the end-cap modules are also overlapped. This is done by placing the outer and inner rings on one side of the disk and the middle ring modules on the other side.

The spatial accuracy for both module types is 17 μm in the $r - \phi$ and 580 μm in the radial direction for the end-caps modules and 580 μm in the $z$ direction for the barrel modules.

### 3.3.3 Transition radiation tracker (TRT)

The outermost layer of the inner detector, the TRT, consists of 372,032 straws. Each straw is between 40 − 150 cm long (depending on its location), 4 mm in diameter and contains a 31 μm gold-plated tungsten anode wire and has a 35 μm aluminium coated wall which acts as a cathode. The straw itself is filled with Xenon gas and when a particle crosses the straw, which is set to a high negative voltage, the particle ionizes the gas and the electrons start to drift toward the wire. This drift forms an avalanche that produces a high electric field. By splitting the wire into two parts, the electron drift time can be measured from both ends and the particle hit position can be determined with an accuracy of ~140 μm. This yields a total of ~420,000 readout channels, since not all straws have a split wire. The Xenon, allows the detection of transition radiation, hence the name TRT. The transition radiation is the emission of X-rays when charged particles cross the boundary between two different dielectric materials. In the case of the TRT, the straws are embedded in a polypropylene/polyethylene fibre radiator. The Xenon also allows the use of a double threshold which helps with the electron identification. The lower threshold helps detect the hits in the gas mixtures itself and the higher threshold helps detect the X-rays generated by the particles momentum from the transition radiation.

In the barrel region, the TRT has three concentric cylindrical layers with a triangular substructure. The barrel modules have between 329 and 793 straws. Each row of the barrel has 12 modules covering the radial range from 64 cm to 103 cm. In total, there are 52,544 straws in the barrel region all aligned parallel to the beam line. The remaining 319,488 straws make up the 36 disks in the end-cap. 18 disks per end-cap distributed to three wheels each with different

number of disks. Both barrel and end-cap regions provide a spatial resolution of 130 μm in the $r - \phi$ plane.

## 3.4 Calorimeters

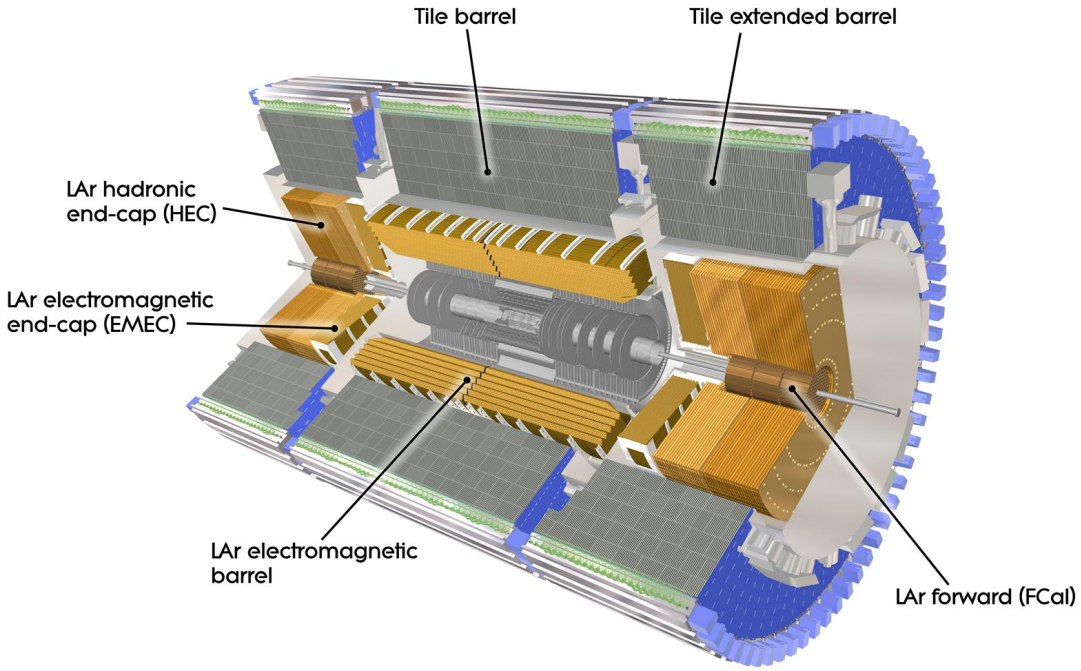



Figure 3.7: A schematic of the ATLAS calorimeters[7].

Calorimeters absorb and measure the energies of charged and neutral particles. Calorimeters are usually composed of absorbing high density layers (such as Lead) interleaved with active layers (such as liquid-argon). Electromagnetic calorimeters measure the absorbed energy as particles lose energy when they interact with charged particles in matter, while the Hadronic calorimeter sample the energy of hadrons as they interact with the atomic nuclei. The energy

measurement is usually localised which means the position of the particle can also be measured. They are also responsible for measuring the direction of the jets and the missing transverse momentum. By studying the shower profile, particle identification becomes possible and can also be involved in the event selection.

ATLAS has two types of calorimeters, the liquid-Argon Electromagnetic (EM) calorimeter and the hadronic calorimeter. The EM calorimeter surrounds the inner detector in the barrel region and is responsible for identifying and measuring the energies of electrons and photons. The hadronic calorimeter surrounds the EM calorimeter and is used to measure the energies of both charged and neutral hadrons. The hadronic calorimeter has a coarser granularity which is acceptable for jet reconstruction. Both calorimeters also have end-caps in the forward regions. The ATLAS calorimeters are shown in Figure 3.7.

### 3.4.1 Electromagnetic (EM) calorimeter

The EM calorimeter is a sampling calorimeter. It uses interleaved Lead and liquid-Argon in a radial accordion geometry where the Lead acts as an absorber and the liquid-Argon as the sampling material. The EM calorimeter has one barrel and two end-caps covering the pseudo-rapidity region $|\eta| < 3.2$[10] and has ~170,000 readout channels. The barrel is split into two identical halves separated by a gap of 6 mm at $z = 0$ and is also segmented into three longitudinal sections. The total thickness of the EM calorimeter in the barrel region is $24X_0$[2] and $26X_0$ in the end-caps (The radiation length of the inner detector is about $2.8X_0$). Thus, electromagnetic showers may start to appear in the inner detector and hence a ‘pre-sampler‘ segment is required in the barrel region to allow energy measurement corrections.

[2] $X_0$ is the radiation length. It is a characteristic of the material and relates to the amount of energy lost in the material (mostly due to electromagnetic interaction), as high-energy particles travel through it.

### 3.4.2 Hadronic calorimeter

The layer surrounding the EM calorimeter is the hadronic calorimeter. The hadronic calorimeter has two components giving coverage in the region $|\eta| < 4.9$[11]. The first are tiles of steel interleaved with scintillators and the second is the liquid-Argon sampling calorimeter similar to the one used in the EM calorimeter. The thickness of the hadronic calorimeter corresponds to $11\lambda$[3] which is enough to minimise the punch-through[4] to the Muon Spectrometer. The tile calorimeter forms the central and two extended barrels while the liquid-Argon forms the end-caps and forward sections, providing better radiation tolerance. This feature is particularly beneficial for the Forward calorimeter as it experiences the highest amounts of radiation and it acts as a good radiation barrier for the muon spectrometer.

## 3.5 Muon spectrometer

The spectrometer measures the deflection of muon tracks in large air-core toroidal magnets. The muon spectrometer is designed to offer triggering information and momentum measurements at a wide range of pseudorapidity and azimuth angles. The muon spectrometer is the largest component in the ATLAS detector. The measurements are achieved using the muon chambers that are placed between the eight superconducting toroidal magnets. The muon chambers all have the same underlying principal of having drift tubes with a thin wire held at high voltages in a tube filled with a gas mixture. When a particle crosses the tube the gas is ionized and an electric current is produced. The Monitored Drift Tubes (MDT) cover the range $|\eta| < 1.05$ and are used in both the barrel and end-caps and consist of 30 mm Aluminium tubes with a thin central

[3] $\lambda$ is the nuclear interaction length and it is the mean path length required to reduce the numbers of relativistic charged particles by the factor $1/e$, as they travel through the material. $X_0$ is not used here as the presence of the stronger hadronic interaction is dominant.

[4] When stray particles are not absorbed at the calorimeters and reach the muon spectrometer.

wire. The spatial resolution is around 80 μm. Within every MDT barrel layer a Resistive Plate Chamber (RPC) is placed. This chamber employs two plates with a gas filling the gap providing a spatial resolution of 10 mm. The Cathode Strip Chambers (CSC) are multi-wire proportional chambers that are placed in the innermost end-cap ring, closest to the beam pipe covering the region $2 < |\eta| < 2.7$. The CSC provides two coordinates, one read out from the cathode strips with a spatial resolution of 60 μm and the other through the anode wires (orthogonal to the cathode strips) with a resolution of 5 mm. Finally, the trigger signal is provided by the Thin Gap Chambers (TGC) along with a second coordinate measurement in the end-cap region. The TGCs are very similar to the CSC but have a faster drift velocity. The TGC resolution is about 2 mm to 7 mm and cover the range $1 < |\eta| < 2.7$[12].

## 3.6 Triggering

### 3.6.1 Requirement

Due to the large number of bunch crossings and the fact that only a small number of events contain interesting physics, a triggering system is required to select and permanently store the events of interest. The triggering system faces the following challenges:

- The bunch crossing rate of 25 ns is a very short time to make a decision on whether to keep or discard the event. It takes longer than 25 ns for a particle travelling at the speed of light to go through the entire detector.
- The ~25 interaction pile-up[5] (for a $10^{34}$ cm$^{-2}$ s$^{-1}$ peak luminosity[13]) increases the volume and complicates the task.
- Only 100 interactions can be recorded from the 1 billion interactions every second (25 interactions × 40 million bunch crossings every second at a luminosity of $10^{34}$ cm$^{-2}$ s$^{-1}$).

[5] For a given collider luminosity, the mean number of interactions per bunch crossing is called “pile-up”

### 3.6.2 System design

The ATLAS trigger is a three level triggering system, where each level refines the decisions made by the previous one, as shown in Figure 3.8. The triggering system must have a high rejection rate to reduce the 40 million events per second to only 100 events per second while maintaining high efficiency as not to compromise rare physics events.

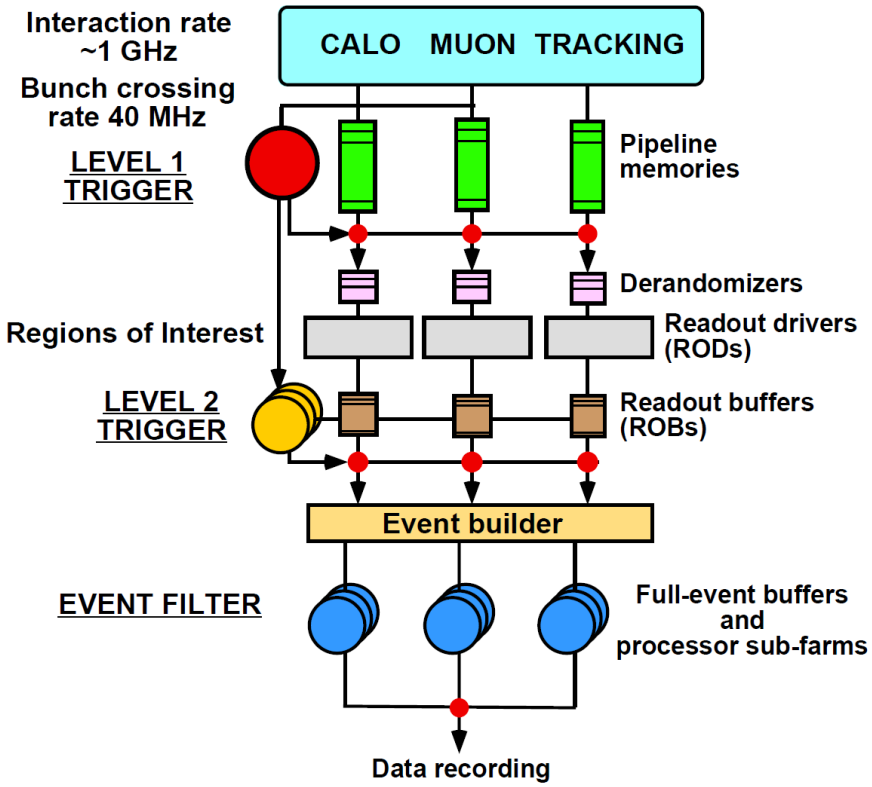



Figure 3.8: A block diagram showing the three levels comprising the ATLAS trigger system [14].

The data flow of the triggering system is as follows.

The main input for the triggering system comes from the calorimeters and muon spectrometer. The Level-I trigger processes this information to identify particles with high transverse momen-

tum ($P_T$), and/or large missing transverse momentum ($E_T^{miss}$) and filters the data accordingly. The Level-I trigger then moves the selected events to Read Out Buffers (ROB) at a rate < 100 kHz. The data is kept at the ROBs until a decision is made by the Level-II trigger. The Level-II trigger, which uses Region-of-Interest (RoI) information to make its decision, moves the data from the ROB to the full event buffer. This process is known as Event Building, because the event data are fragmented at the ROBs and they are joined up together for the Event Filter. At this level, the data rate is reduced to 1 kHz. The Event Filter will finally perform offline code algorithms and further filter the events taking the rate down to 200 - 400 Hz.

### Level-I triggering system

The Level-I trigger decision relies on the input from the calorimeters and muon spectrometer. The muon spectrometer is used to identify high $P_T$ muons and the calorimeters can identify high $P_T$ electrons, photons, jets and taus decaying into hadrons. The physical size of the muon spectrometer alone implies a time-of-flight interval longer than the 25 ns bunch crossing interval. Also, the pulse shape of the calorimeter signal can extend over a number of bunch crossings. Due to these factors among others, the pipelines were designed to hold a hundered bunch crossing giving the readout electronics a latency of 2.5 μs. The data flow of the Level-I trigger is illustrated in Figure 3.9.

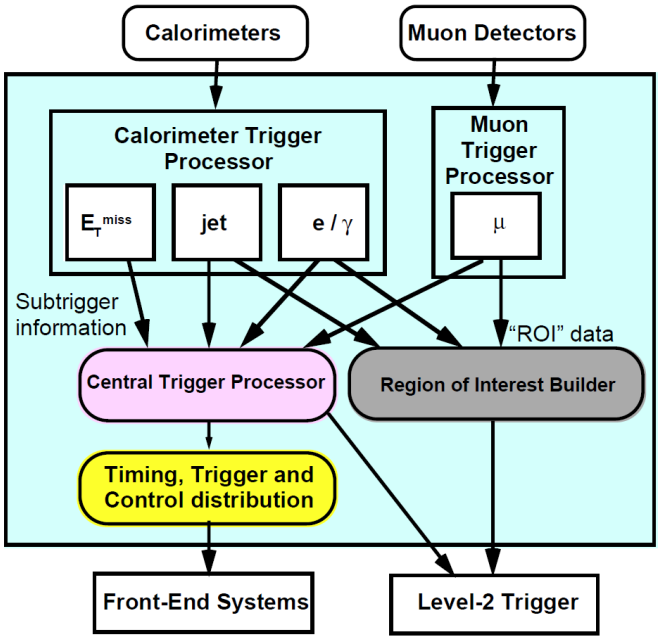



Figure 3.9: The Level-I trigger block diagram[14].

The Level-I trigger also prepares RoI data to help with the selection process at the Level-II trigger. The RoI data includes locations of candidate muons, electrons, photons, jets and hadrons.

### High level triggering system

The Level-II trigger and the Event filter define the high level trigger. Both of which are built using PC farms, the Level-II trigger provides a high rejection with limited algorithms and modest computing power. While the Event filter requires extensive computing power with high precision algorithms for a further rejection. As opposed to the fixed latency of the Level-I trigger, the latency of the Level-II trigger is variable and it ranges between 1 ms and 10 ms. The Level-II trigger employs optimized trigger selection algorithms that processes only a fraction of the event

data, typically ∼2%. The RoI supplied by the Level-I trigger is the input for these algorithms. This enables the Level-II trigger to request only data from the ROBs holding the interesting features. In addition, the use of the RoI reduces the volume of data to be moved to and analysed in the Level-II trigger system. The Level-II trigger uses many processors from the farm to process the data and can treat several events concurrently.

For the selected events from the Level-II trigger, the event builder creates full events from the fragmented events held at the ROBs. The Event filter receives the selected full events and uses a single processor to implement complicated selection algorithms, which can take upto one second to complete.

# 4 ATLAS Phase-II Upgrade

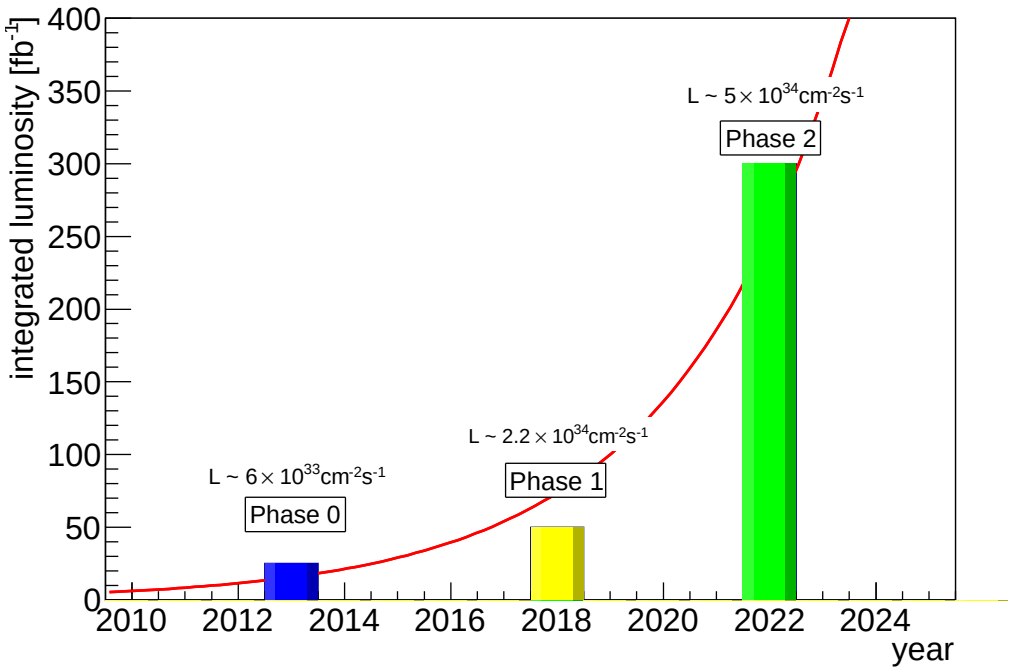



Figure 4.1: The luminosity upgrade plans at the LHC.

The physics reach of the LHC is expected to saturate within eight years of operation as the statistical error decreases as the square-root of the running time. In order to maximise the physics potential of the LHC, it will be upgraded to the High Luminosity LHC (HL-LHC). This provides the same reach in 5 years as would be obtained from a further 30 years of running the LHC with-

out an upgrade. A series of upgrades are foreseen for the Large Hadron Collider with the aim to maximise the physics accessible with a total integrated luminosity of 3000 $fb^{-1}$. Following the first LHC upgrade (Phase-0), the LHC is expected to deliver a total integrated luminosity of 100 $fb^{-1}$ over 2-3 years. At which point, the second upgrade will commence (Phase-I) allowing an operation with an instantaneous luminosity of $2.2 \times 10^{34}$ $cm^{-2}\,s^{-1}$ and delivering 300 $fb^{-1}$ of integrated luminosity over a course of another three years. This chapter will describe the final stop of this series of upgrades (Phase-II).

The Phase-II upgrade will mark the start of the HL-LHC which will deliver 2500 $fb^{-1}$ of integrated luminosity over its lifetime (~10 years). The large data collected at the HL-LHC will significantly improve the precision measurements of rare processes. It will also expose the detectors to large particle fluences which will increase the detectors occupancy and radiation damage. The HL-LHC will increase the instantaneous luminosity by a factor of five with "luminosity levelling" and the integrated luminosity by a factor of 10. The instantaneous luminosity of $5 \times 10^{34}$ $cm^{-2}\,s^{-1}$ at the HL-LHC is expected to have ~140 particle interactions per bunch crossing (assuming a bunch crossing rate of 25 ns), a large increase from the Phase-I ~55 interactions per bunch crossing. This increase and the fact that most of the detector's electronics will be at the end of their 15-20 years lifetime, means a new detector design is needed. The proposed design of the ATLAS detector assumes 200 interactions per bunch crossing and an integrated luminosity of 2500 $fb^{-1}$ over 10 years.

One of the major design changes in the new detector is the inner tracker. With the current inner tracker, the high particle fluences of the HL-LHC are expected to cause bandwidth saturation and high radiation damage at the Pixel and SCT layers and very high occupancies at the SCT and TRT (100% occupancy for the TRT). These factors have resulted in an all-silicon inner detector design. Other changes to the detector design include using lighter carbon fibre for the support structure to minimize the material within the detector. Front-end readout chips are being

redesigned using new radiation hard ASIC technologies that will provide functionalities that are essential to the new triggering system that will be described in Section 4.2.

## 4.1 Physics motivation

With the recent discovery of the Higgs boson [3, 4], high energy physics enters a new era of investigations into the standard model. In addition, there is a hope that new physics beyond the standard model will fall within the reach of the LHC. As well as measuring the mass of the Higgs boson, recent studies have also started to investigate the detailed properties, including spin and parity of the new particle [15] and the strength of its coupling to fermions and bosons. The large samples of data that will be collected over the next few years will increase the sensitivity of these measurements to physics beyond the standard model.

Models like supersymmetry predict deviations in the Higgs couplings that can be large. The HL-LHC will be able to measure the couplings more precisely and in parallel can look for heavier particles. These processes include:

**Already established processes:**

- $H \rightarrow \gamma\gamma$ [16]
- $H \rightarrow ZZ^* \rightarrow 4\ell$ [17]
- $H \rightarrow WW^* \rightarrow \ell\nu\ell\nu$ [18]
- $H \rightarrow \tau^+\tau^-$ [19]

**New rare decays:**

- $H \rightarrow b\bar{b}$: An abundant decay, however at the HL-LHC more of the decays associated with the Higgs boson will be produced and they can be isolated with b-tagging, which requires a high precision tracker.
- $H \rightarrow \mu\mu$: Very low signal to noise ratio at the LHC but expected signal significance is

larger than $6\sigma$ with 3000 $fb^{-1}$ at the HL-LHC. A high performance tracker is also required to isolate the signal created from this decay.

## 4.2 Triggering

The design of the triggering system is motivated by the future physics goals of the ATLAS experiment. It is expected to have the flexibility that can maintain the low transverse momentum threshold for isolated electrons and muons at around 20 GeV, which can maximize physics acceptance for rare processes.

Evolving from the current triggering system, the upgraded triggering system has a split Level-0/Level-1 hardware trigger. The overall rate for the Level-0/Level-1 trigger is 200 kHz with a latency of 20 μs. The triggering levels have the following requirements:

**Level-0**

- Same functionality as Phase-I Level-1 trigger.
- Acceptance rate of > 500 kHz.
- Latency < 6 μs.
- Decision based on calorimeter input and Phase-I Level-1 muon trigger.

**Level-1**

- Acceptance rate of < 200 kHz.
- Latency < 30 μs.
- The acceptance decision is made on the information supplied by the Region of Interest (RoI), the full calorimeter granularity within the RoI and the refined muon selection using the Muon Drift Tube chamber (MDT).
- The Level-1 trigger should provide parameters for tracks within the RoIs found at Level-0.

**Level-2**

- 5-10 kHz using offline algorithms.

### 4.2.1 Trigger rates

Most constraints on the L1 triggering rates come from the hardware limitations. The majority of the detector's front-end electronics can be replaced and/or upgraded. The upgraded electronics can have their pipelines significantly extended to achieve the required latencies. However, the MDT is the only part that cannot be fully upgraded due to its inaccessibility, thus imposing a major constraint on the triggering rates. This constraint is met by having the triggering rate ≤ 200 kHz and a latency of 20 μs. Other constraints across the detector can be seen in Table 4.1.

| **Detector** | **Max. Rate** | **Max. Latency** |
|---|---|---|
| MDT | ~200 kHz | ~20 μs |
| LAr | any | any |
| TileCal | > 300 kHz | any |
| ITK | > 200 kHz | < 500 μs |

Table 4.1: The anticipated constraints on the Level-1 accept rate.

### 4.2.2 Level-0/Level-1

Level-0 has the same design as the current Phase-I Level-1 trigger. The newly introduced Level-1 trigger has the following sub-systems:

- L1Track trigger: to Supply RoI track parameters found at Level-0.
- L1Calo trigger: has access to full calorimeter granularity and can access data from the RoI region.
- MDT trigger: track momentum is reconstructed using the information from the MDT. It provides improves the background rejection of low momentum muons. This could be part of Level-0 or Level-1.

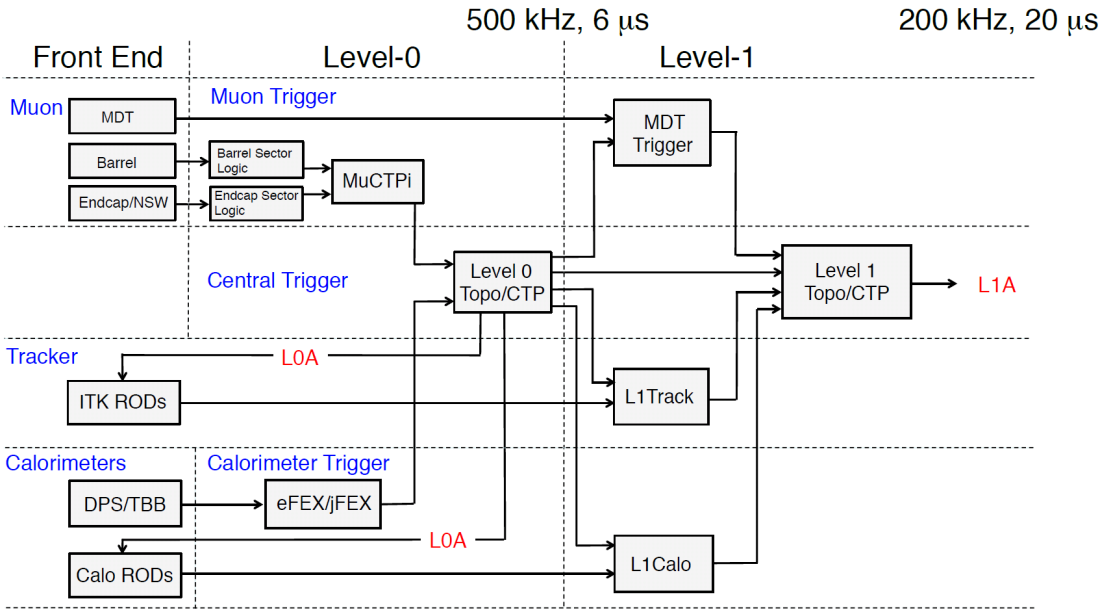



Figure 4.2: The Level-0/Level-1 triggering architecture. The MDT is shown as part of Level-1 but could be moved to Level-0[20].

- Central Triggering Processor (CTP): makes a decision based on the information from the three systems mentioned above.

### Level-1 track trigger

Triggering only on the information from the calorimeters and the muon chambers is not sufficient and unsustainable. The tracker is another source of information and along with the L1Calo and MDT trigger, it has the capability to improve the purity of the events accepted at Level-1. Simulations[68] have shown that the Level-1 tracker is capable of reducing the total trigger rate from ~ 500 kHz to ~ 200 kHz. The RoI principle is the baseline design of the track trigger system: it would provide information for all the tracks within the RoI defined at Level-0. This type of design can only be implemented in the Level-0/Level-1 split trigger system. Another alternative self-seeded track trigger design is also being investigated [20].

On the arrival of a Level-0 trigger an event is moved from the front-end to a buffer tagged by a unique Level-0 ID (L0ID). Later, a RoI device broadcasts a Regional Readout Request (R3) to the front-end devices within the RoI. The R3 data is consequently sent to the CTP along with information from the MDT and L1Calo triggers to generate a Level-1 Accept (L1A) signal. Preliminary results have shown that the RoI driven track trigger can read out 95% of the RoI data within 6 μs, assuming 160 MHz readout lines[20].

### 4.2.3 High-level trigger

Many tools previously employed in Level-2 will move to Level-1 for the Phase-II triggering system. This includes tracking, fine granularity calorimetry and topological triggers. The HLT is expected to reduce the Level-1 200 kHz rate to 5-10 kHz and will utilise multi object signatures (e.g. a combination of lepton, jets, jets with b-tagging and $E_T^{miss}$). The HLT also has to be redesigned to employ offline type selections while fully exploiting the evolution in computer hardware.

## 4.3 Inner tracker

The ATLAS tracker's role is to identify and reconstruct tracks of charged particles. The new ATLAS tracker has to do this while operating in the harsh conditions of the HL-LHC. The new tracker is currently being prototyped with an all-silicon layout that will mitigate against the anticipated high occupancies. The sensors will have fine granularity to handle the high pile-up and facilitate the track reconstruction. In addition, new electronics are needed to significantly increase the bandwidth compared to the current detector while improving their radiation hardness.

### 4.3.1 Motivations for the new layout

#### Radiation damage

The inner pixel layer is predicted to have a maximum fluence of $1.4 \times 10^{16}$ $n_{eq}$ cm$^{-2}$ while the inner most layer of the strips tracker to have a maximum fluence of $5.3 \times 10^{14}$ $n_{eq}$ cm$^{-2}$, this is shown in Figure 4.3. The current pixel and SCT layers are designed to withstand $10^{15}$ $n_{eq}$ cm$^{-2}$ and $2 \times 10^{14}$ $n_{eq}$ cm$^{-2}$, respectively. Both design limitations are well below the predicted fluences at the HL-LHC.

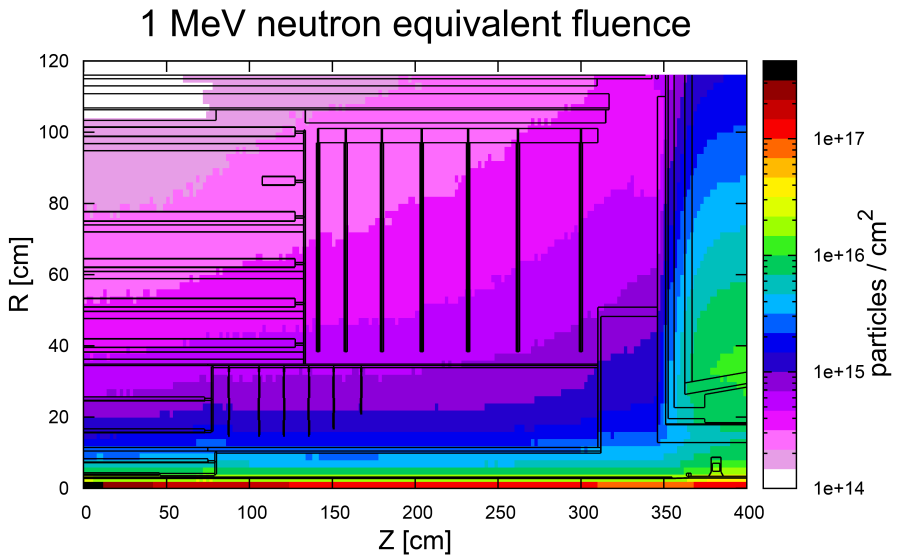



Figure 4.3: The inner tracker at 3000 fb$^{-1}$. Plotted as 1 MeV $n_{eq}$ fluence in R and Z direction[21].

#### Bandwidth limitation

The pixel and SCT front-end chips were designed to employ zero suppression[1] logic for upto 50 pile-up events per bunch crossing. The increase in the number of pile-up events, as expected in

[1] A simplistic compression method where all the data with no information (the zeros) are removed. The remaining data no longer becomes an array and loses its indices, therefore the channel number has to be attached to every '1'.

the HL-LHC, would saturate this bandwidth and lead to a significant reduction in efficiency.

#### Occupancy

One of the major drivers behind the all-silicon tracker is the HL-LHC occupancy. The occupancy measures the number of particles traversing a detector element per event. Using the current inner tracker design at the HL-LHC would result in high occupancy, with the TRT expected to have an occupancy close to 100%. In addition, the increased occupancy at the different layers of the detector reduces the efficiency in resolving close-by particles.

### 4.3.2 Layout comparison

The current and upgrade layouts are compared in Table 4.2 and Figure 4.5.

| | Current tracker | | | Upgrade tracker | | |
|---|---|---|---|---|---|---|
| | $R_s$ (mm) | $R_e$ (mm) | $A_{Si}$ (m$^2$) | $R_s$ (mm) | $R_e$ (mm) | $A_{Si}$ (m$^2$) |
| Pixel barrel | 50.5 | 122.5 | 2.7 | 39 | 250 | 5.1 |
| Pixel end-cap | 88.8 | 149.6 | | 150.1 | 315 | 3.1 |
| Strip barrel | 299 | 514 | 62 | 407 | 1000 | 122 |
| Strip end-cap | 275 | 560 | | 385 | 970 | 73 |
| TRT barrel | 563 | 1066 | | | | |
| TRT end-cap | 644 | 1004 | | | | |

Table 4.2: A comparison of the geometry of the current and upgrade trackers. $R_s$ is the start radius, $R_e$ is the end radius and $A_{Si}$ is the total Si area.

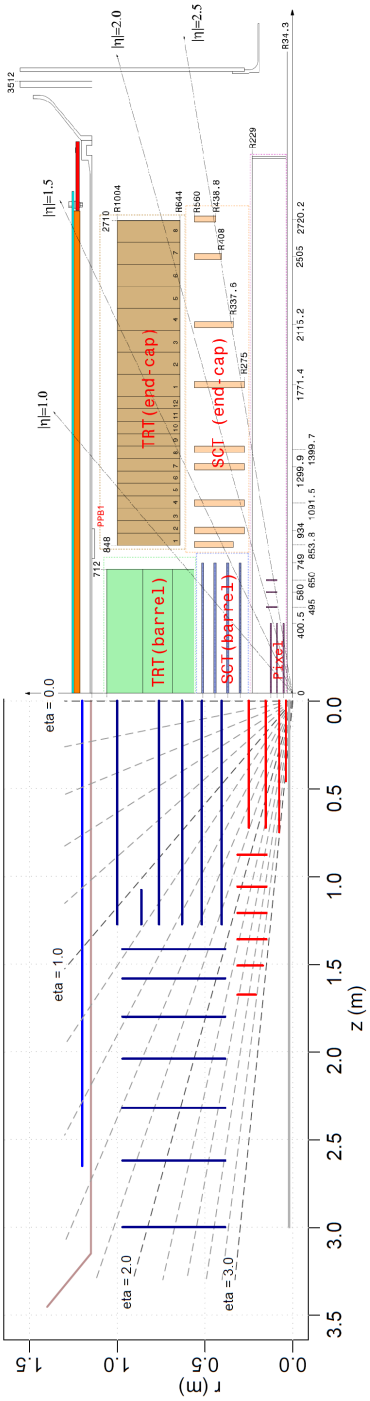



Figure 4.4: A comparison of the layouts of the upgraded inner tracker (left) and the old inner tracker (right). For the upgrade layout, the blue color represents the strips and the red represents the pixel. Note that the TRT layer is not part of the new layout.[9, 20]

### 4.3.3 Layout performance

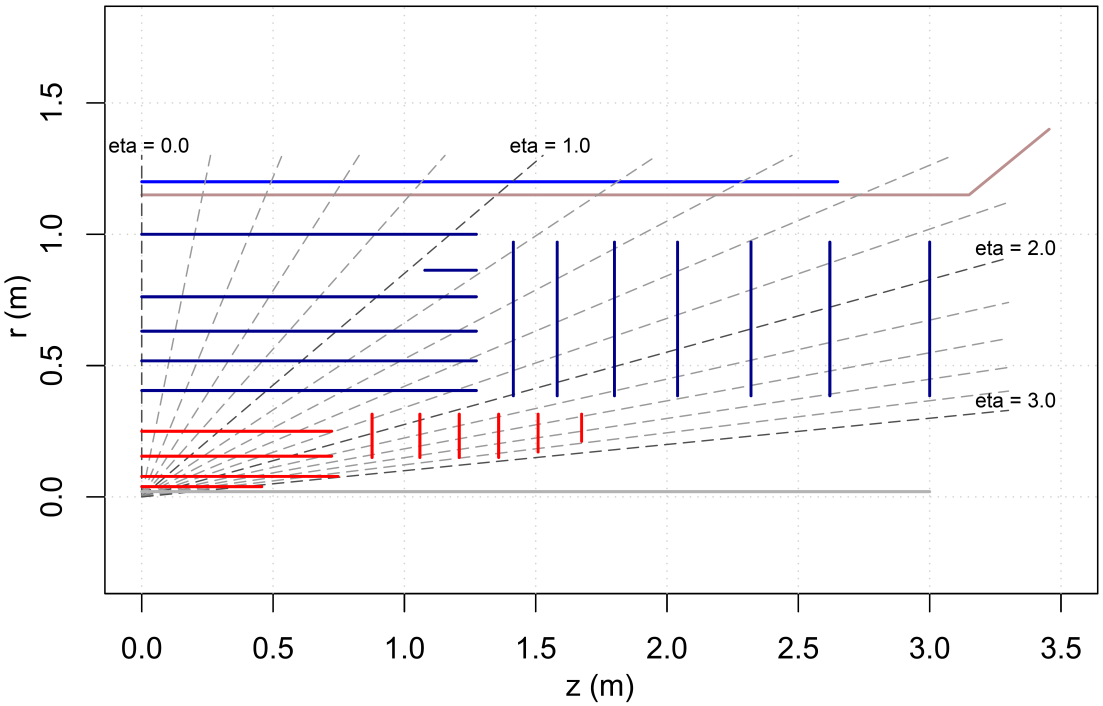



Figure 4.5: The layout of the upgrade inner tracker[20].

In addition to the considerations that have been put into the layout design due to the harsh HL-LHC conditions, the layout must also be designed to improve the tracking performance. There are several criteria in achieving this:

1. Number of hits per track.

   Simulations[20] have shown that a minimum of 11 hits are required to reconstruct a track while minimizing the number of fake tracks[2]. Figure 4.6 shows the ratio of the reconstructed number of tracks to the true number of tracks and this increases for 9 hits per track with higher pile-up. This indicates an increase in the number of fake tracks. On the

[2] Tracks that do not belong to a real particle

other hand, having 11 hits per track shows no clear increase in the reconstruction ratio, hence no there was no increase in the number of fake tracks.

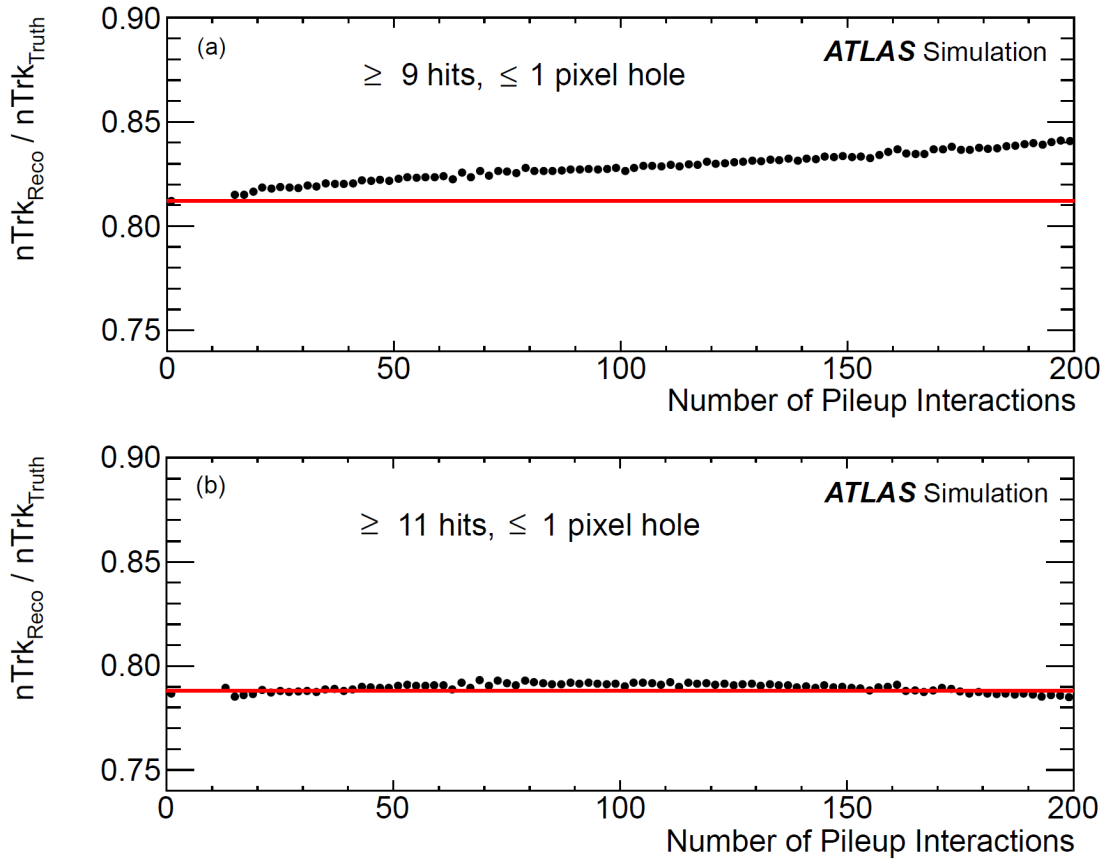



Figure 4.6: The ratio of the number of reconstructed to the number of generated tracks for different levels of pile-up events. The plots show the ratio for 9 hits per track and for 11 hits per track.

The upgraded layout is designed to achieve 14 hits per track. Figure 4.7 shows that for $|\eta| \leq 2.3$ the strip hits dominate while for $|\eta| > 2.3$ there is more reliance on the pixels.

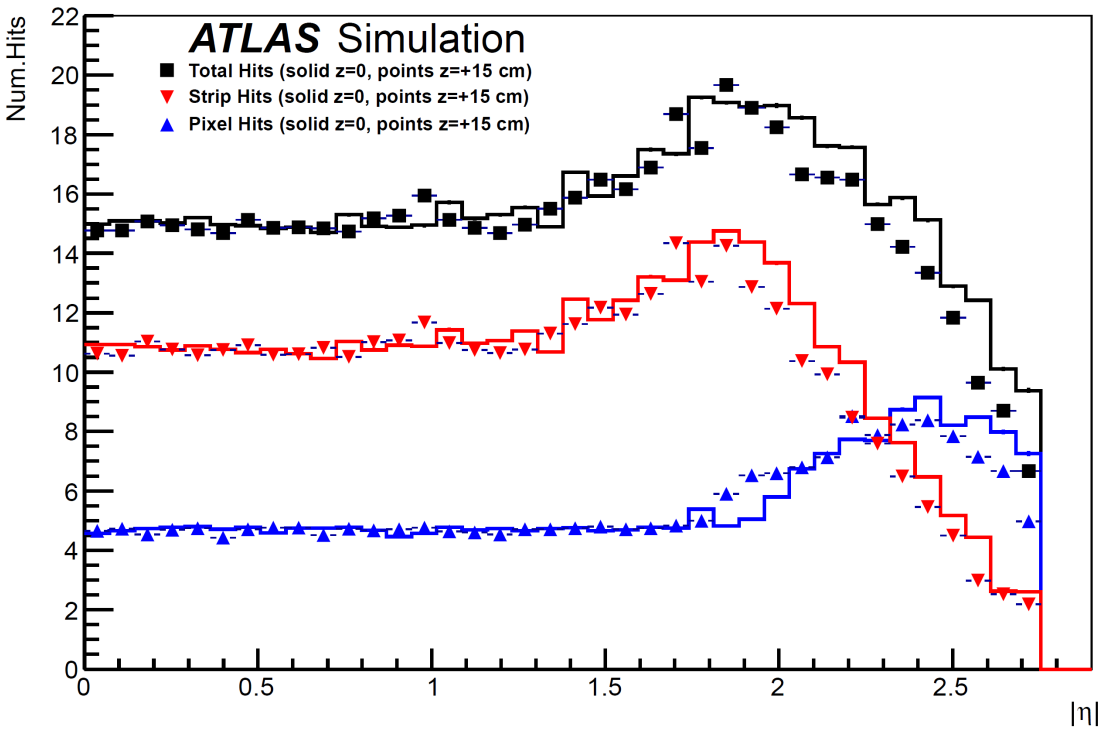



Figure 4.7: The number of hits on muon tracks as a function of $|\eta|$[20].

2. Momentum resolution.

   The momentum resolution can be improved by having a layer arrangement that maximizes the length of the particle trajectory in the solenoid. Short stubs have also been added to avoid the loss of acceptance between the barrel and end-caps regions.

3. Occupancy and particle separation.

   A finer sensor granularity is required to accommodate the high pile-up. This is achieved by having smaller pixel sizes and shorter strips. This is most relevant in the inner most layers. Figure 4.8 shows the expected occupancies for a 200 pile-up event.

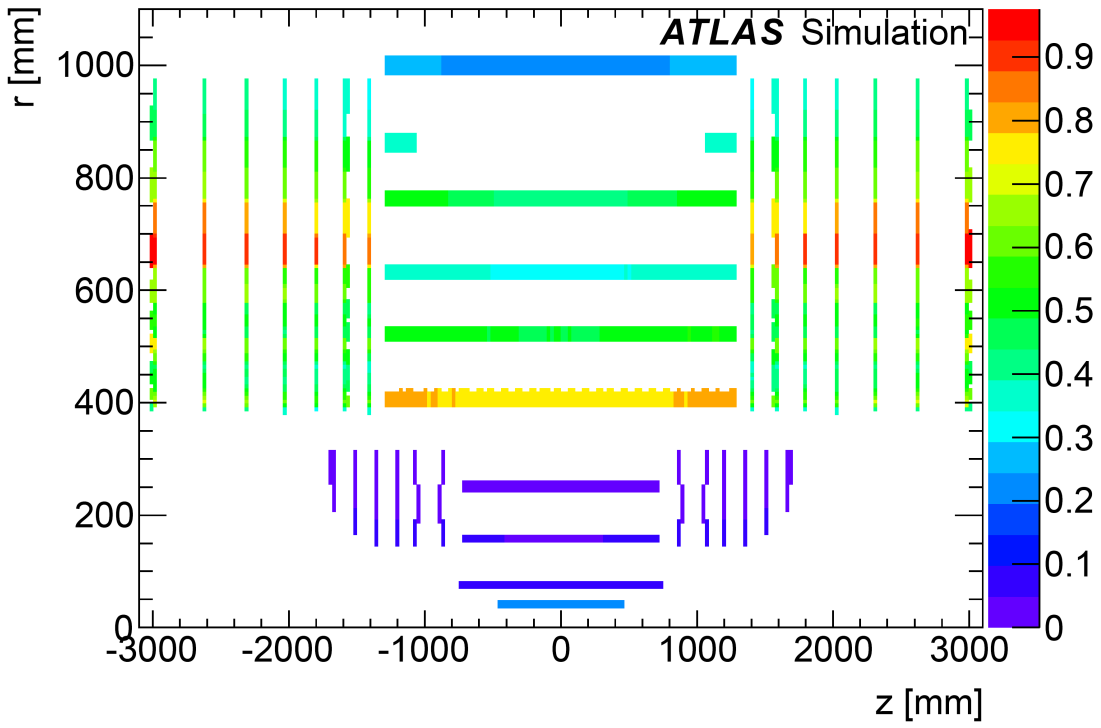



Figure 4.8: The channel occupancies (%) for a 200 pile-up event[20].

4. Material.

   Interactions with the detector material could greatly affect the performance of the tracker. The material used in the inner tracker has to be minimized to reduce particle losses due to interactions with the detector material. A reduction in the material can reduce the multiple scattering which improves the resolution of the detector. The new layout has a radiation length less than $0.7X_0$ up to $|\eta| = 2.7$ compared to $1.2X_0$ for the current inner tracker.

### 4.3.4 Pixel detector

To address the physics requirements and the harsh tracking environment at the HL-LHC, the pixel layer needs to provide fine granularity, high bandwidth and have the minimum amount of

material. The new tracker has four pixel barrel layers and six end-cap disks, as shown in Figure 4.5. The radial position of the layers dictates the amount of radiation it is exposed to and this will be one of the major factors in determining which technology is used for the pixel sensors.

### Pixel sensor technologies

The experience that will be gained from the Insertable B-Layer (IBL)[22] will help decide on the the pixel sensor technology for the Phase-II upgrade. The IBL is employing planar and 3D sensor technologies, these two technologies along with Diamond and CMOS sensors are the four possible pixel technologies. Table 4.3 summarises the advantages and disadvantages of the four sensor technologies.

Planar sensors are good candidates for the outer layers of the barrel region and for all of the end-cap disks, because of the lower radiation dose at these layers compared to the inner barrel layers. At the inner barrel layers, 3D sensors could be more suited due to their improved radiation hardness.

The R&D efforts that have been put into investigating monolithic CMOS technology have shown the technology to have great potential in particle detection and there are a few proposals of an all CMOS pixel detector[24]. In general, there will also be three different geometries for the pixel modules for the different layers. A 2-chip module (two chips with a $4 \times 2$ cm$^2$ sensor) used at the inner-most barrel layer. A quad-module (four chips with a $4 \times 4$ cm$^2$ sensor) for the outer barrel layers and a hex-module (six chips with a $6 \times 4$ cm$^2$ sensor) for the end-cap disks.

| | Advantages | Disadvantages |
|---|---|---|
| Planar sensors | • Mature technology.<br>• Can be mass produced.<br>• Many vendors.<br>• High yield.<br>• Low cost.<br>• Good rad-hard models. | • Irradiation damage leading to higher bias voltage.<br>• Increase of noise with irradiation.<br>• Dead areas due to guard rings.<br>• High bias voltage. |
| 3D sensors [23] | • Low bias voltage.<br>• Fast charge collection.<br>• Active edges (No guard rings).<br>• Radiation hard. | • The edges can be inefficient.<br>• Costly.<br>• Low yield. |
| Diamond sensors | • Fast signal.<br>• High signal to noise ratio.<br>• Radiation hard.<br>• No processing needed, only electrodes.<br>• No cooling required. | • Low signal.<br>• Expensive. |
| HVCMOS sensors | • High resolution.<br>• Includes active circuit (amplifier, comparator, etc.).<br>• Low capacitance; low noise.<br>• Cheap; an industry standard process. | • Very thin depletion zone.<br>• Radiation hardness not properly tested.<br>• Immature technology in HEP. |

Table 4.3: A comparison between the four pixel sensor technologies.

### 4.3.5 Strips detector

As opposed to the current SCT, where individual modules are used, the upgraded strip tracker will employ staves and petals accommodating modules that share common powering, commu-

nication lines and cooling. The five cylinders at the strip barrel region consists of 472 full length staves, each carrying 26 modules (13 on each side). The module comprises of one or two hybrids (formed of ten ABC130 readout chips) glued on two back-to-back strip sensors. Similar to the current ATLAS design, the two glued sensors have a 40 mrad stereo angle. The readout chips are connected to the n-in-p AC-coupled sensors via wire-bonds, as shown in Figure 4.9. There are two variations of the strip sensors; long (47.755 μm) and short (23.820 μm). The short strips are used in the inner three cylinders and the long for the outer two, thus providing higher resolution in the inner layers. Each of the 14 end-cap disks (7 on each side) is populated with 32 petals sharing the same electronics found on the stave but using different sensor geometry. The sensors have radial strips pointing towards the beam line, resulting in a wedge shaped sensor. The petal modules also have an effective 40 mrad stereo angle between the opposite sides of the sensor, this is a result of a 20 mrad rotation within the sensor. A stave and a petal are shown in Figure 4.10. The design and operation of the strip sensors and the ABC130 chip are described in Chapter 5 and 10, respectively.

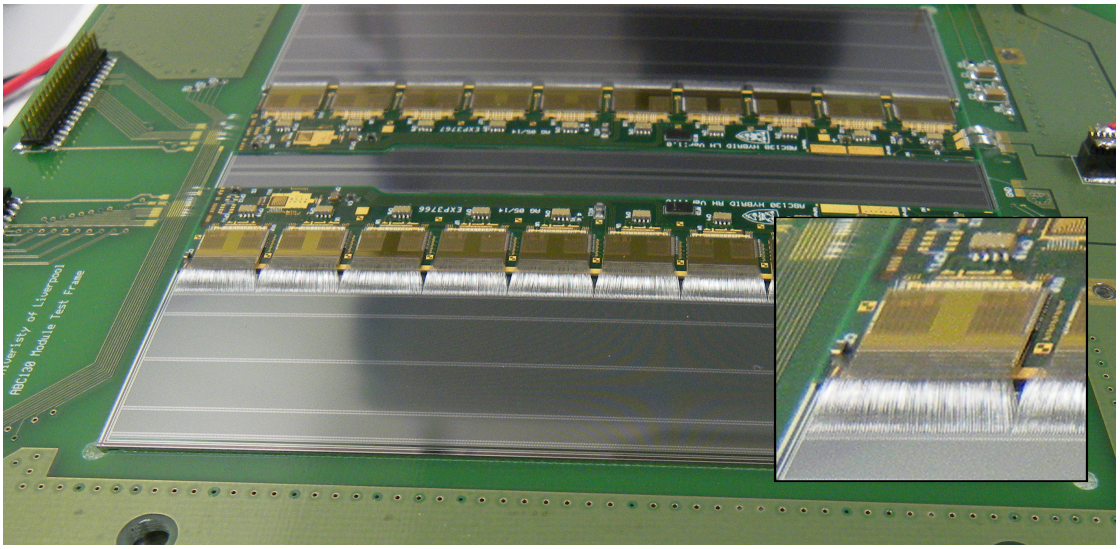


Figure 4.9: A picture of a strip module with ABC130 readout chips, assembled at University of Liverpool. The wire-bonds can be seen in the inset box.

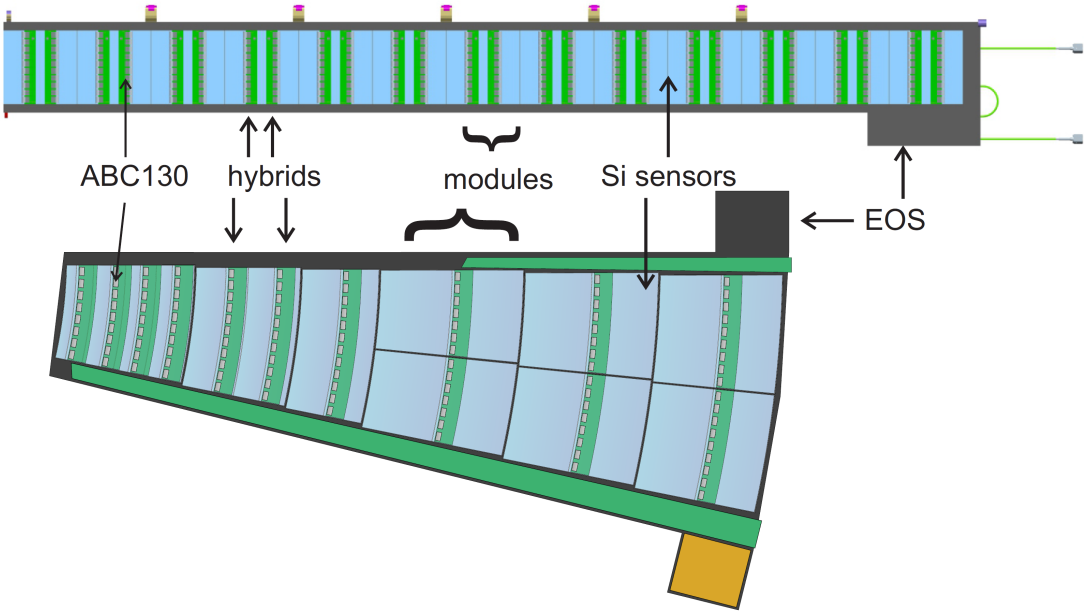



Figure 4.10: The proposed stave (top) and petal (bottom) structures. The diagram highlights the different sensor geometry for the two layouts and the number of readout chips per module.

## 4.4 Calorimeters

The expected energy deposition at the calorimeters for the HL-LHC is 5 to 10 times larger than the LHC values[20]. Most of the calorimeter readout electronics have to be replaced to cope with the harsher operating conditions while taking advantage of modern rad-hard technologies.

### 4.4.1 LAr calorimeter

The front-end of the liquid-Argon Calorimeter is partially placed in the calorimeter cryostat. It is subjected to a high radiation dose and can sustain good performance during the LHC but not at the HL-LHC. The LAr front-end electronics will be upgraded in steps and new triggering boards will be added during the anticipated long shutdowns of the LHC. These changes will result in a fully digital triggering architecture. In the new triggering system the LAr calorimeter digitizes all its signals and sends them off the detector at the bunch crossing rate. This effectively creates an unlimited Level-1 latency at the LAr calorimeter. This gives great flexibility and can accommodate both low and high latency triggering systems.
Furthermore, the back-end electronics that are housed in a non-radiation area will also be upgraded to cope with the data rates from the front-end electronics. The back-end needs to efficiently process the received data which is expected to have a total input rate of 140 Tbps.
At this stage the upgrade work on the Forward calorimeter is still under investigation with some studies[25] assessing the performance of the calorimeter at the HL-LHC.

### 4.4.2 Tile calorimeter

The tile calorimeter is to be upgraded to provide high granularity information to the triggering system. The tile calorimeter will be designed to continuously digitize and transfer its data off the detector. The data will include all readout channels and will be transferred at the bunch crossing

rate. The pipelines and derandomizing buffers will be integrated in the PreProcessor (PrP) units (housed in a non-radiated area) that will provide information to the Level-0 trigger.
The electronics at the tile calorimeter are shielded by the calorimeter itself. Thus the radiation constraints are not as stringent as they are on the other layers of the detector. This is why the front-end electronics could be developed with commercial FPGAs, but it will still be a challenge to meet the fast switching requirements and single-event-upset scenarios due to the large area of FPGAs.
To extract the signal features, off-detector electronics are used to receive information from the front-end electronics and perform their own sophisticated algorithms. The total bandwidth required for the tile calorimeter is around 9.5 Tbps.

## 4.5 Muon spectrometer

The latency value for the Level-1 trigger is dictated by the MDT. The MDT's readout electronics have to be replaced to overcome the latency problems. This is challenging since some chambers are located inside the toroidal magnets. Upgrading the electronics will also provide a better background rejection for high $p_T$ muons by reducing the number of low $p_T$ muons passing to the triggering system. Sharpening the high $p_T$ threshold is believed to reduce the rate of fake muon triggers by a factor of three[20]. In addition, the present electronics for the RPC and TGC will not be able to cope with the new Level-0/Level-1 trigger scheme and thus also need to be upgraded.

## 4.6 Phase-II scheduling

The third long LHC shut down is scheduled to start in 2023. The cavern will be accessible for around 27 months and the time for the installation is mainly driven by the time needed to insert the new inner tracker. The scheduling for the 27 months period can be seen in Figure 4.11.

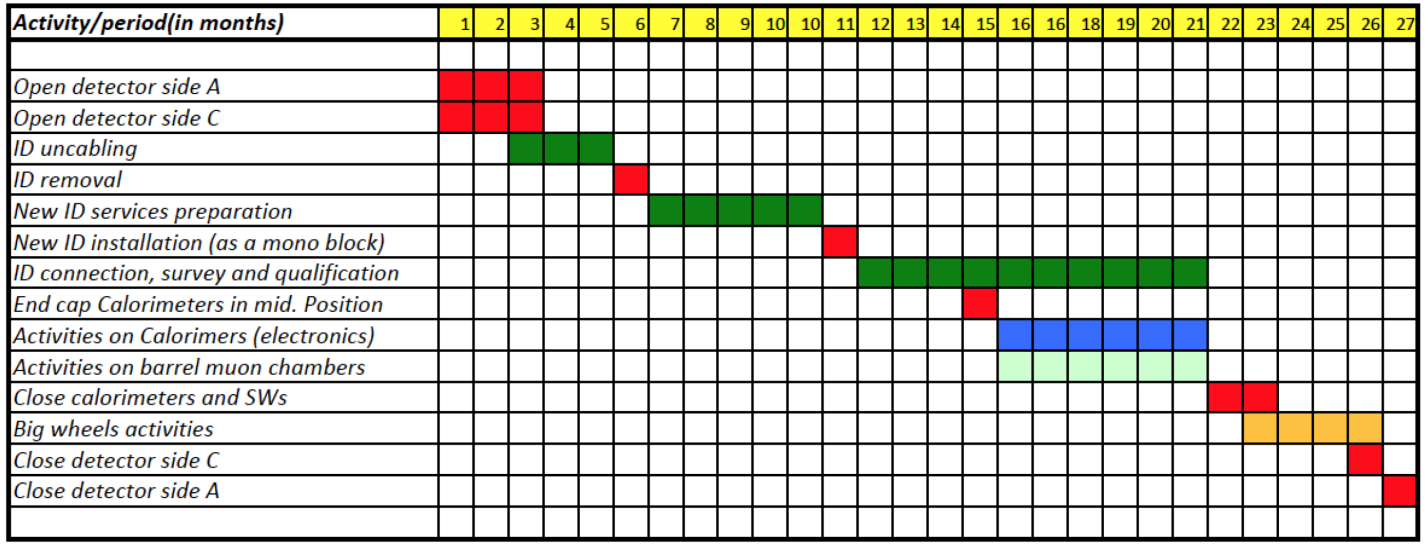



Figure 4.11: The installation schedule of the ATLAS Phase-II upgrade[20].

# 5 Silicon as a Particle Detector

## 5.1 Semiconductor properties

Depending on the energy band structure, solids can be classified as metals, semiconductors or insulators. Bohr[26] was able to explain why electrons of an atom occupy discrete energy bands and continuously orbit the nucleus. Bohr's model was sufficient to explain the behaviour of electrons in an atom but when a large number of atoms come together to form a solid, their behaviour changes. In a crystalline structure of atoms, the atomic forces of attraction and repulsion balance out to create the inter atomic spacing equilibrium. At equilibrium, the atoms create two continuous energy bands, the conduction and valence bands. The region between the two bands is called the forbidden gap. This gap, which is characterized by the band gap energy ($E_g$), defines the conduction properties of solids, as shown in Figure 5.1. Only electrons in the conduction band are allowed to freely move from one atom to the other, which is how the electric current is generated. Insulators have a large band gap that makes it impossible to excite electrons from the valence band to the conduction band by means of thermal energy or even an applied electric field. In metals, the forbidden gap does not exist so there are always free electrons in the conduction band. Semiconductors, on the other hand, sit in the middle and have a relatively small band gap.

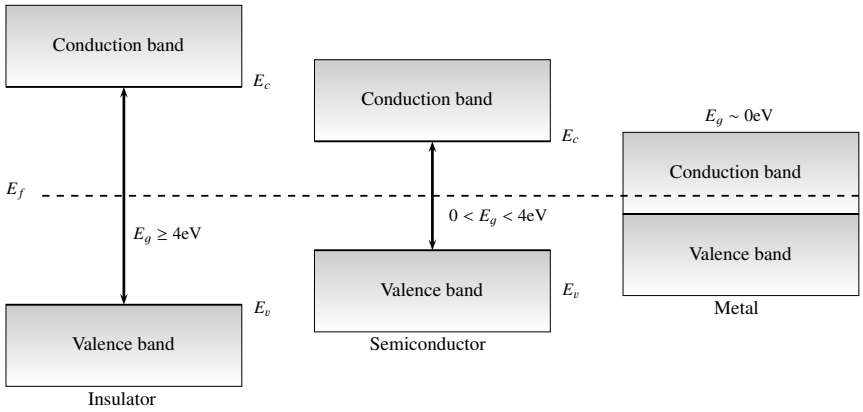



Figure 5.1: The energy band structures for insulators, semiconductors and metals.

An intrinsic semiconductor (i.e. with no impurities) at a temperature above absolute zero can have some thermally excited electrons jumping from the valence band to the conduction band, leaving a hole behind. Holes can be regarded as positive charge carriers and follow the same Fermi-Dirac statistics.

For an intrinsic semiconductor:

$$n = p = n_i$$

$n$: Concentration of electrons; $p$: Concentration of holes; $n_i$: Intrinsic carrier concentration

The free charge carriers are the electrons and holes in the conduction and valence bands, respectively.

In the presence of an electric field, both electrons and holes drift. Their drift velocity is proportional to the applied electric field and can be expressed as:

$$v = \mu\epsilon,$$

where $\mu$ is the carrier mobility and $\epsilon$ is the applied electric field. For electrons $v_n = -\mu_e\epsilon$, note

the negative velocity since the electrons, which are negatively charged, drift against the electric field. The current density for electrons and holes can be expressed as:

$$J_n = -nev_n \text{ and } J_p = -pev_p.$$

Due to the dependence of the conductivity of a semiconductor on the electric field and the net current density $\sigma = J/\epsilon$, the conductivity can be finally expressed as

$$\sigma = ne\mu_e + pe\mu_p.$$

### 5.1.1 Band gap and doping

The number of states across the energy bands is infinite. However, the number of electrons is not. They must equal the number of protons, therefore only a few states can be occupied at any given time. The probability of any electron occupying an energy level is defined by the following Fermi-Dirac distribution

$$f_e(E) = \frac{1}{e^{\frac{E-E_f}{kT}} + 1}.$$

Where $E_f$ (Fermi level) is the energy level at which the probability of an electron occupation equals $\frac{1}{2}$. Similarly, the Fermi-Dirac distribution for holes can be expressed as

$$f_h(E) = 1 - f_e(E),$$

and is due to the fact that if an energy state is not occupied by an electron then it will be occupied by a hole. The distribution, represented in Figure 5.2, illustrates the temperature dependence of the probability of an electron occupying the conduction band; the higher the temperature the higher the probability.

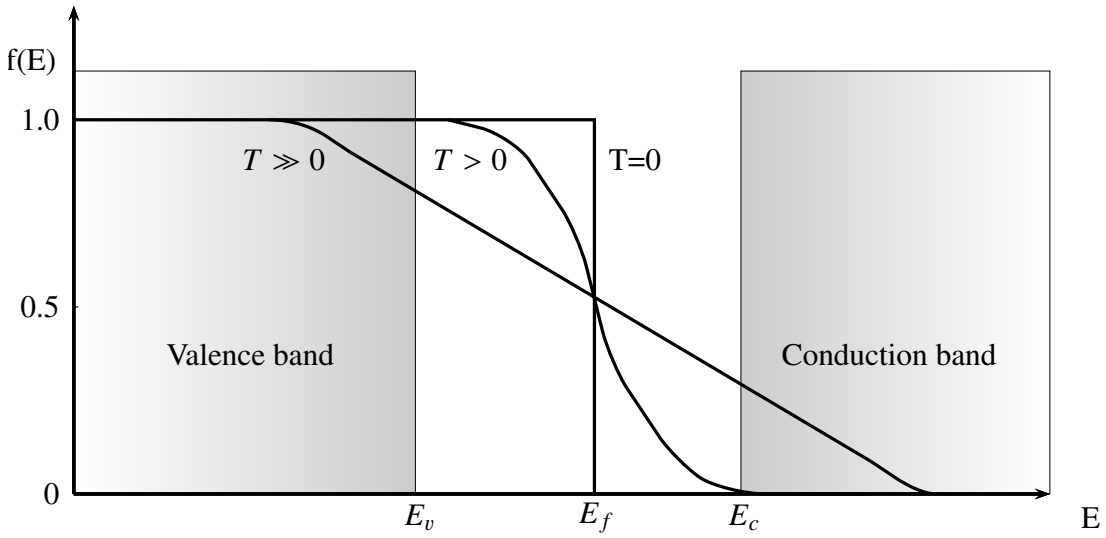



Figure 5.2: The Fermi energy distribution function f(E) as a function of the electron energy (E). $E_v$ and $E_c$ are the energy levels for the valence and conduction bands, respectively[27].

While the Fermi-Dirac distribution depends on the temperature, the density of states function, which is a pure quantum mechanical distribution, depends on the material itself. It describes all the intervals of energy an electron can occupy at a certain energy level. The density of states function is expressed as

$$g_e(E) = M_c \frac{\sqrt{2}}{\pi^2} \frac{(E - E_c)^{\frac{1}{2}}}{\hbar^3} (m_e^*)^{\frac{3}{2}}.$$

Similarly for holes

$$g_h(E) = M_v \frac{\sqrt{2}}{\pi^2} \frac{(E - E_c)^{\frac{1}{2}}}{\hbar^3} (m_h^*)^{\frac{3}{2}},$$

where $M_c(M_v)$ is the number of equivalent conduction(valence) band minima contained in the first Brillouin zone (for Si $M_c = 6$ and $M_v = 1$), $m_e^*(m_h^*)$ is the density of states effective mass and $\hbar$[1] is the Dirac constant.

[1] $\hbar = \frac{h}{2\pi}$ also known as reduced Planck constant.

Consequently, the density of free electrons in the conduction band can be calculated by integrating the product of $f_e(E)$ and $g_e(E)$, giving:

$$n = \int_{E_c}^{\infty} f_e(E) g_e(E)\, dE.$$

Due to the difficulty of including the width of the conduction band and the fact that the Fermi level is well below the top of the conduction band, the upper limit has been replaced by infinity and the integral reduces to:

$$n = N_c e^{-\frac{E_c - E_f}{kT}}.$$

and for holes

$$n = N_v e^{-\frac{E_f - E_v}{kT}},$$

where $N_c$ and $N_v$ are the effective densities of states and are affected by the temperature and the effective mass. $N_c$ and $N_v$ can be approximated to

$$N_c = 2M_c \frac{m_e^* kT}{2\pi\hbar^2} \text{ and } N_v = 2M_v \frac{m_h^* kT}{2\pi\hbar^2}.$$

To maintain charge neutrality, the number of electrons in the conduction band must equal the number of holes in the valence band.

Thus,

$$np = n_i^2 = N_c N_v e^{-\frac{E_g}{kT}}$$

where $E_g$ is the band-gap ($E_v - E_c$).

This is known as the mass action law and it holds for intrinsic and extrinsic semiconductors (i.e. doped and undoped semiconductors).

The physical properties of a semiconductor can be altered by the introduction of impurities, a

process known as doping. Depending on the impurity, donor or acceptor, they either increase the electron or the hole density, respectively. The type of dopant can be determined from the periodic table. Group IV elements (Si and Ge) can have Group V donors (P, Sb and As) and Group III acceptors (B, Al and Ga). Acceptors lack an electron which they can acquire from the host atom, releasing a mobile hole, while donors have an unpaired electron which frees and moves to the conduction band. Donors are n-type dopants and acceptors are p-type dopants.
Doping affects the band-gap ($E_g$) of a semiconductor. Dopants create a new energy level within the forbidden region, effectively reducing $E_g$. Donors create an energy level just below the conduction band ($E_d$) while acceptors create one just above the valence band ($E_a$), as illustrated in Figure 5.3.

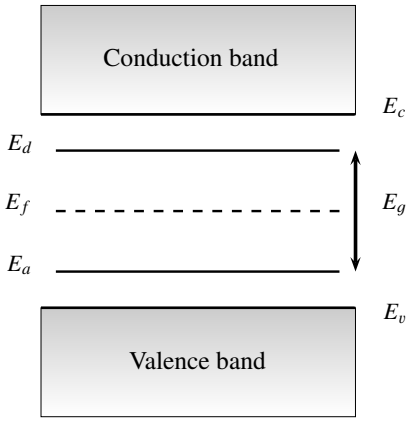



Figure 5.3: The donor and acceptor levels within the forbidden gap.

Doping also affects the electron and hole mobility. The carrier mobility decreases when the doping concentration increases. Silicon has high mobility which makes it suitable for fast particle detection. For high donor dopant density $N_d$, the resistivity of an extrinsic semiconductor can be expressed as

$$\rho = \frac{1}{e(\mu N_d)}. \tag{5.1}$$

This is an important parameter for particle detectors as it defines the operational voltage of the sensors; a characteristic of the sensors which will be explained later in this chapter.

## 5.2 The p-n junction

In a standard silicon sensor the number of free charge carriers is much greater than the amount of charge generated by an ionizing particle. To reduce the number of charge carriers the sensor can be cooled to very low temperatures (near zero Kelvin) or a reversed biased p-n junction can be used. The latter is more suitable for HEP due to the size of the experiment which makes cryogenic cooling a highly non-practical solution.

The principal of a p-n junction is to bring two semiconductor regions, of opposite and uniformly distributed doping types, together to form a junction. At the junction, electrons start to diffuse to the p-region and holes diffuse to the n-region, thus creating a region depleted of mobile carriers. This region is known as the depletion region or space-charge region (SCR).

When no voltage is applied across the p-n device the Fermi level is constant across the device as seen in Figure 5.4.

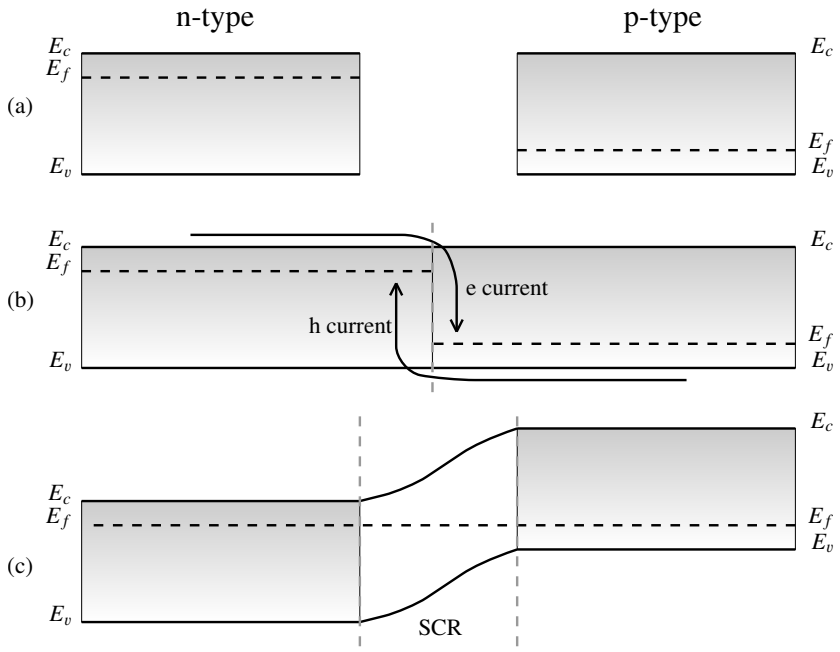



Figure 5.4: The energy levels of a p-n junction. (a) shows the p-type and n-type material separated and when joined (b) electrons move to the lowest Fermi level and holes move to the highest Fermi level, creating the SCR region in the middle.(c) At equilibrium, the Fermi level is equal everywhere.

The difference between the n-type and p-type regions $E_f$ (prior to the equalization), defines the built-in equilibrium voltage ($V_{bi}$) to be

$$eV_{bi} = E_{fn} - E_{fp},$$

where $e$ is the charge of the electron.

The junction between the two regions acts as a barrier to the movement of free charge carriers. An applied external voltage can assist the charge carriers to move across the junction or it can make the movement even more difficult. If the positive voltage is applied to the p-region (referred to as forward biasing) it allows the charge carriers to move freely across the junction (i.e. lowering the barrier). If the positive voltage is applied to the n-region (reverse biasing) the

barrier will be raised and the free charge carriers will not be able to move across the barrier. This is illustrated in Figure 5.5.

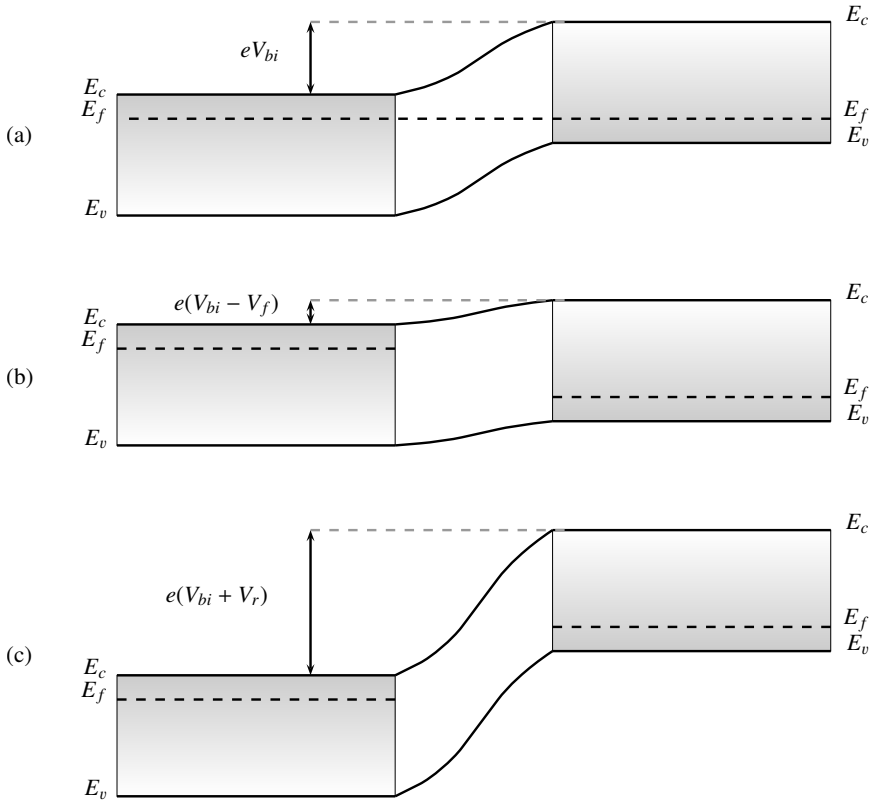



Figure 5.5: An illustrations of the energy band diagrams for (a) a p-n junction in equilibrium (b) in forward-bias (c) in reverse-bias. $V_f$ and $V_r$ are the positive forward and negative reverse applied voltages, respectively.

For particle detectors a reverse bias is required. The ionization happens at the SCR and the charge is collected at the junction. Charges created at the non-depleted regions recombines with free charge carriers and are lost. The width of the depletion region can be expressed as

$$w = \sqrt{2\epsilon\rho\mu V_{bias}},$$

where $\rho$ is the charge density (Equation 5.1), $\epsilon$ is the permittivity, $\mu$ is the permeability and $V_{bias}$ is the external applied voltage.

Thus the full depletion voltage can be expressed as

$$V_{fd} = \frac{D^2}{2\epsilon\mu\rho},$$

where $D$ is the thickness of the sensor.

Reverse biasing a p-n junction with a potential lower than the full depletion voltage will results in an under-depleted sensor with an inactive volume. Also, having a reverse bias voltage that is much greater then the full depletion region will result in an over-depleted sensor and might risk an electric field breakdown. The electric fields for all biasing conditions are described below:

$$\begin{aligned}
V_{bias} < V_{fd}: \quad & E(x) = \frac{2V}{D}\left(1 - \frac{x}{w}\right) \\
& \Rightarrow E_{max} = \frac{2V}{w} \\
V_{bias} = V_{fd}: \quad & E(x) = \frac{-q_e N}{\epsilon}(D - x) \\
& \Rightarrow E_{max} = \frac{2V}{D} \\
V_{bias} \gg V_{fd}: \quad & E(x) = \frac{2V_{fd}}{D}\left(1 - \frac{x}{D}\right) + \frac{V - V_{fd}}{D} \\
& \Rightarrow E_{max/min} = \frac{V \pm V_{fd}}{D}.
\end{aligned}$$

Using the standard capacitor parallel plate model and due to the dependence of the electric field to the depletion width, the capacitance of a silicon sensor ($C_{bulk}$) can be expressed as:

$$C_{bulk} = \begin{cases} A\sqrt{\frac{\varepsilon_{Si}}{2\rho\mu V_{bias}}} & V_{bias} \leq V_{fd} \\ A\frac{\varepsilon_{Si}}{D} = \text{constant} & V_{bias} > V_{fd}, \end{cases}$$

where A is the surface area of the sensor.

## 5.3 Principles of a Silicon detector

### 5.3.1 Particle detection

In order to detect a particle, it must interact with the detector and be able to transfer its energy in some recognizable way. Particles traversing through detectors lose energy by ionization, which could happen in any material. Semiconductors are particularly attractive due to their low intrinsic energy threshold. For instance, silicon generates one electron-hole pair for every 3.6 eV released by a traversing particle. This is ~10 times lower than the energy required to ionize gas molecules in a gaseous detector.

The mean rate of energy loss for a charged particle crossing a material is described by the Bethe-Bloch formula[28]:

$$-\left\langle \frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[ \frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right], \tag{5.2}$$

where $z$ is the charge of the incident particle, $T_{max}$ is the maximum energy transfer in a single collision, $I$ is the mean excitation energy, $m_e$ is the electron's mass, $Z$ is the atomic number, $A$ is the atomic mass, $K$ is a constant[2], $\beta = \frac{v}{c}$, $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ and $\delta(\beta\gamma)$ is the density effect correction to ionization energy loss.

The Bethe-Bloch formula is plotted in Figure 5.6. The most noteworthy region is around the minimum at $\beta\gamma = 3$. This point describes the minimum amount of energy that can be deposited into the medium. This energy is deposited by what is called a Minimum Ionizing Particle (MIP) and any detector must have its noise below this energy to be able to detect it. The values for the minimum ionizing energy loss rate against atomic number are shown in Figure 5.7.

[2] $K = 4\pi N_A r_e^2 m_e c^2 = 0.307075\ \text{MeV g}^{-1}\,\text{cm}^2$. $r_e$ is the classical electron radius, $m_e$ is the electron mass, $c$ is the speed of light and $N_A$ is Avogadro's number.

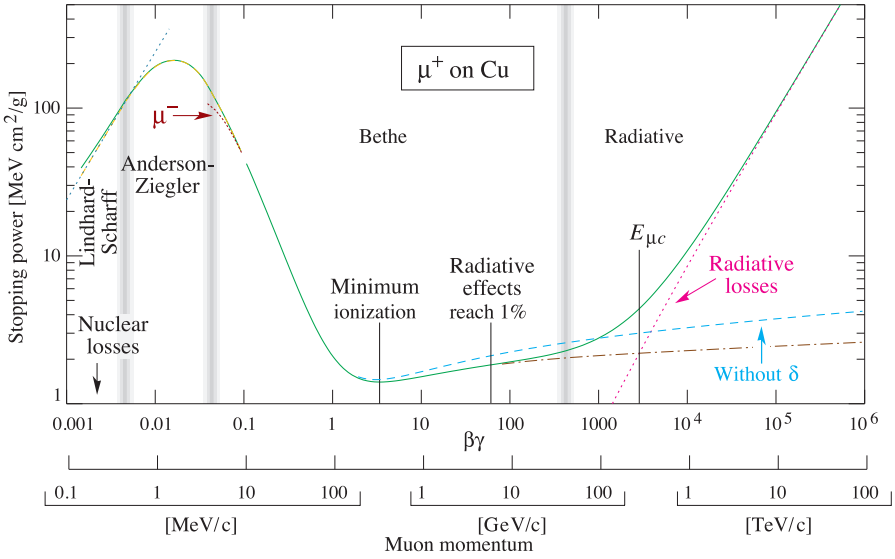



Figure 5.6: The $-\langle dE/dx\rangle$ for positive muons in copper as a function of $\beta\gamma = p/Mc$[28].

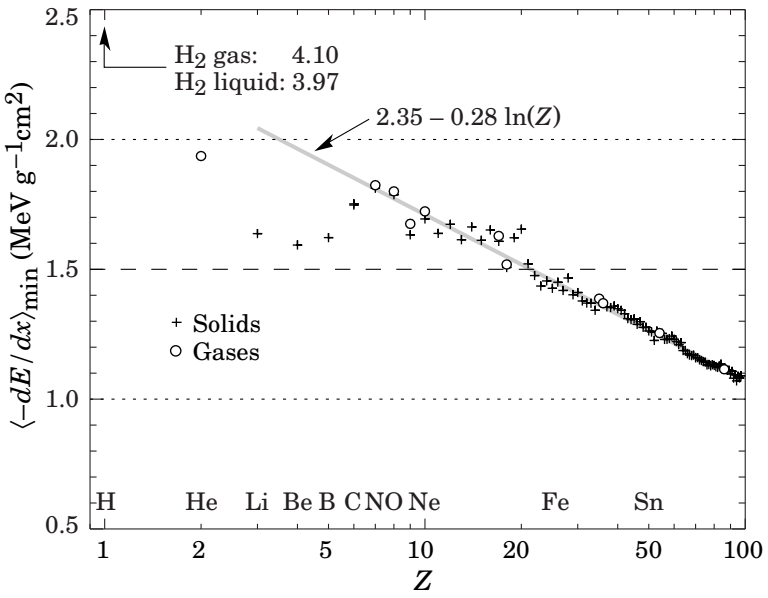



Figure 5.7: The minimum ionization energy for different elements. The minimum ionization energy for Si = 1.66 MeV $g^{-1}$ $cm^2$[28].

The mean energy loss given by the Bethe equation is not experimentally well-defined. It was not found very useful for describing the energy loss for single particles but does find application in dosimetry. Landau defined the statistical fluctuations and the kinematic limit on the maximum transferable energy in a single collision in a distribution known as Landau-Vavilov energy loss probability distribution [29, 30]. The most probable energy loss is

$$\Delta_p = \xi \left[ \ln \frac{2mc^2\beta^2\gamma^2}{I} + \ln \frac{\xi}{I} + j + \beta^2 - \delta(\beta\gamma) \right] \text{[31]} \tag{5.3}$$

Here $\xi = (K/2)(Z/A)(x/\beta^2)$ MeV for a detector with thickness $x$ in $\mathrm{g\,cm^{-2}}$. All other variables have their meanings as described in equation 5.2. Plotting the formula results in an asymmetric distribution. The beginning of the formula can be described with a Poisson distribution, while the second part (the tail) is described as the "straggling function". The tail extension comes from the transfer of energy by the creation of rare $\delta$-electrons or secondary-electrons. 90% of the collisions contribute to energy deposits below the mean. Thus, the most probable energy loss is 62% of the mean. Examples of a 500MeV pion traversing through different thicknesses of silicon are shown in Figure 5.8. A similar energy loss probability but scaled at minimum ionization is shown in Figure 5.9.

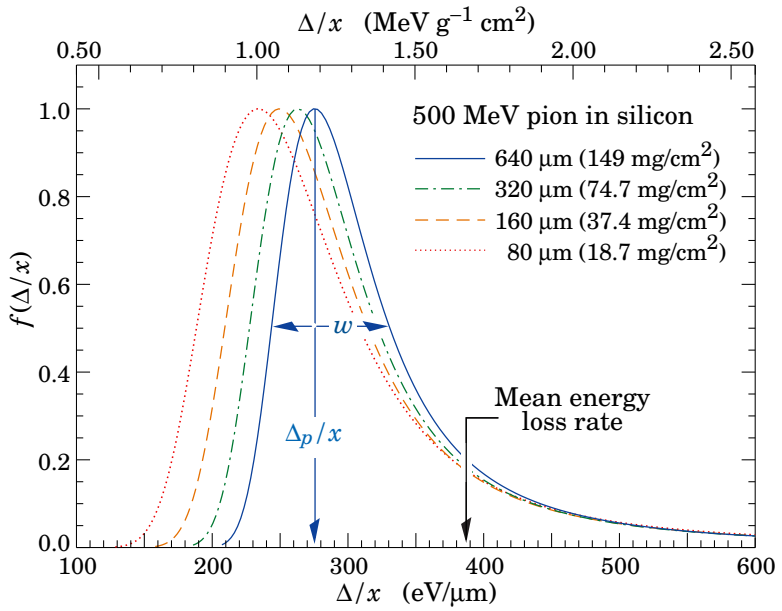



Figure 5.8: The straggling functions in silicon for 500 MeV pions, normalized to unity[28].

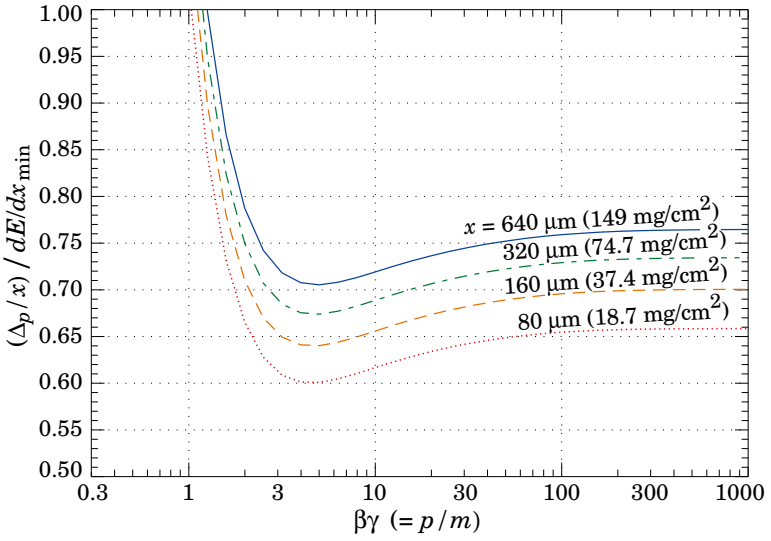



Figure 5.9: The most probable energy loss in silicon, scaled to the mean loss of a MIP[28].

The mean energy loss for Silicon is 3.87 MeV cm$^{-1}$ (1.66 MeV g$^{-1}$ cm$^2$×2.33 g cm$^{-3}$) and the mean ionization energy is 3.62 eV, three times larger than the energy band gap of 1.12 eV due to the deposited energy used for phonon creation, which will be explained in the next section. Assuming a 300 µm thick silicon sensor with an area of 1 cm$^2$, a signal of a MIP would be equivalent to

$$\frac{\left\langle \frac{dE}{dx} \right\rangle d}{I_0} = \frac{3.87\,\text{MeV cm}^{-1} \times 0.03\,\text{cm}}{3.62\,\text{eV}} \approx 3.2 \times 10^4\,\text{e-h pairs.}$$

Due to the Landau fluctuations the most probable number of e-h pairs is $62\% \times (3.2 \times 10^4) \approx 2 \times 10^4$ e-h pairs. The sensor at 300 K will have a number of free charge carriers = $dAn_i$ = $0.03\,\text{cm} \times 1\,\text{cm}^2 \times 1.45 \times 10^{10}\,\text{cm}^{-3} \approx 4.35 \times 10^8$ e-h pairs. The dominance of the thermally created e-h pairs (noise) explains the need for a fully depleted sensor.[3]

### 5.3.2 Photons and the minimum ionization energy

The mean energy required to create an e-h pair is considered as a material property of semiconductors. The bandgap of semiconducting material sets the minimum detection threshold. However, silicon photodiode measurements[32] have shown that an energy almost three times greater than the bandgap is needed to create an electron-hole pair. In silicon, there is an offset between the minimum wave vector at the conduction band and the maximum of the valence band, hence silicon is called an indirect semiconductor. For this reason, the transfer of both energy and momentum is needed to excite an electron to the conduction band, since a charge carrier cannot recombine on its own, as shown in Figure 5.10. The generation of phonons, which is basically a quantization of the lattice vibration, is needed to conserve momentum and energy. Band to band excitations in indirect semiconductors are theoretically impossible, therefore they need to be assisted by traps. The charge recombination and generation in indirect semiconductors are

[3] Intrinsic carrier density ($n_i$) of Silicon is $1.45 \times 10^{10}$ cm$^{-3}$[35].

described by the Shockley–Read–Hall process[33]. The process is described in two-steps where impurities introduce intermediate energy levels within the band gap (known as a deep level). In the the first step an electron is excited to the to the the deep level and in the second step an electron is excited to the conduction band. In both cases, momentum is conserved by generating phonons.

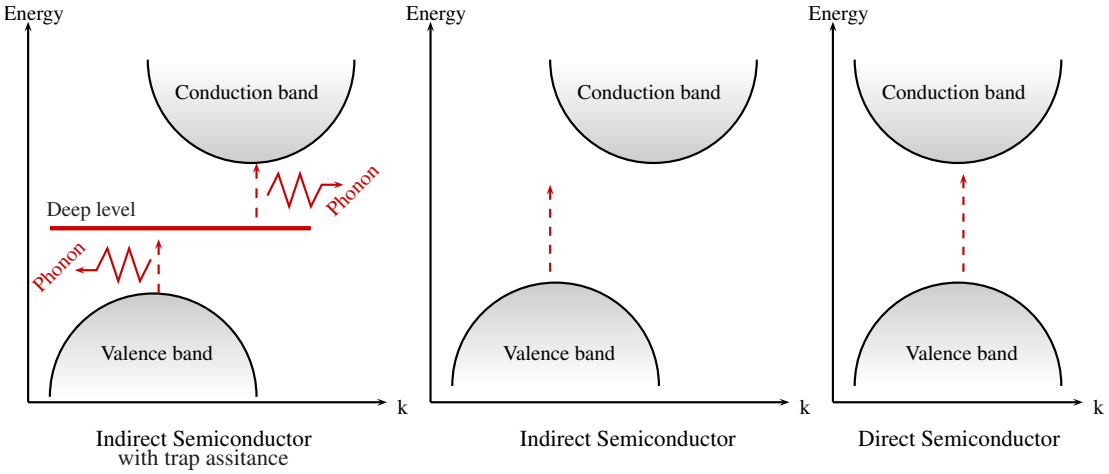



Figure 5.10: The energy band gap against the space wave vector (k) for direct and indirect semiconductors. The plot on the left shows how a phonon is needed to assist the movement of charge carriers to the conduction band.

The minimum energy needed for e-h pair generation is roughly proportional to the band-gap of the material and can be approximated by

$$E_i \approx 2.8E_g + 0.6\,\text{eV}[34].$$

The minimum ionization energy of Si is 3.62 eV, with a bandgap of 1.12 eV. This means only 30% of the photon's energy is used in forming mobile charge and the rest is lost into phonon production.

### 5.3.3 Silicon as a tracking device

The working principle of a silicon strip detector is illustrated in Figure 5.11. As a particle crosses through the detector, electron hole pairs are created along its path. Generated electrons drift to the n+ backplane of the sensor while generated holes drift to the p+ implants. The sensor has an applied voltage between the implants and backplane, a biasing voltage $V_{bias}$ which needs to be greater than the full depletion voltage of the sensor to ensure full activity of the sensors volume and enforce fast drift, as explained in Section 5.1. The charge collected at the implants is then induced via capacitive coupling (i.e. across the $SiO_2$ layer) to the metal strips. The strips are AC coupled to a charge pre-amplifier that is usually implemented in the readout chip.

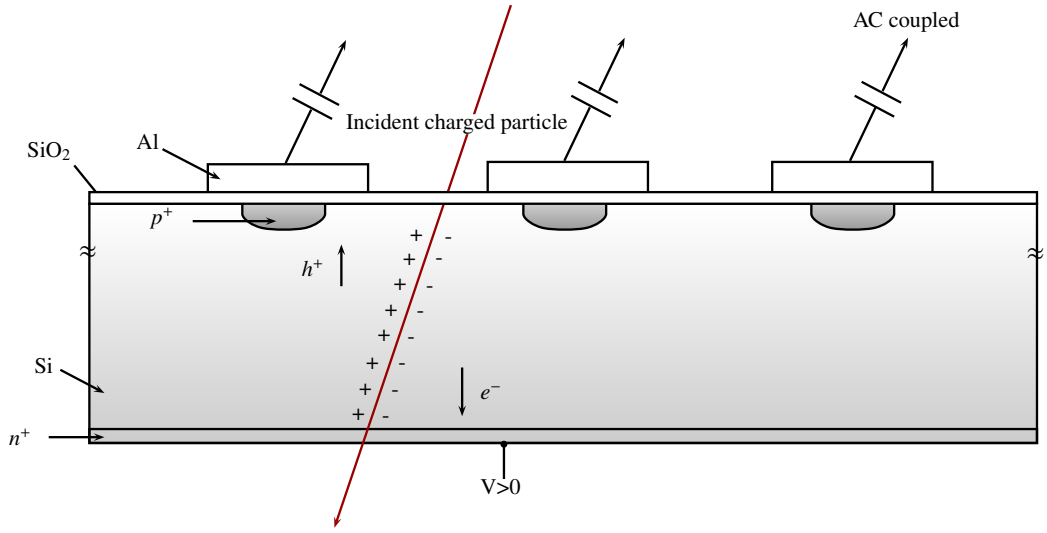



Figure 5.11: An illustration of a typical silicon strip detector and the passage of a particle.

One of the most important parameters of a strip detector is the resolution. This is initially set by the physics requirements on the detector (notably the momentum resolution, two particle separation and vertex reconstruction accuracy) and this is primarily governed by the strip spacing

"pitch". As shown in Figure 5.12, particles can cross anywhere between the strips. Due to the presence of noise, a threshold is set. A particle crossing the metal strip will have its charge almost completely collected at that strip, making it relatively easy to localize it. However, a particle going through two strips will have its charge collected by both strips. Assuming uniform charge collection, the particle position would be considered to be closer to the strip with more charge. For particles generating enough charge on two strips exceeding the threshold level, a centre of gravity method can be used, or an algorithm that processes the actual shape of the charge distribution to get a more precise location. However, the noise plays a major role in the localization. If a particle track is much closer to one of these strips, then the farther strip might be collecting charge with a level below the noise level, thus leading to poor localization. If pulse height ($ph$) is measured between two strips ($x_1$ and $x_2$), the position of a particle crossing the strips can be interpolated as follows

$$x = x_1 + \frac{ph_2}{ph_1 + ph_2}(x_2 - x_1) = \frac{ph_1 x_1 + ph_2 x_2}{ph_1 + ph_2}$$

As long as digital readout is required and by taking the center of the strip as the true coordinate, the resolution of the measurement can be estimated from the root-mean-square deviation from the strip coordinate as such:

$$\langle \Delta x^2_{intrinsic} \rangle = \frac{1}{\text{pitch}} \int_{-\text{pitch}/2}^{\text{pitch}/2} x^2 \text{dx} = \frac{\text{pitch}^2}{12}$$

The resolution is also limited by the noise performance of the sensor and is estimated as

$$\Delta x_{noise} \propto \frac{\text{pitch}}{SNR}$$

Thus, for digital readout, assuming (SNR » pitch), the resolution is

$$\Delta x = \sqrt{\Delta x^2_{noise} + \Delta x^2_{intrinsic}} \approx \frac{\text{pitch}}{\sqrt{12}}$$

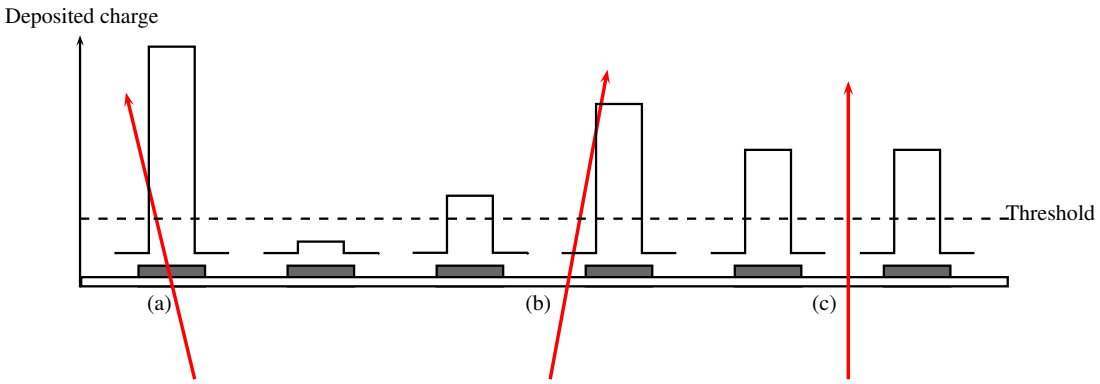



Figure 5.12: The signal on the strip depends on the particle location. (a) All of the deposited charge goes to the strip the particle is crossing. (b) The charge is distributed but more is collected at the strip nearer to the particles path. (c) A particle track is centred between the two strips and the charge is distributed equally.

### 5.3.4 Passivation and protection rings

#### Passivation

Pure silicon is very chemically reactive. $SiO_2$ is on the other hand a very stable and a near perfect dielectric and insulator. A thin layer of $SiO_2$ therefore coats the sensor and acts as a dielectric material between the metal strip and the implant, thus facilitating the capacitive coupling. $SiO_2$ is also used as final passivation, covering the entire sensor including the metal. Only the wire bonding and testing areas are later uncovered.

#### Rings

The strips are surrounded by two types of rings. The first is the bias ring, connecting to the implants through the bias resistors. The bias voltage is applied between the bias ring and the backplane. The bias ring covers the entire perimeter of the active area, to ensure a homogeneous potential throughout the sensor.
Outside the bias ring, there is the guard ring which is used to cover the sensitive edges of the sensor. This minimizes the edge effects where current could leak across the edges. The guard ring is usually connected to ground to drain the current.

## 5.4 Electrical sensor parameters

The electrical parameters define the quality of the signal and it also sets the operational conditions of the sensor. These parameters and their importance to the overall detector performance are described in this section.

### 5.4.1 Electric field

To guarantee an electrically stable sensor, the field configurations have to be taken into account. The strip structure is chosen carefully to obtain the best possible field layout, avoiding micro-discharges and field breakdowns. In intrinsic silicon, the breakdown voltage of a sensor with thickness ($t$) is

$$\frac{V_{break}}{t} = \frac{\varepsilon E_g^2}{2qN_{eff}} \approx 30\,\mathrm{V}\,\mu\mathrm{m}^{-1},$$

where $N_{eff}$ is the effective carrier density.
This clearly shows that a thick sensor will have a higher breakdown voltage. Also, to avoid areas with high fields, edge or point structures have to be avoided. This is why the implants have

round corners.

### 5.4.2 Coupling capacitance $C_{cp}$

The coupling capacitance is directly proportional to the charge created by the traversing particle. The capacitance is measured between the strip and implant. The value can be calculated using the standard parallel plate capacitance formula:

$$C = \varepsilon \frac{A}{d},$$

where $A$ is the surface area of the plate, $d$ is the distance between the parallel plates and $\varepsilon$ is the permittivity.

The $SiO_2$ is the dielectric between the two plates (strip and implant). The area the plates cover must not be too large as it affects other aspects of the sensor, such as the pitch of the detector. In this way, the thickness of the oxide is the only variable parameter. The $SiO_2$ layer needs to be as thin as possible, to obtain the high capacitance, while maintaining its original passivation functionality. The layer must provide robust and reliable insulation between the strip and implant without short-circuiting them. Points at which this happens are known as "pin-holes". With all these considerations and the technological challenges, an achievable thickness of an effective $SiO_2$ layer is about 200 nm.

### 5.4.3 Interstrip capacitance $C_{int}$

Capacitive coupling between strips can facilitate charge sharing; a very important aspect of the "centre of gravity" position determination and a large interstrip capacitance is desirable. However, the value for $C_{int}$ should still be less that $C_{cp}$, otherwise no charge will go into the pre-amplifier. Different experiments choose the capacitances based on a fixed ratio of $C_{int}/C_{cp}$.

For ATLAS the ratio is ~ 1:20.

### 5.4.4 Bulk capacitance $C_{bulk}$

The bulk capacitance is the capacitance formed between the backplane and the implant. The total bulk capacitance is measured from the implant to the backplane. The bulk capacitance for a single strip is then:

$$C_{blk} = \frac{C_{total}}{\text{number of strips}}.$$

Measurements of $C_{blk}$ can be helpful in locating damaged and/or faulty strips. Things like pinholes and defects significantly increase the measured $C_{blk}$ value. It can also be used to calculate the full depletion voltage of the sensor.

### 5.4.5 Strip capacitance $C_d$

Strip capacitance is the sum of all readout strip related capacitances.

$$C_d = C_{int} + C_{blk}.$$

This is the capacitance load to the pre-amplifier and is a major contributor to the overall noise.

### 5.4.6 Strip resistance $R_m$

The metal strip resistance helps define the signal pulse shape, which imposes a minimum acceptable resistance. The resistance of an aluminium strip of width ($w$) and thickness ($d$) can be calculated as follows

$$R_{Al} = \frac{\rho_{Al}}{dw}\,\Omega\,\text{cm}^{-1}.$$

where $\rho_{AL}$ is the resistivity of Aluminium.

### 5.4.7 Interstrip resistance $R_{int}$

The interstrip resistance is the resistance between neighbouring strips. High $R_{int}$ (of the order of GΩ) ensures good strip isolation. $R_{int}$ is only measurable with a fully depleted $SiO_2$ interface. It is known that any charge on the surface of the oxide will affect the value of $R_{int}$.

### 5.4.8 Bias resistance $R_{bias}$

The polysilicon bias resistor connects the implant to the bias ring. Due to the thermal noise contribution of the bias resistor, which are known to be proportional to $\sqrt{\frac{kT}{R}}$, a large $R_{bias}$ is needed. But this has a performance compromise as large resistances lead to a large RC time constant. The bias resistors are also expected to have very low variability in their resistance values to avoid non-uniform field distribution among the strips. A picture of a bias resistors in an ATLAS strip detector is shown in Figure 5.13.

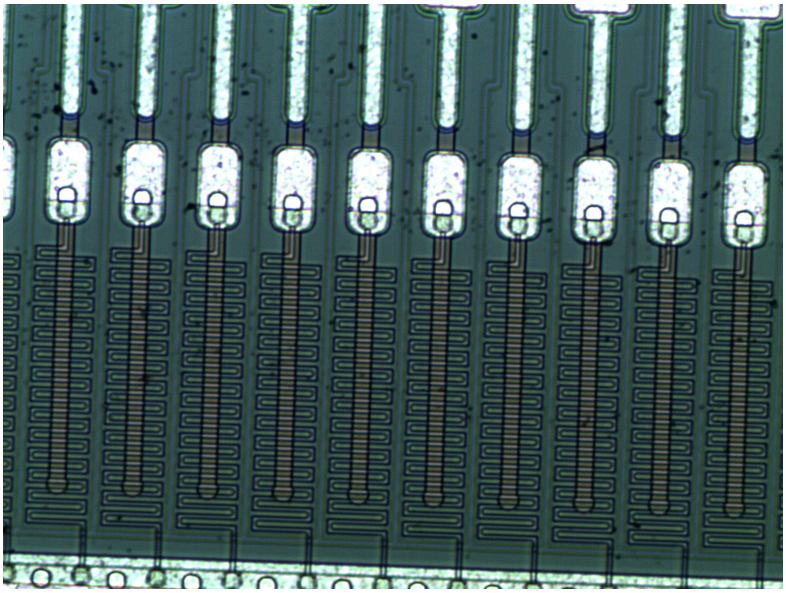


Figure 5.13: An image showing the polysilicon bias resistors connecting the implants to the bias ring.

### 5.4.9 p-stop and p-spray

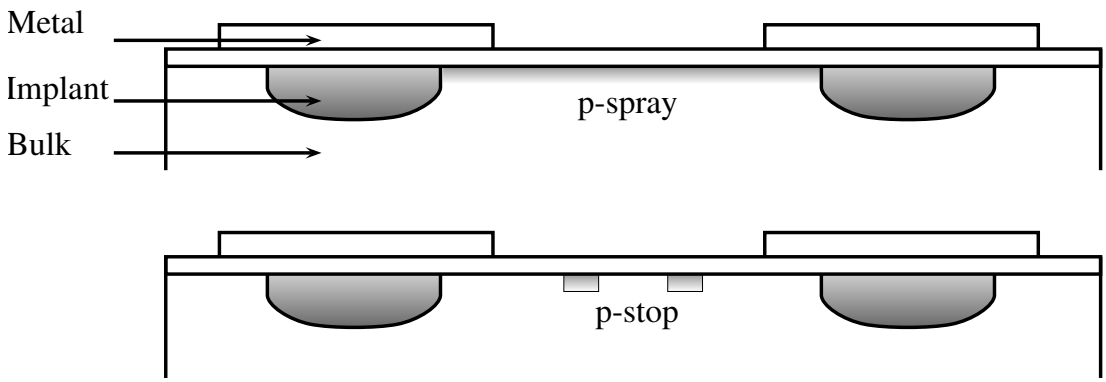



Figure 5.14: An illustration of p-spray and p-stop structures.

Accumulation of fixed positive charges on the $SiO_2$ interface can lead to electrons drifting to the oxide layer, leading to a short circuit. By adding a p+ barrier surrounding the implant (p-stop), it is possible to dissipate the electron accumulation at the oxide interface. Other measures could also be taken such as adding a diffuse layer of p+ (p-spray), which works in a similar fashion to the p-stop. A combination of both is also a common approach. The two structures can are shown in Figure 5.14.

### 5.4.10 Noise contributions

The signal of the traversing charged particle always competes with the sensor's noise. The strength of the signal depends on the thickness of the depletion zone and the average energy-loss rate of the particle. On the other hand, the noise depends on many parameters (design of the detector, operating conditions, readout electronics). The noise is typically measured in terms of the Equivalent Noise Charge (ENC)[4]. The major noise contributors are:

- Leakage current: $I_L$

[4] ENC is the number of electrons contributing to noise

- Strip capacitance: $C_d$
- Parallel and series resistance: $R_p$ & $R_s$

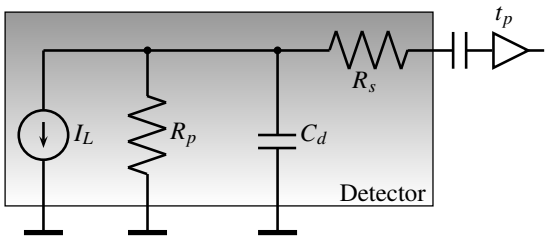



Figure 5.15: The equivalent circuit of a detector showing the noise contributors.

These contributions sum up quadratically:

$$ENC = \sqrt{ENC_{C_d}^2 + ENC_{I_L}^2 + ENC_{R_p}^2 + ENC_{R_s}^2}.$$

The equivalent network of noise contributors is shown in Figure 5.15. All contributions depend on their own resistance and/or capacitance value plus the peaking time of the pre-amplifier.The above four contributions are:

- The leakage current shot noise contribution:

$$ENC_{I_L} = \frac{e}{2}\sqrt{\frac{I_L t_p}{q_e}}.$$

- The parallel resistance thermal noise contribution:

$$ENC_{R_p} = \frac{e}{q_e}\sqrt{\frac{kTt_p}{2R_p}}.$$

- The series resistance thermal noise contribution:

$$ENC_{R_s} = C_d \frac{e}{q_e} \sqrt{\frac{kTR_s}{6t_p}}.$$

- And the most significant contribution:

$$ENC_{C_d} = a + bC_d,$$

where $e$ is the Euler number, $k$ is the Boltzmann constant, $T$ is the temperature in K, $t_p$ is the peaking or integration time, $a$ and $b$ are constants given by the pre-amplifier design. Short integration times usually lead to large values of a and b. e.g

$$\text{for } t_p = 1\,\mu\text{s} \qquad a \approx 160\,e \text{ and } b = 12\,e/\text{pF}.$$

Due to the high bunch crossing rate at the LHC and the need for a short integration time, the noise for the strip detectors at the LHC is mostly dominated by $ENC_{C_d}$. In general, to minimize the overall ENC, the following design constraints need to be met

1. Small $R_s$ (the strip resistance).
2. Large $R_p$.
3. Low $I_L$.
4. Small $C_d$ (shorter strips).

## 5.5 ATLAS strip sensor design

The ATLAS upgrade strip sensor has been through many design iterations, starting with the current ATLAS p-in-n sensor to the upgrade n-in-p sensor. Due to the irradiation of the cur-

rent operational p-in-n sensors and their interaction with hadrons (pions, protons, neutrons, etc) acceptor impurities were added to the silicon bulk mutating it from n-type to p-type, which affected the performance of the sensor. Having a n-in-p sensor is firstly cost-effective, secondly more radiation tolerant and lastly provides faster charge collection, since electrons are being collected. This section describes the ATLAS07 and ATLAS12 sensors. They are n-in-p single sided, AC-coupled sensors with implants biased through polysilicon resistors. The sensors are used in the development and prototyping of the HL-LHC ATLAS strip tracker. The sensors are manufactured from a floating-zone (FZ)[36] 6" wafer. To accommodate 10 readout ASICS (the number of readout ASICS on a hybrid) with 128 channels, the strip pitch becomes 74.5 μm. A corner picture of the mini ATLAS07 sensor is shown in Figure 5.16.

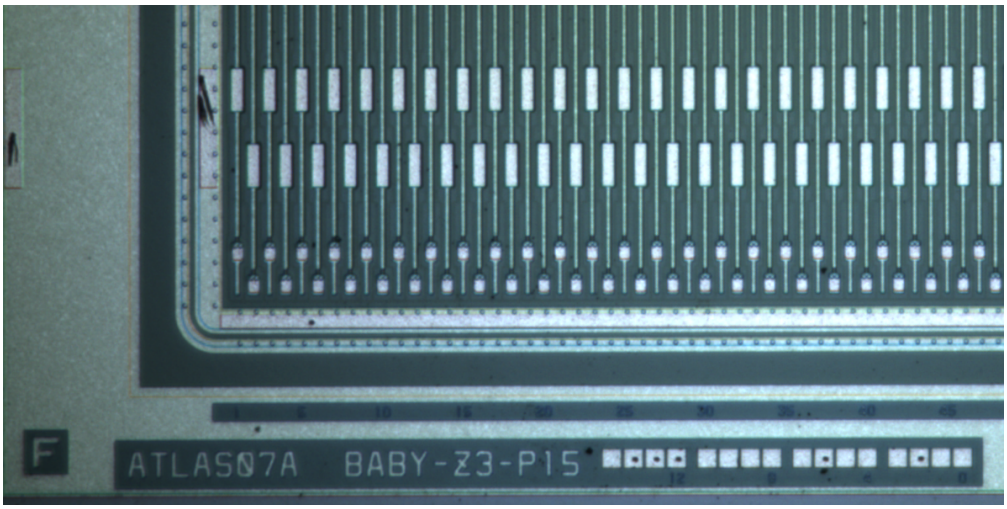



Figure 5.16: The lower left corner of an ATLAS mini sensor.

The new sensors employ a variety of p-stop and p-spray configurations (see Figure 5.17). The p-stop structure, which acts as a barrier interrupting the charge accumulation at the Si-$SO_2$ interface, will give different performance and electric field configurations. The mini sensors have different structures and they have been experimentally tested (pre- and post- irradiation) to

compare them with simulation[37]. Figure 5.18 is an image captured with a microscope showing the p-stop structure of an ATLAS07 mini sensor.

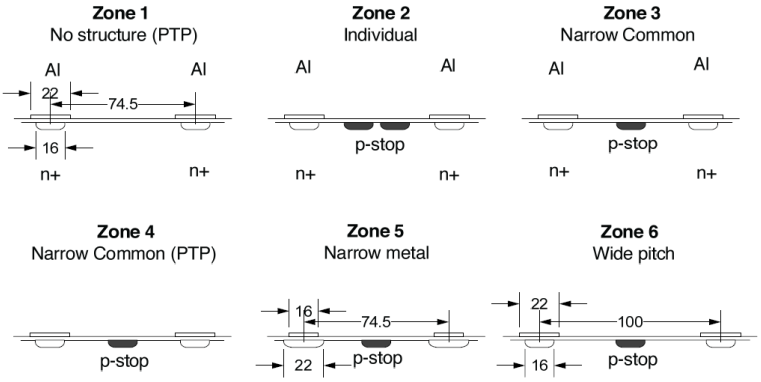



Figure 5.17: The different types of mini ATLAS07 sensors[38]

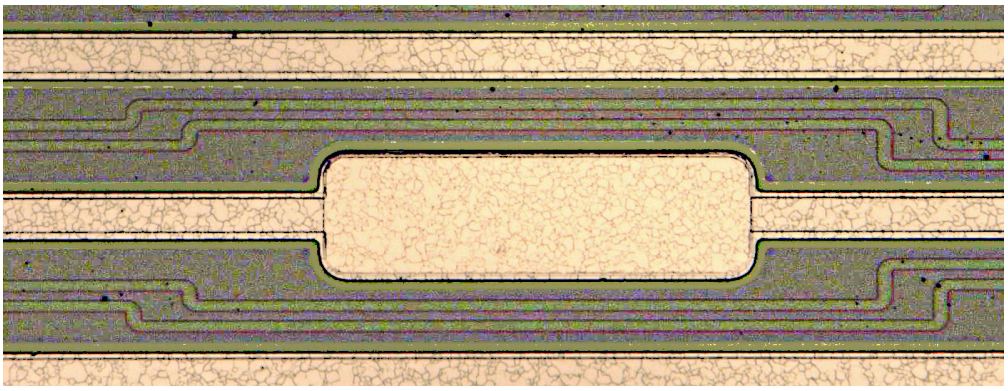


Figure 5.18: A metal strip pad surrounded by the p-stop barriers.

### 5.5.1 ATLAS07 & ATLAS12

The ATLAS07 and ATLAS12 sensors were designed to be large-area for prototyping purposes and to test the effects of radiation on the sensor. The first supply of sensors of the ATLAS07 design was in 2008. This pre-series was a batch of 12 wafers which were used to ensure that

the manufacturer complied with the technical requirements. ATLAS07 was followed by ATLAS12 in 2013 which was the second pre-series batch with modified requirements based on the R&D undertaken on the ATLAS07 sensors. The specifications for the ATLAS07 and ATLAS12 sensors can be found in [38] and [39].

### 5.5.2 Punch-through protection PTP

In AC-coupled strip sensors, the charge accumulated between the strip and implant is collected through the metal strip. If the LHC beam hits one of the accelerator components then a large number of particle can enter the tracking volume. The so-called beam-splash results in a large amount of charge being deposited in the sensor and accumulated at the oxide layer. Therefore, protection is needed to provide an alternative path for the excess charge to ground. The Punch-through protection (PTP) is simply a low resistance path parallel to the bias resistor and is activated when the voltage across the coupling capacitance (oxide) exceeds a sensor dependant value. A simple PTP is usually achieved by extending the implant strip as close as 5 μm to the bias ring. The ATLAS12 PTP structure is shown in Figure 5.19. Other novel PTP gated structures also exist [40].

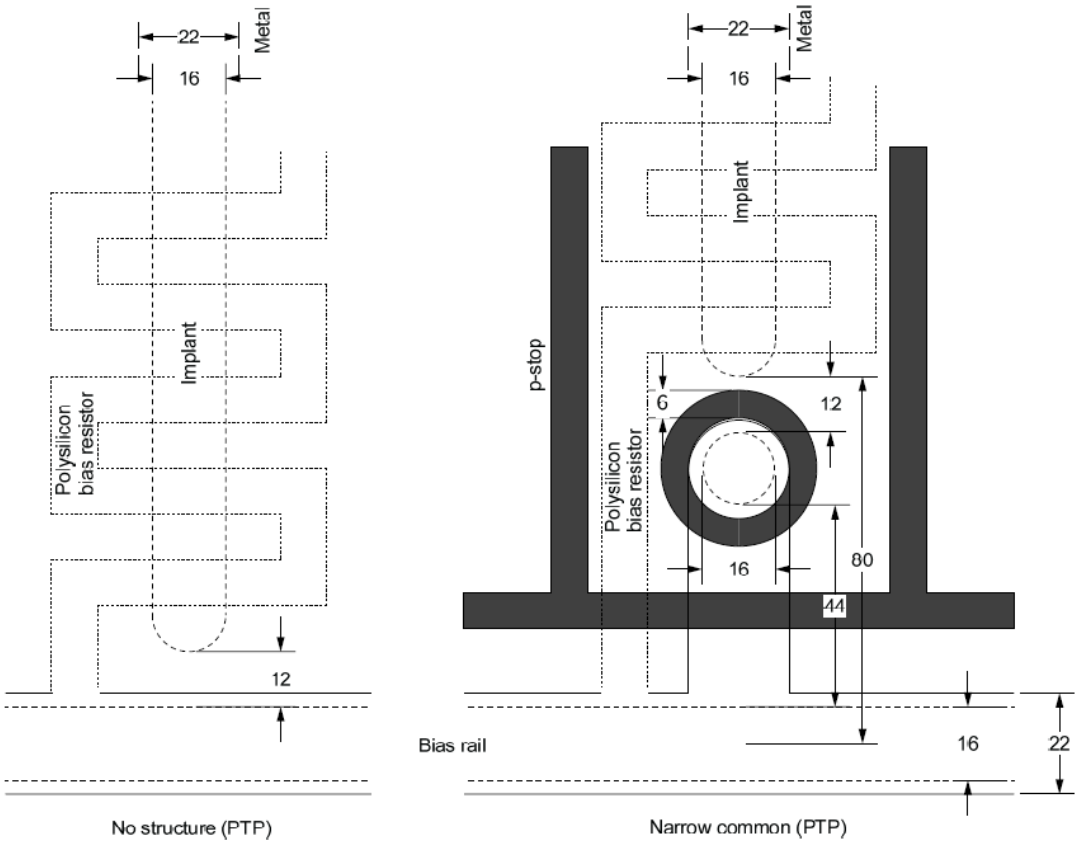



Figure 5.19: The punch through protection structure. The schematic on the right shows the bias rail extended to be around 12 µm away from the implant which facilitate the PTP functionality[39].

# 6 Laser Charge Injection Tests

The close proximity of the detector to the interaction point may subject its components to damage in the event of an accidental beam loss. The sensors are designed to detect single Minimum Ionising Particles (MIPs). The absorption of radiation due to a beam loss can be equivalent to $\sim 10^6$ MIPs per strip per bunch crossing, thus it is important to experimentally verify and properly evaluate the operational limits of the sensors. A laser can inject charges into a sensor ranging from a few MIPs to $10^8$ MIPs (see Section 5.3.2). The laser tests described in this section are used to investigate the electric field behaviour within the layers of the strip sensor, mainly between the metal strip and implant. The tests have shown that the breakdown of the electric field between the metal and implant can result in damage to the sensor. An electrical model of the strip sensor has also been created to help with simulating the electric potentials between the different layers of the sensor and to estimate the absorption efficiency of the sensor. Values obtained from such tests can also be used in conjunction with beam-loss simulations to define the protection requirements for the upgrade strip system.

## 6.1 Electrical Measurements

The electrical parameters, described in Section 5.4, are essential for testing and modelling the sensors. These parameters can also help define the operational limits of the sensors. Specifically

for our case, it is important to determine the maximum injected charge the sensor and readout ASIC can absorb before damage or failure occurs. The following section describes how each parameter has been measured.

### 6.1.1 Measurements

- Current-Voltage Measurements (IV Curve)

  This is a basic check of sensor quality. The mini sensor is placed in a probe station with a controlled voltage source with its low and high terminals connected to the bias ring and the backplane, respectively. The voltage is varied from 0 to 600 V in steps of 20 V every 10 s and the current and temperature are recorded.

- Capacitance-Voltage Measurements (CV Curve)

  A CV meter's AC input is connected to the bias ring and the voltage output to the backplane using probe needles, whilst biasing the sensor with the voltage source. The voltage is varied as in the IV measurements and the capacitance is measured. The values are plotted as $1/C^2$ vs. the bias voltage. For a sensor behaving as expected, the plot should have a linear and an asymptotic region. The transition between the two regions happens at the full depletion voltage.

- Coupling Capacitance

  The coupling capacitance between a metal strip and the implant is measured using a CV meter. The metal pad is probed with a needle and connected to the AC input of the CV meter. The implant pad is also probed and connected to the voltage output of the CV meter. The capacitance is measured at 1kHz with resistance set to parallel[1].

[1] The AC method of capacitance measurement is described in detail in A.2.

- Interstrip Capacitance

  Using a CV meter and a voltage source, the voltage source is first connected as described in the IV measurement. Three neighbouring metal strips are used: the centre strip connects to the AC input of the CV meter and the two neighbouring strips connect to the voltage output of the CV meter. The measurement is done with a bias voltage of 200 V, at a frequency of 100 kHz and resistance set to parallel.

- Implant and Metal Resistance

  This test only requires an ohmmeter. The implant or metal strip is probed with a needle on two pads at either side of the sensor and the resistance at the full length of the strip is measured. The resistance is read through an ohmmeter and the distance between the two pads is recorded.

### 6.1.2 Results

The IV plots are used to determine the quality of the sensor. By looking at the leakage current of three ATLAS07 mini sensors (Figure 6.1) it can be seen that sensor W33 shows the best behaviour and it was therefore selected for the laser tests. The depletion voltage and bulk capacitance can be derived from the CV plot in Figure 6.2. The depletion voltage is recorded at $218 \pm 0.2$ V and the bulk capacitance of the sensor at full depletion is determined to be $26 \pm 0.03$ pF.

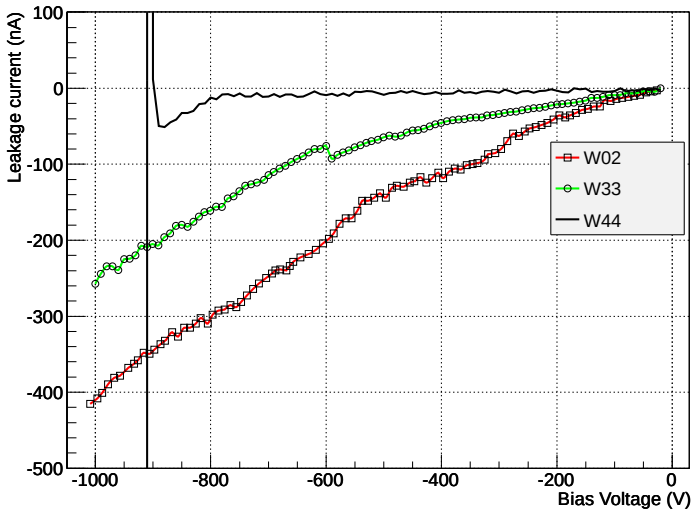



Figure 6.1: The IV plots for three different mini sensors. W44 shows an early breakdown at ~900 V. W33 shows a reasonable leakage current with no breakdowns.

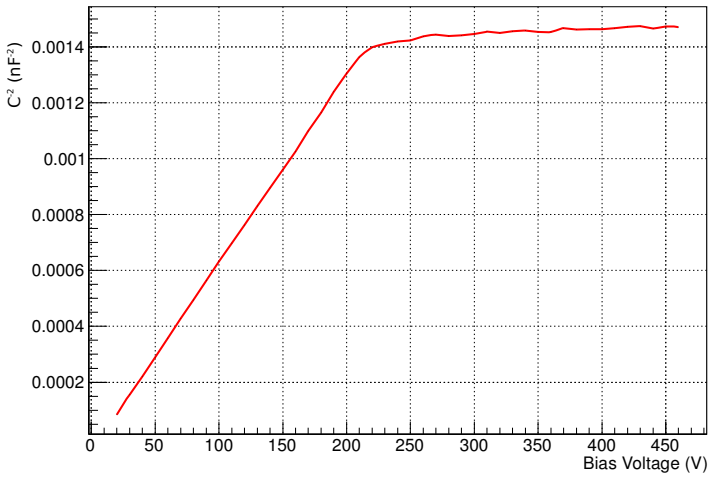



Figure 6.2: The measurement of the sensor's capacitance plotted as $\frac{1}{C^2}$ against bias voltage. The full depletion voltage is ~230 V, this is at the transition region when the plot starts to flatten (i.e. the sensor is fully depleted and the capacitance is no longer changing)

Table 6.1 lists the properties of the ATLAS07 W33 mini sensor and the recently delivered ATLAS12 mini sensor.

| **Description** | **ATLAS07 (W33)** | **ATLAS12** |
|---|---|---|
| Metal (Al) Resistance | 15 ± 0.01 Ω | 15 ± 0.01 Ω |
| Implant Resistance | 15 ± 0.3 kΩ | 20 ± 0.4 kΩ |
| Coupling Capacitance between metal and implant | 20 ± 0.15 pF | 24 ± 0.2 pF |
| Implant length | 7.5 mm | 7.5 mm |
| Metal length | 7.34 mm | 7.34 mm |

Table 6.1: The ATLAS mini sensor measurements.

## 6.2 Sensor Simulation

Simulating silicon sensors can provide an insight into the sensor's behaviour especially when a large amount of charge is injected into it. There are a few ways to model such behaviour with the simplest being an electrical circuit simulation using a tool such as SPICE[2]. A failure of a sensor is generally caused by the generation of electric fields that are too large to be maintained within the sensors. Once the electric field can no longer be sustained, it breaks down and the generated charge carriers flow freely through the sensor until they have all been cleared. The electric fields are due to the potential differences between the different layers of the sensor and can be calculated with SPICE. This allows a model of the electric field as a function of the injected charge to be developed.

### 6.2.1 Strip sensor electrical model

The diffusive line property of a silicon strip detector is modelled as a simple one dimensional RC line with a homogeneous distribution of discrete resistances and capacitances. The strips are

[2] Simulation Program with Integrated Circuit Emphasis

divided into discrete portions with each portion adding resistance and capacitance to the entire model. Figure 6.3 is a schematic of the electric model of a sensor.

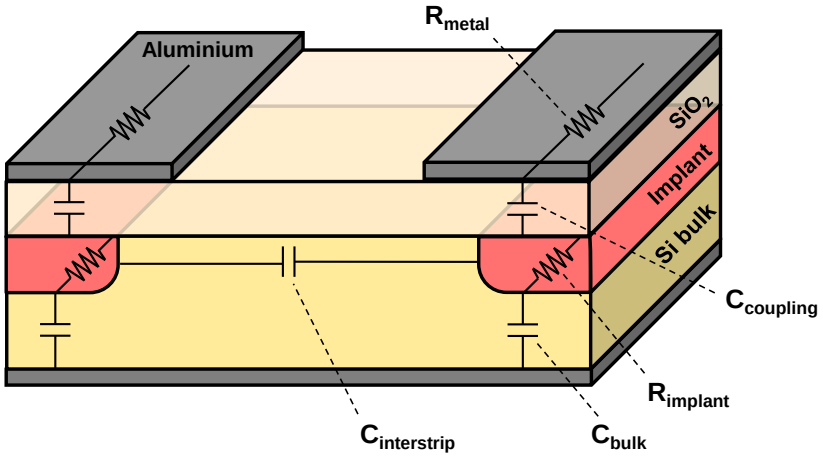



Figure 6.3: An electrical model of the strip sensor as represented in SPICE. The sensor is modelled in discrete portions with every portion adding some resistance and capacitance to the entire model. This particular illustration shows two short strips with resistances along the strips and capacitances between the layers and the neighbouring strip.

### 6.2.2 Punch Through Protection (PTP) model

Two measurements of the PTP were performed. The first, a DC measurement, was done at the bias resistor end, the "near end", and the second measurement was recorded using the strip contact furthest away from the bias resistor, the "far end". In both measurements, an IV curve was recorded across the bias resistor, with the voltage increasing from 0 V to 20 V, in 0.4 V steps. The ground connections of the PTP test supply were tied to the ground of the bias supply close to the detector.

The calculated resistance of the PTP from the IV recorded values can be seen in Figure 6.4. The difference between the "far end" and "near end" plots is due to the strip resistance. The plot clearly shows the point at which the PTP is activated. Below 15.5 V, the measured resistance

was about 1.5 MΩ. Above 15.5 V, there is a sharp drop in resistance. It is also important to note that the measured values are of the effective parallel resistance of the PTP and bias resistor.

To model the PTP in SPICE, the two measurements were fitted to the following formula:

$$R_{PTP} = \begin{cases} R_{bias} & V_{PTP} \leq 15.5V \\ \left(e^{-\frac{1}{2}\left(\frac{V_{PTP}+P_1}{P_2}\right)^2}\right) \times 10^{14} & V_{PTP} > 15.5V. \end{cases} \tag{6.1}$$

$P_1$ and $P_2$ were determined to be 39.8 ± 0.025 and 9.2 ± 0.033, respectively.

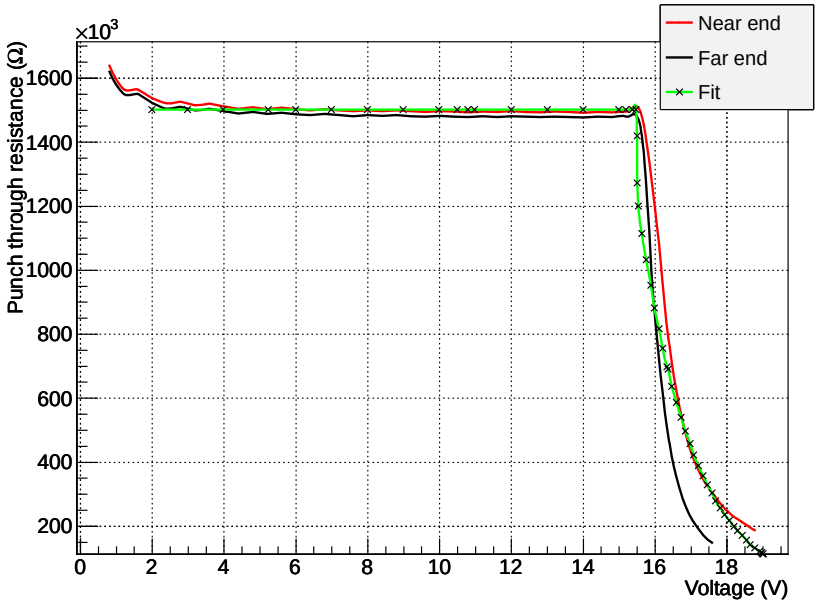



Figure 6.4: The DC PTP fit plot. The resistance value of the PTP was measured from the pad near the PTP and another measurement from the pad on the other side of the sensor. The PTP is activated when the voltage across it exceeds ~15.5 V. The higher resistance at $V_{PTP} < 2\,V$ is not related to the PTP and is due to a measurement error. A fit was calculated for the measurements.

### 6.2.3 SPICE

The entire sensor was modelled with blocks of RC circuits as shown in Figure 6.3. Using LTSpice, the RC circuit blocks were added together to create a sensor with a defined length and number of strips. The full circuit is illustrated in Figure 6.5. Charge injection is driven by a current source where the charge is the integral of the current pulse over time. The number of MIPs can then be derived using the formula

$$\text{Number of MIPs} = \frac{\text{Charge Injected}}{e \times \text{\#e-h pairs per MIP}}.$$

The number of e-h pairs per MIP is calculated to be 23700 for a 300µm thick sensor[3].

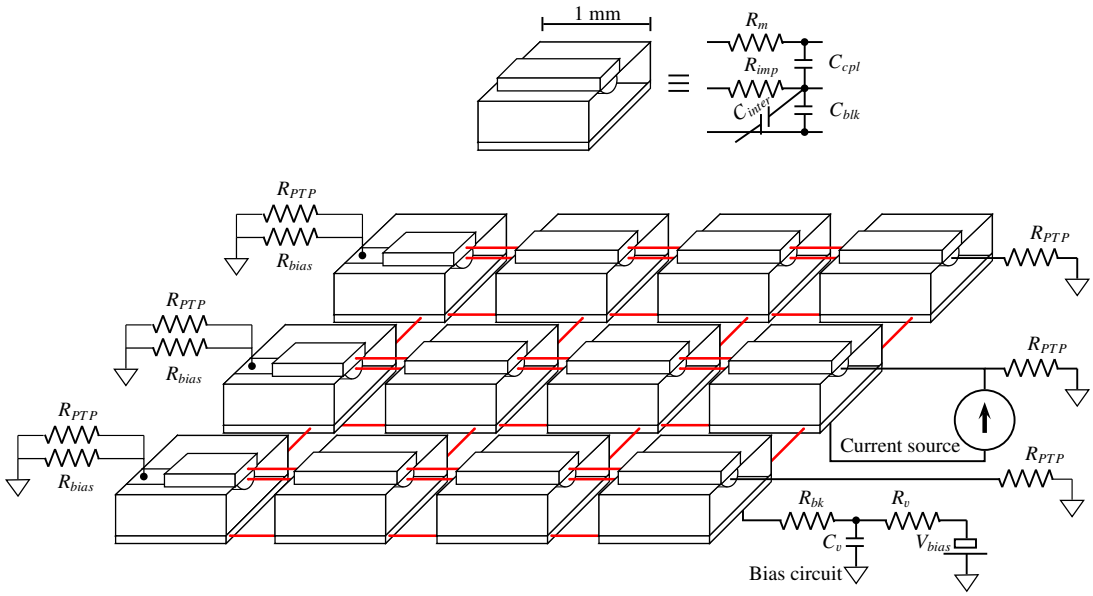



Figure 6.5: The full electrical circuit of a sensor with three 4 mm strips.

When the sensor is fully depleted ($V_{bias} \geq V_{fd}$) the efficiency of the charge collection is highest. When a large charge is injected to the sensor the potential difference across the bulk

[3] For Silicon, 1 MIP produces 79 e-h pairs per 1 µm

(i.e. the biasing voltage) is expected to be disturbed. The relationship between the depletion width, the bias voltage and the full depletion voltage[41] can be expressed as

$$d = D\sqrt{\frac{V_{bias}}{V_{fd}}} \text{ for } 0 < V_{bias} < V_{fd}.$$

where $d$ is the depletion-zone width, $D$ is the full depletion width, $V_{bias}$ is the bias voltage and $V_{fd}$ is the full depletion voltage, respectively. When the depletion-zone width decreases the charge collection efficiency degrades. The relationship, derived from the equation above, is illustrated in Figure 6.6.

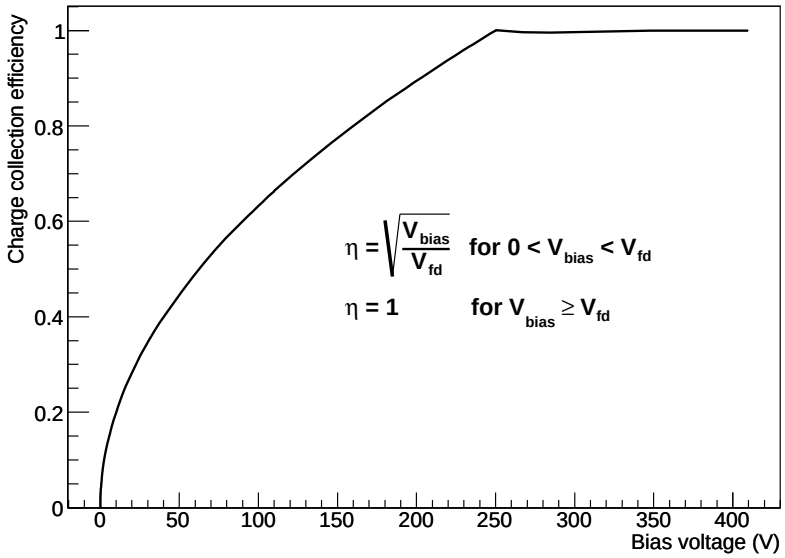
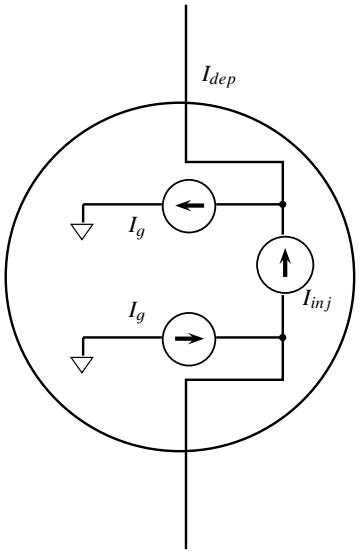



Figure 6.6: The relationship between charge collection efficiency and bias voltage. In this plot, the full depletion voltage $V_{fd}$ is assumed to be 250 V.

To model the efficiency behaviour, the current source has to be modified to monitor the voltage between the implant and backplane and adjust the current accordingly. This is illustrated in Figure 6.7.




$$I_{dep} = I_{inj} - I_g \qquad \text{for } V_{bias} < V_{fd}$$
$$I_{dep} = I_{inj} \qquad \text{for } V_{bias} \geq V_{fd}$$

$$I_g = I_{inj} - I_{inj}\sqrt{\frac{V_{bias}}{V_{fd}}}$$

Figure 6.7: A schematic of the current source. The two extra current sources ($I_g$) adjust the output of the current source to simulate the effect of the depletion zone width.

| Component | Description | Value |
|---|---|---|
| $R_m$ | Metal (Al) resistance | 15 Ω / cm |
| $R_{imp}$ | Implant resistance | 20 kΩ / cm |
| $C_{inter}$ | Inter strip capacitance | 25 pF / cm |
| $C_{cpl}$ | Coupling capacitance | 25 pF / cm |
| $C_{blk}$ | Bulk capacitance | 2.5 pF / cm |
| $R_{bias}$ | Bias resistance | 1.25 MΩ |
| $R_{bk}$ | Backplane resistance | 10 Ω |
| $R_v$ | Bias voltage circuit resistance | 5.1 kΩ |
| $C_v$ | Bias voltage circuit capacitance | 50 nF |
| $R_{PTP}$ | PTP resistance | Refer to equation 6.1 |

Table 6.2: The sensor's SPICE schematic component list.

The sensor's SPICE model also includes a circuit for the power supply that consists of a DC voltage source, a capacitor, a resistor and a current limiting diode. The power supply provides a biasing voltage to the sensor through the backplane. Each strip is also connected to a bias resistor and two PTP resistors on each side. The typical component values are shown in Table 6.2. The simulation results are represented and compared to the real measurement results in

section 6.5.3.

## 6.3 Laser charge injection setup

### 6.3.1 Sensor readout board

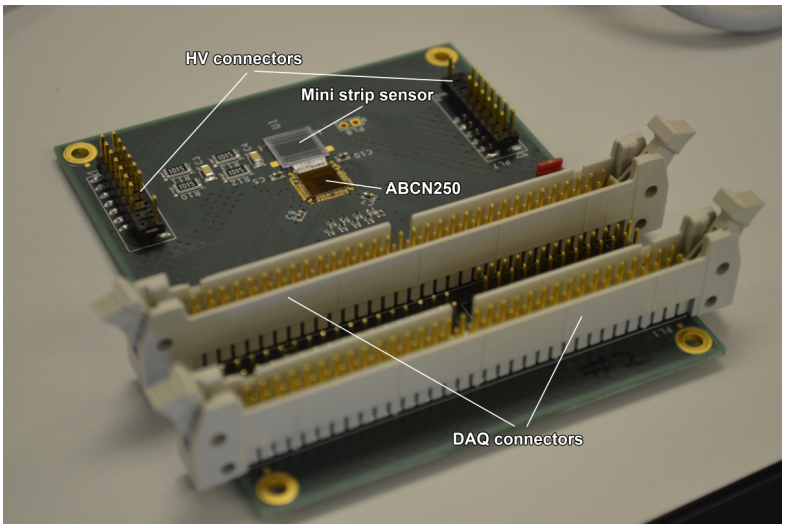



Figure 6.8: The mini sensor readout board with an ABCN250 chip.

An ATLAS mini strip sensor was glued and wirebonded to an ABCN250 chip on a board that was previously used to test the ABCN250 readout chips. The board provides high voltage pins for biasing the sensor and also 2 large connectors that connect the IO pins on the ABCN250 to an external readout board. The readout board incorporates an FPGA which facilitates the mapping of the IO pins from the ASIC to commercial off-the-shelf hardware from National Instruments. The hardware is then interfaced with the SCTDAQ[65] software that was used in the early tests of the ABCN250 chip. The software allows us to evaluate every channel on the ABCN250 chip by measuring the input noise. It is expected that a damaged channel/strip would have a substantial increase in noise compared to the good channels.

### 6.3.2 Laser machine

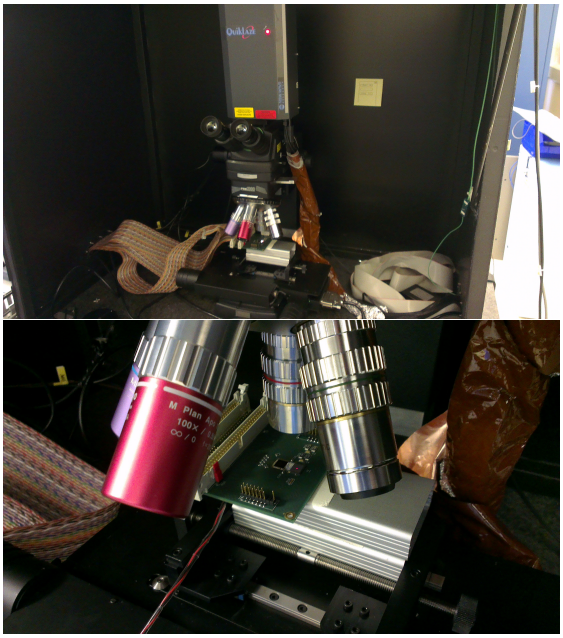


Figure 6.9: The laser set-up showing the laser head and the DAQ board. The laser system has a built-in microscope camera which helps guide the laser through the strips.

A high energy laser machine, such as the one shown in Figure 6.9, is commonly used as a semiconductor repair tool. It is equipped with three laser heads with a wavelength of 1064 nm. The infrared laser simulates the passage of charged particles through the sensor and can produce pulses with energies ranging from 1 nJ to 50 μJ, equivalent to ~$10^9$ MIPs to ~$10^{14}$ MIPs. The lower energy limit can also be minimized down to a few MIPs with the use of NDA[4] filters. The optics on the laser head are capable of focusing the laser down to 2 μm. The charge injection capability of the laser relies on the photon absorption at the sensor. However, reflection also needs to be accounted for as previous studies[42] have shown that charge injection via a laser results in only ~50% of light being absorbed.

[4] Absorptive Neutral Density

The QuikLaze-50ST laser system from New Wave Research produces 4 ns pulses at a maximum frequency of 50 Hz.

## 6.4 Effects of large charge dosage on the sensor

### 6.4.1 Test procedure

A laser was aimed at a biased sensor with an aperture size small enough to fit between two strips. After calibrating the laser head, the laser energy was set to 560 nJ and 100 shots were burst into the sensor. A 3-point-gain[5] scan was run after every burst. If the scan did not report any increase in noise, in any of the channels, then the energy of the laser is increased and the process is repeated. When the scan reports a noise increase the sensor is examined under a microscope for any surface damage.

### 6.4.2 Sensor Damage

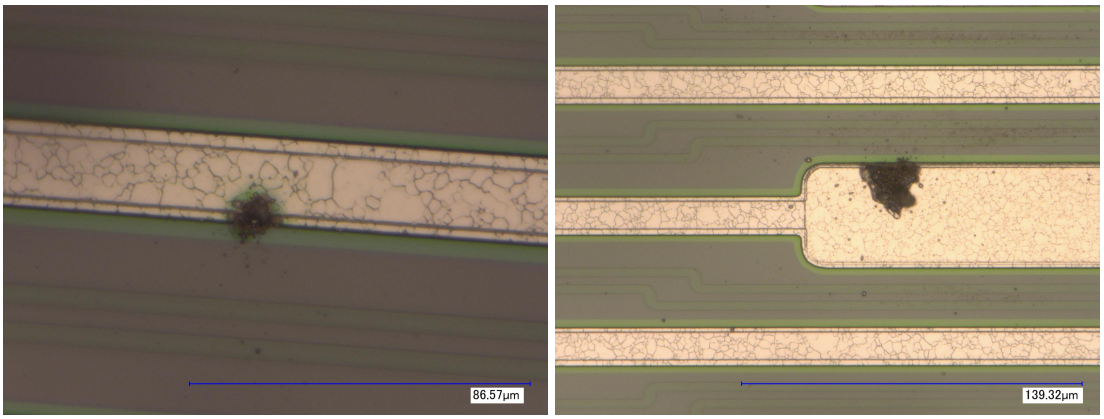



Figure 6.10: The damage on the metal strip due to a large amounts of charge injected into the sensor. Left: damage on the strip track. Right: damage on the bond pad.

[5] 3-point-gain scans are described in Section 9.2.5

The tests were initially setup to determine the failure point of the readout ASIC due to larges charges. However damage on the sensor was observed first and inspected with a microscope. The microscope images showed clear damage to the strips that were reporting high noise. Examples of the damage can be seen in Figure 6.10. These two images show the two kinds of damage seen on the strip and bond pad. In some cases, debris was also seen around the damage point.

The damage also created a substantial increase in leakage current. In most cases, the damage also caused a short-circuit between the metal and the backplane. The short-circuit was removed by disconnecting the wirebond of the channel. It was also observed that by disconnecting the channel, the noise migrates to the neighbouring strips creating what has become known as the "Fuji" effect (the noise channel occupancy now resembles the crater of a volcano). Cutting the wirebonds of these now-noisy neighbouring strips also further migrated the noise. The deterioration of the leakage current over the period of the tests can be seen in Figure 6.11.

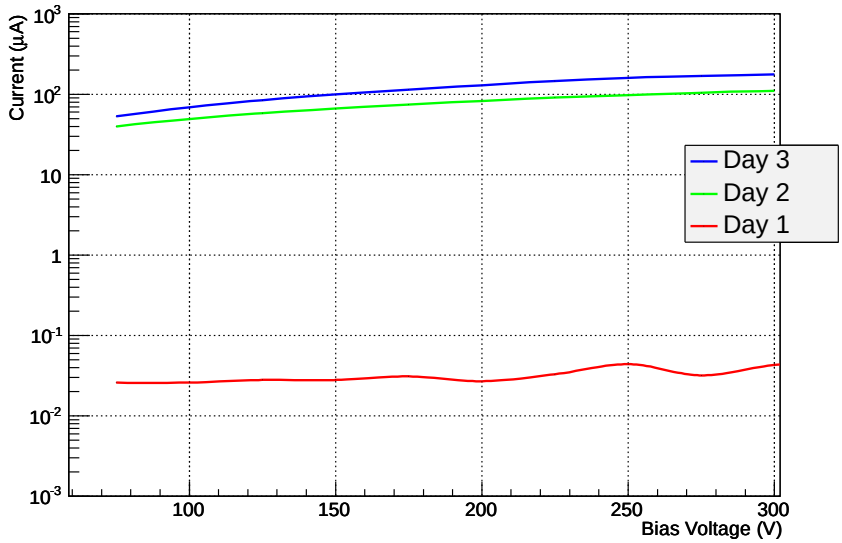



Figure 6.11: The IV measurements of a single sensor during the three days of testing. Note the increase in leakage current due to the damage to the sensor at the end of day one.

A very important observation with regard to the position of the damage is that it always appeared away from where the laser was impacting the sensor's surface. This confirms that the damage was not due to thermal burning, and since the damage appears at random places, that the damage occurs where the electric field breaks. On strips where no damage appeared, the PTP structure has most probably been activated thus creating a path for the excess charge.

## 6.5 Electric field measurements

After observing the sensor damage caused by the large-charge injection, the electric field between the metal strip and implant was monitored. The PTP is responsible for draining the accumulated charge between the strip and the metal. When the PTP fails to promptly drain the charge, an electric field breakdown occurs which causes damage to the sensor. This measurement will help understand the relationship between the injected charge and the electric field across the coupling capacitor, which could define the maximum potential difference the sensor can maintain before damage: a value which can be essential to the PTP design. The sensor under test is an ATLAS12 mini sensor. It was glued onto the same DAQ board as the previous tests with the ABC250 chip. The sensor was wirebonded to external pads as shown in Figure 6.12. The laser intensity is measured with Joules, to convert this energy into MIPs and then to charge (to be used in simulation) the following equation was used:

$$\text{Number of MIPS} = \frac{\text{Energy of laser pulse}}{\text{\#e-h pairs per MIP} \times \text{Minimum ionization energy} \times e}$$

The minimum ionization energy for photons is 3.62 eV, as discussed in 5.3.2.

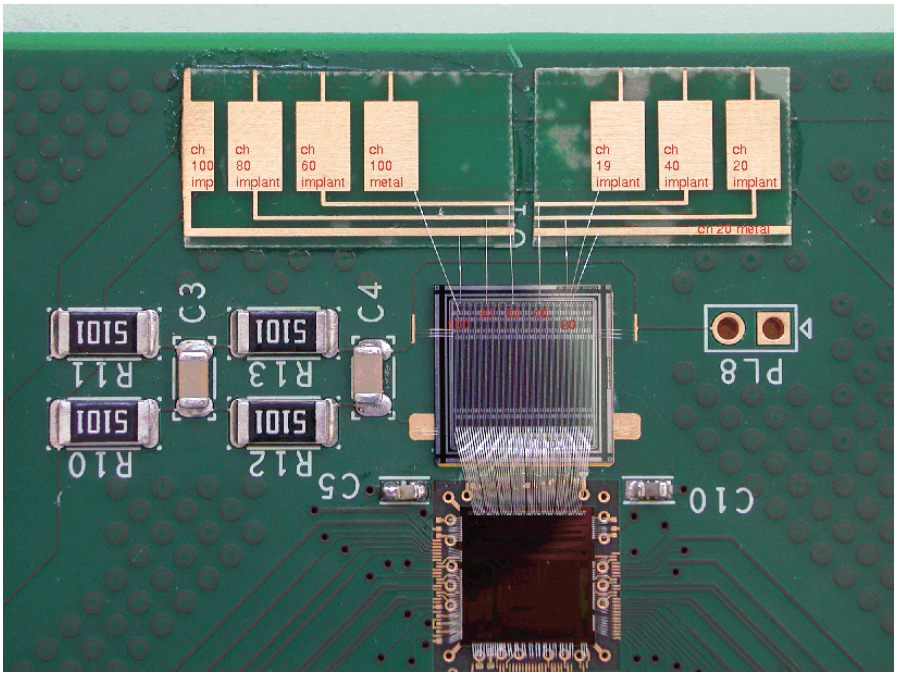



Figure 6.12: A picture of the DAQ board connecting an ABC250 chip (bottom of image) to an ATLAS mini strip sensor.

### 6.5.1 Test procedure

A laser was aimed at a biased sensor as shown in Figure 6.13. The laser was firing continuous shots onto the sensor and the potential difference between the strip and implant near the laser spot was measured. The measurements were done using an active differential probe connected to an oscilloscope. The pulses seen on the oscilloscope are averaged and recorded. The whole process is then repeated with increasing energy.

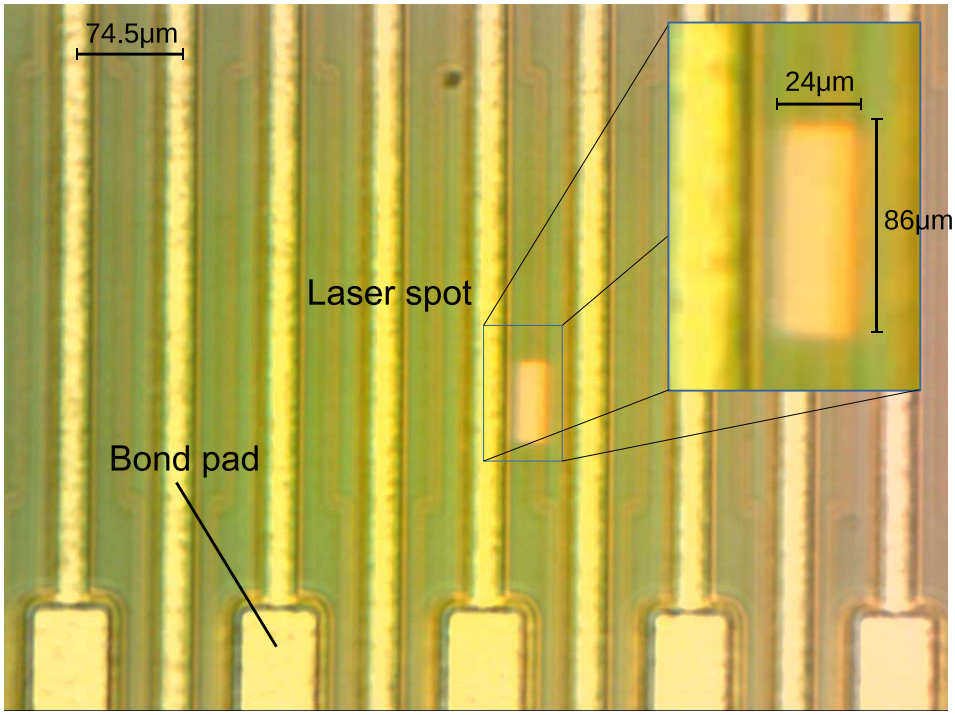



Figure 6.13: A picture obtained from the laser microscope showing the position of the laser spot.

### 6.5.2 Measurement limitations and problems

A number of problems have risen due to the limitation of the available apparatus. These are described here.

#### Laser stability

A laser system controller sets the energy and the aperture size of the laser head. Using a laser power meter, the energy output of the laser was plotted against the attenuation value, Figure 6.14, and shows a non-linear relationship between the attenuation and the output energy. Significant fluctuations were also seen at high power settings.

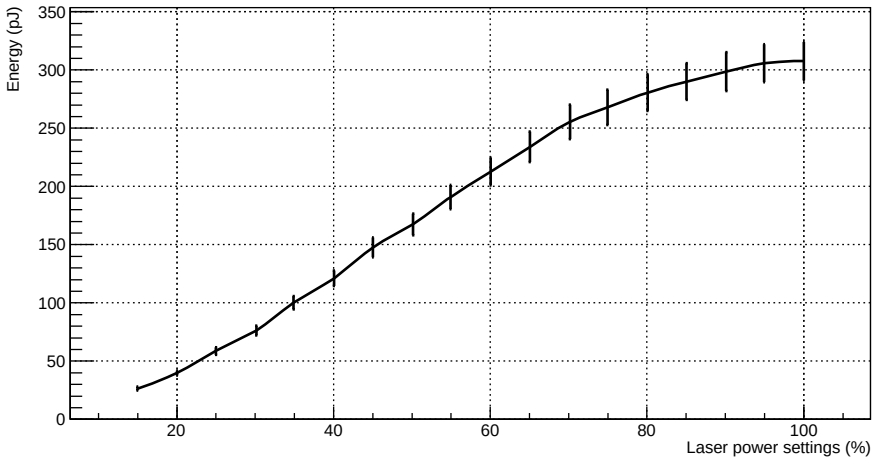



Figure 6.14: A plot of the laser power settings as they were measured by the power meter. An NDA filter with an attenuation of $6 \times 10^{-6}$ was used. The laser was seen to be more stable when the laser power setting is low.

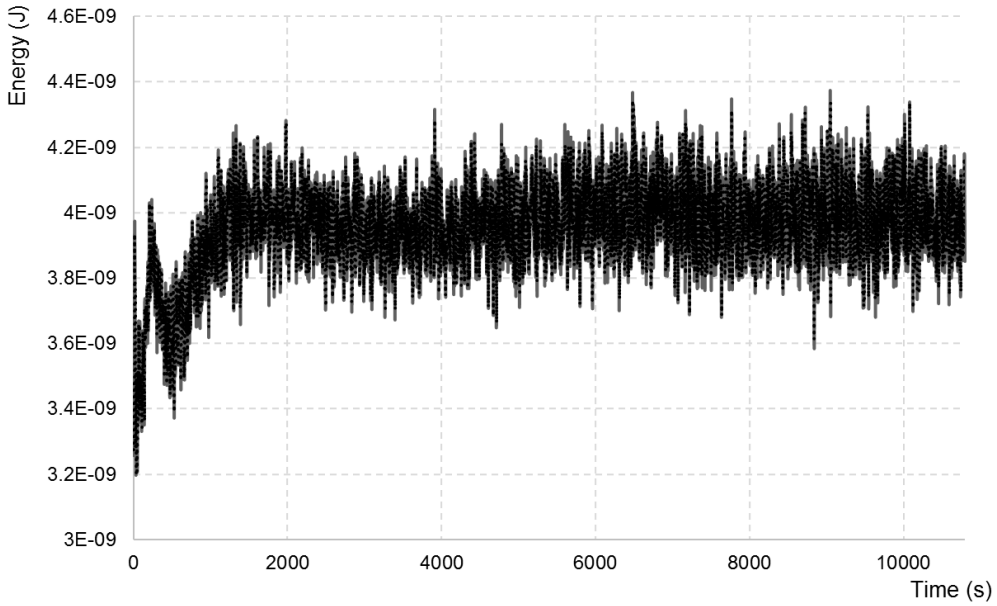



Figure 6.15: A plot showing the energy output of the laser over a duration of three hours. An NDA filter with an attenuation of $8 \times 10^{-5}$ was used and the laser power set to 100%. The laser is seen to become more stable after ~30 minutes.

The laser was also tested for its stability over time. The attenuation was fixed and the laser was fired continuously at the power meter. The test ran for almost three hours and the energy was recorded every few seconds. The plot in Figure 6.15 shows that there is a wide variation in the output over time and the stability was observed to improve after the laser had been running for ~30 minutes.

### Probe loading

Another issue which adversely affected the measured signals was the probe loading. An ideal probe is expected to have: absolute signal fidelity, zero signal source loading and complete noise immunity. The probe used for the measurements (Figure 6.16) had a significant signal loading effect. In order to be able to interpret the results, it was necessary to add this loading into the simulation. The probe load circuit is shown in Figure 6.17.


Figure 6.16: The Pico TA046: 800 MHz, 15 V active differential oscilloscope probe used in the measurements.

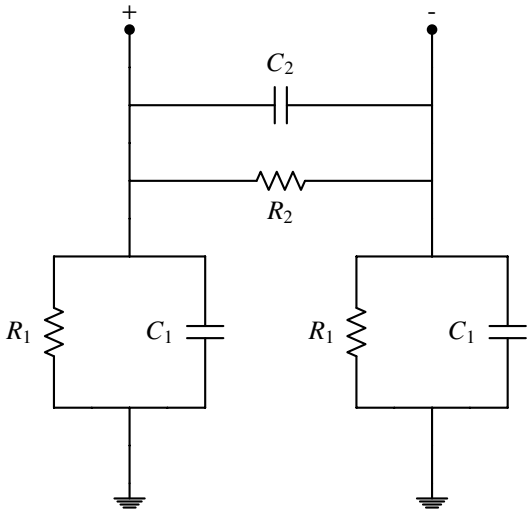



Figure 6.17: The load circuit implemented in the simulation. The values for the TA046 probe are $R_1$ = 10kΩ, $C_1$ = 2pF, $R_2$ = 100kΩ and $C_2$ = 0.1pF.

### 6.5.3 Results

#### Single pulse comparison (Measurement vs. Simulation)

The input to the simulation was a Gaussian current pulse with a width of ~4 ns. This is the width of the laser pulse as measured by a standalone high speed photosensor. The simulated current pulse is shown in Figure 6.18. Once the probe load circuit was introduced, the timing of the signals became closer and the heights were consistent with each other. The simulated and measured pulses are shown in Figure 6.19. The difference in the heights of the pulses can be attributed to the absorption efficiency of the sensor, which will be discussed later.

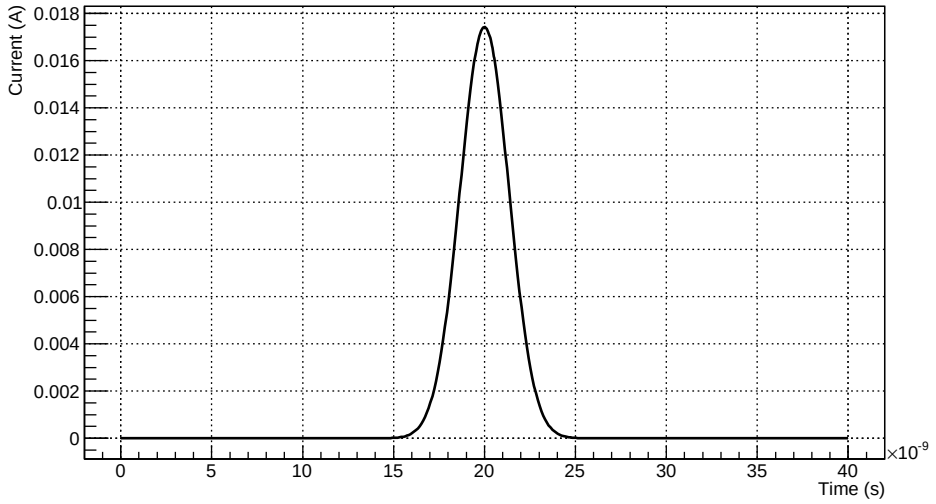



Figure 6.18: The generated (59 pC) Gaussian current pulse in the simulation circuit. The pulse has a width of ~4 ns, similar to the laser pulse.

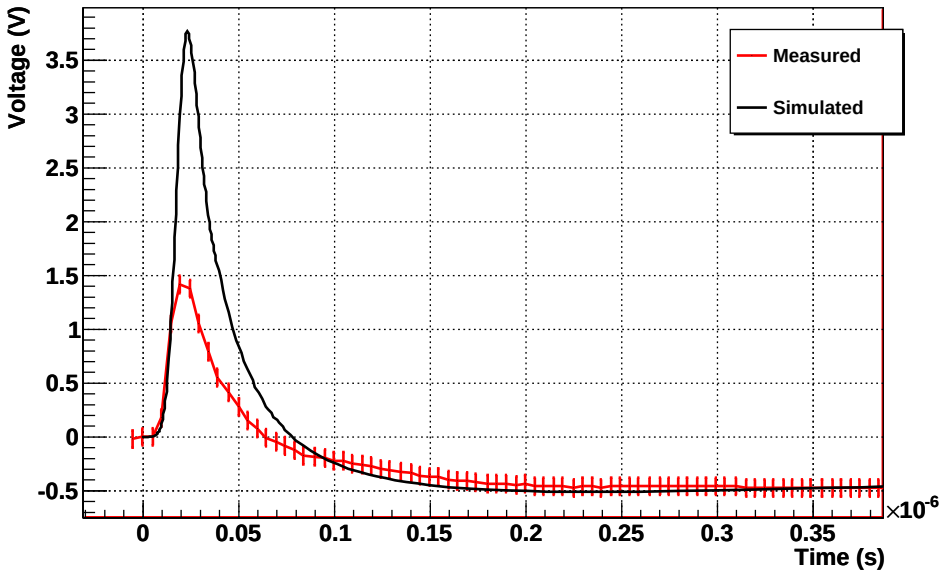



Figure 6.19: The measured and simulated signals between the metal and implant when injecting 59 pC over 4 ns.

### Maximum pulse vs. Energy

In order to further verify the simulation, the laser was set to fire at the sensor at different energies and the potential difference between the metal and implant was measured and compared to the simulation. The difference between the simulation and the measurement can give an insight into the absorption efficiency of the sensor, which will be discussed next.

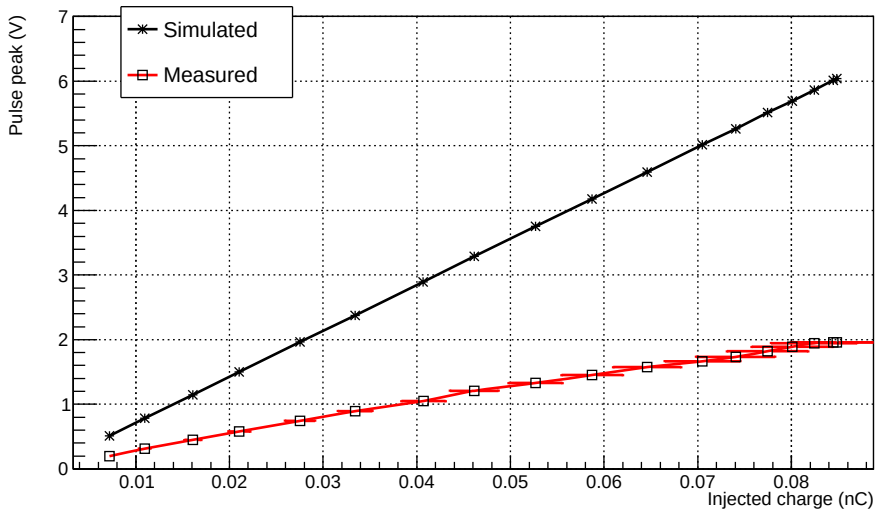



Figure 6.20: The peak voltage of the signal generated between the metal and implant over a range of injected charges. The non-linearity of the measured pulses is due to the non-linearity of the laser that was shown in the plots in Figure 6.14 and 6.15

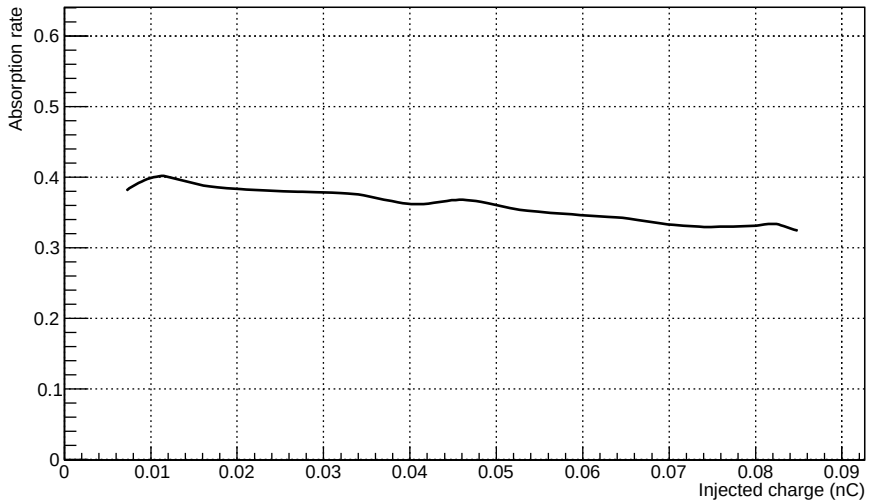



Figure 6.21: The absorption efficiency extracted from Figure 6.20. Absorption rate = Measured / Simulation.

### 6.5.4 Discussion

#### Charge sharing and reflection

The measurements and simulation in Figures 6.20 and 6.21 shows clear evidence that some charge is being lost. The energy (charge) loss is attributed to two factors : charge sharing and reflection.

Due to the refractive index difference between the air and the sensor, some light will be reflected and the remaining absorbed. At normal incident angle, 4.5% of the laser is reflected. The reflection is calculated from the Fresnel reflection equation:

$$R = \left| \frac{n_1 - n_2}{n_1 + n_2} \right|^2 ,$$

where the refractive index for $SiO_2$ ($n_2$) is 1.5341 for a wavelength of 1064 nm and the refractive index for air ($n_1$) is $\approx 1.003$.

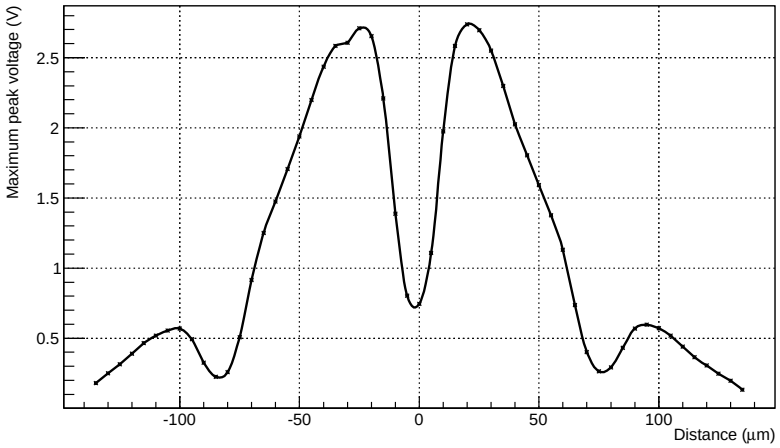



Figure 6.22: The charge distribution between four neighbouring strips. The dips show the position of the metal strips where high reflection occurs. The maximum peak of the signal was recorded from a single strip with the laser moving in 5 μm steps.

The remaining 95.5%, is absorbed and shared among several strips. To create a map of the charge sharing property, the laser was set at a fixed energy and was moved across the strips in 5 μm steps. The signal was measured from the same strip and the maximum pulse peak was recorded at every step. The measured values are shown in Figure 6.22. The dips in the plot indicate the position of the metal strips, where almost all of the laser is reflected. It also shows that when the laser is firing between two strips, these two strips collect 40.5% of the signal each and the next neighbouring strips collect and equally share the remaining 19%. Therefore, the absorption efficiency for one strip is:

$$95.5\% \times 40.5\% = 39.5\% \quad ,$$

Agreeing with that shown in Figure 6.21.

### Signal timing and further work

The simulation results presented here are based on electrical values (resistances and capacitances) of one ATLAS12 mini sensor but the measurements were made on a different ATLAS12 mini sensor. The simulated and measured signals are different as can be seen from Figure 6.20. The height of the pulse is not affected by the probe, but the timing and shape of the pulse is. Ultimately a bespoke system has to be built to measure the fast pulses coming from the sensor. Having such a setup would not only obtain the proper timings of the signals and verify the RC values of the sensor but would also help with evaluating PTP behaviour and limitations.

# 7 Strip Tracker LV Powering Schemes

## 7.1 Introduction

The current ATLAS SCT has 4088 modules serviced with individual electric cables delivering both high and low voltages. In the ATLAS upgrade, the strip tracker is expected to have a substantial increase in the number of modules to around 18,000. There is however insufficient space within the detector to accommodate more power cables. For this reason, more powering schemes that serve multiple modules with a single cable must be developed. Two fundamentally different powering schemes have been considered for the strip tracker and development of both continues as of this publication. The first option, DC-DC powering, delivers the power via a voltage bus to a DC-DC buck converter on every module. A single powering cable carries a fixed low voltage and a high current. The second proposed scheme, serial powering, provides a constant low current but with a high voltage that is equal to the sum of the voltages required to power every module. The modules and hybrids are designed to work with both schemes as it is still unknown which powering scheme will be used; pending R&D work to validate the different schemes. These schemes are, however, only concerned with delivering the LV power to the module itself. It is assumed that the powering within the module for the ABCN130 readout chips will only have one option where the chips are all at the same potential.

The ABCN130 requires 1.2 V to power both its digital and analogue parts. Where it is customary

for the digital part to have a lower voltage, tests have shown higher SEU sensitivity at voltages lower than 1.2 V[51]. The delivery of the 1.2 V to the functional parts of the chip can be done in two ways; the powering schemes could either deliver 1.2 V directly to the chip or deliver 1.3 V where an on-chip Low voltage Drop Out (LDO) regulator will drop the 1.3 V to a stable, ripple free 1.2 V source. The LDOs are externally controlled and their use will be tested during system development.

The different powering schemes are shown schematically in Figure 7.1.

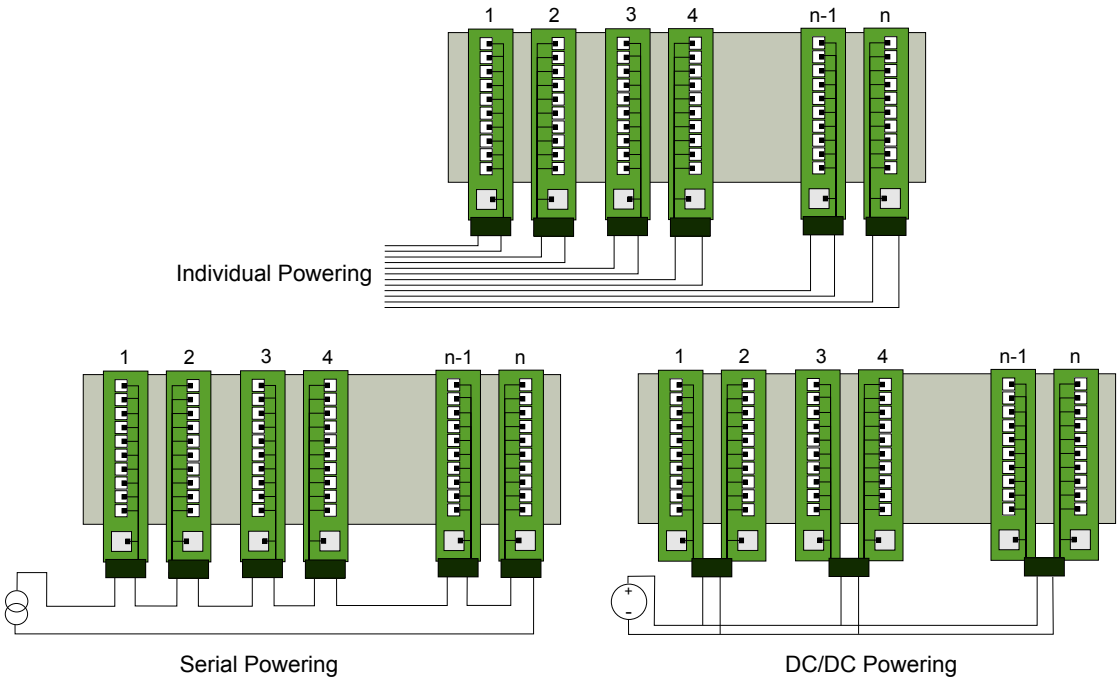



Figure 7.1: The different strip tracker powering schemes.

## 7.2 DC-DC powering

The DC-DC powering distribution scheme is based on powering the 13 modules on the stave plus the End of Stave (EoS) card in parallel. Each module and the EoS card will have their own DC-DC buck converter that takes care of stepping down the 12 V supplied on the voltage bus to 1.2 V (or 1.3 V) at the modules. The EoS will have a different voltage supply requirement of 2.5 V. The total current ($I_{DC}$) on the power line is given by $I_{DC} = N(\frac{I_s \cdot r}{\varepsilon})$ where N is the number of hybrids in a stave, $I_s$ is the hybrid's current, $r$ is the converter's voltage step down ratio and $\varepsilon$ is the converter's efficiency. The buck converter was selected due to the low number of passive components it requires plus the ability to integrate most of them into the converter's ASIC which is designed to withstand the high radiation levels expected in the ATLAS tracker.

## 7.3 Serial powering

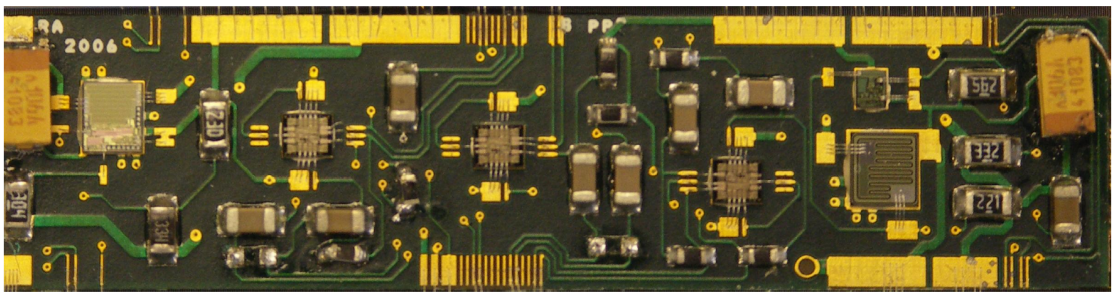



Figure 7.2: The SP Interface Board, comprising a shunt regulator and AC coupled LVDS buffers for communication[52].

Serial powering (SP) is intended to connect the modules to the powering bus serially with a constant current passing through each module. The voltage across this chain of modules ($V_{sp}$) is $V_{sp} = n \times V_h$, where $n$ is the number of hybrids in the chain and $V_h$ is the voltage required for every hybrid. Every module includes a shunt regulator and a shunt transistor to provide the

necessary voltage for the hybrids[53]. Shunt regulators are usually Zener diodes operated in reverse voltage. Operating in that voltage region, a Zener diode can maintain a stable, low ripple voltage under varying current loads. The LDOs on the ASICS would further drop the voltage to provide a stable voltage level for its digital and analogue parts. The fact that the modules are all connected serially means that they will all be floating at different potentials, this is overcome by adding AC coupling to the control and data lines.

## 7.4 Readout electronics power requirements

The power consumptions for the barrel stave and end-cap petal differ due to their different structuring. The ABCN130 is the common readout chip for both the stave and petal. The Hybrid Controller Chip (HCC), currently in the final stages of design, is used to control the ten ABCN130 chips on the stave's hybrid. The end-cap's petal has 10 different hybrids with the number of ABCN130 chips ranging from 7 to 12. Thus, the petal hybrids are expected to have different power requirements due to the different sensor geometries and varied number of readout chips. Assuming the nominal current of the ABCN130 is the same for both the petal and stave, the nominal power consumption of each chip will be:

$$\begin{aligned} P_{abcn} &= (I_d \times V_{ddd}) + (I_a \times V_{dda}) \\ &= (136\,\text{mA} \times 1.2\,\text{V}) + (34\,\text{mA} \times 1.2\,\text{V}) \\ &= 204\,\text{mW}, \end{aligned}$$

where $I_d$ is the nominal current drawn from the digital part, $I_a$ is the nominal current of the analogue part, $V_{ddd}$ and $V_{dda}$ are the voltages of the digital and analogue parts, respectively.

The power consumption of the HCC:

$$P_{hcc} = I_d \times V_{ddd} = 200\,\text{mA} \times 1.2\,\text{V} = 240\,\text{mW},$$

where $I_d$ is the nominal current draw of the HCC and $V_{ddd}$ is the voltage of the HCC.
The End of Stave (EoS) card's power consumption is:

$$\begin{aligned} P_{eos} &= (I_c \times V_c) + (I_{opt} \times V_{opt}) + (I_{sc} \times V_{sc}) \\ &= (1080\,\text{mA} \times 1.2\,\text{V}) + (200\,\text{mA} \times 2.5\,\text{V}) + (50\,\text{mA} \times 1.2\,\text{V}) \\ &= 1856\,\text{mW}, \end{aligned}$$

where $V_c$ and $I_c$ are the voltage and current of the EoS controller, $V_{opt}$ and $I_{opt}$ are the Opto-devices voltage and current. $V_{sc}$ and $I_{sc}$ are the Slow-Control voltage and current.
The total single sided stave power consumption is therefore:

$$\begin{aligned} P_{stave} &= ((P_{abcn} \times N_{abcn}) + P_{hcc})N_{hybrid} + P_{eos} \\ &= (((204\,\text{mW} \times 10) + 240\,\text{mW}) \times 26) + 1856\,\text{mW} \\ &= 61.1\,\text{W}. \end{aligned}$$

The total single sided petal power consumption, assuming all ABCN130 chips in the petal have the same performance is:

$$\begin{aligned} P_{stave} &= (P_{abcn} \times N_{habcn}) + (P_{hcc} \times N_{hybrid}) + P_{eos} \\ &= (204\,\text{mW} \times 82) + (240\,\text{mW} \times 11) + 1856\,\text{mW} \\ &= 21.2\,\text{W}, \end{aligned}$$

where $N_{habcn}$ is the number of ABCN130 chips in a petal and $N_{hybrid}$ is the number of hybrids in a petal. The above current and voltage values were obtained from [51].

## 7.5 Comparison

### 7.5.1 Powering schemes for petals and staves

A single powering scheme for both barrel and end-cap regions would clearly be the preferred solution, since this can minimize development and production time and costs. For the staves and petals, while the readout electronics are the same, the geometry and the number of chips per module are different. This creates different power profiles for the barrel and the end-cap regions and the powering schemes have to adjust accordingly. SP assumes that all the modules in the chain have the same power requirements, this is true for the stave but not for the petal because of the different number of chips per hybrid, as seen in Figure 7.3. On the other hand, the DC-DC powering schemes can possibly perform better in this situation where every buck converter would provide the necessary currents for the hybrids. i.e. adjusting with the power requirements.

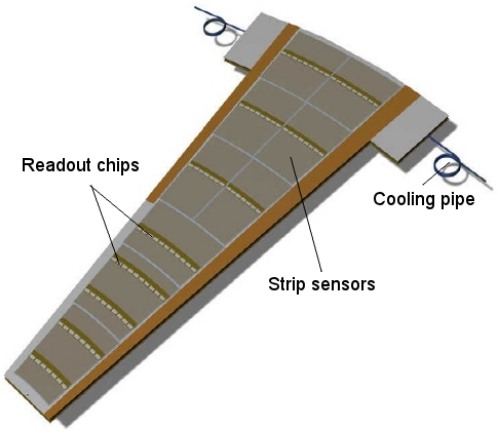



Figure 7.3: The proposed petal geometry [20].

### 7.5.2 Powering efficiency

The powering efficiency is defined by the ratio of the power delivered to the load to the total power delivered by the power source. In our example, the power efficiency for a short strip stave was evaluated. Tables 7.1 and 7.2 show the two efficiencies for the different powering schemes taking into consideration the different voltage requirements and the different conversion efficiencies ($\varepsilon$). The values for $\varepsilon$ were obtained from prototypes of the different converters.

| **End of Stave card** | $\varepsilon$ | |
|---|---|---|
| Current at 1.2 V | | 1130.0 mA |
| Current at DC-DC converter (12 V - 1.2 V) | 70% | 161.4 mA |
| Current at 2.5 V for opto-devices | | 200 mA |
| Current at DC-DC converter (12 V - 2.5 V) | 85% | 49 mA |
| Total current at 12 V | | 210.5 mA |
| **Hybrid** | | |
| Current at 1.3 V | | 1900 mA |
| Current at DC-DC converter (12 V - 1.3 V) | 80% | 257 mA |
| Total current at 12 V (single sided - 26 hybrids) | | 6.9 A |
| Total dissipated power | | 83 W |
| Total useful power | | 61 W |
| Total Efficiency | | **74 %** |

Table 7.1: The DC-DC estimated power efficiency table.

| **End of Stave card** | $\varepsilon$ | |
|---|---|---|
| Current at 1.2 V | | 1130.0 mA |
| Current at DC-DC converter (2.5 V - 1.2 V) | 88% | 614 mA |
| Current at 2.5 V for opto-devices | | 200 mA |
| Total current at 2.5 V | | 816 mA |
| **Hybrid** | | |
| Current at 1.3 V | | 1900 mA |
| Current at shunt regulator | 85% | 2235 mA |
| Total current to stave (single sided - 26 hybrids) | | 3 A |
| Total dissipated power | | 78 W |
| Total useful power | | 61 W |
| Total Efficiency | | **79 %** |

Table 7.2: The SP estimated power efficiency table.

A slight difference in the overall efficiency is observed with the SP scheme having a marginally better efficiency.

### 7.5.3 Operation in magnetic fields and radiation tolerance

The inner detector sits in a 2 T magnetic field that cannot be perturbed and operates in a high-radiation environment. Both these factors must be considered in defining the powering scheme. The main constraint of the 2 Tesla field is the restriction to use ferromagnetic coils that are essential for the DC-DC converter's operation. Air core coils can be operated in high magnetic fields but due to the absence of a ferromagnetic core the inductance value for such coils is lower. In compensation for the lower inductance, the air-core coil would need to be larger in size. For the SP scheme, no inductors are required for operation but the high radiation environment is expected to have effects on the electronics such that the ASICs for both SP and DC-DC converters have to be designed to be radiation-tolerant. The DC-DC converter ASIC have been successfully qualified to withstand radiation levels up-to hundreds of Mrads[54].

### 7.5.4 Real-estate and material budget

The material budgets of the two schemes have been previously estimated [55]. The study investigated the number of circuit components needed for the design and the extra space required on the hybrid to accommodate the powering components.

| **Material** | **Radiation length** |
|---|---|
| Copper | 0.0518% |
| Capacitors | 0.0368% |
| Resistors | 0.0002% |
| Plastic | 0.0121% |
| FR4 | 0.0149% |
| ASIC | 0.0002% |
| **Total** | 0.1160% |
| **% of module** | 21.6% |

Table 7.3: The material budget for the DC-DC powering scheme. The copper radiation length includes the inductor.

| **Material** | **Radiation length** |
|---|---|
| Extra hybrid area | 0.00636% |
| Capacitors | 0.00452% |
| Resistors | 0.00297% |
| SPP | 0.00020% |
| Shunt transistor | 0.00003% |
| ASIC | 0.00060% |
| **Total** | 0.01468% |
| **% of module** | 2.7% |

Table 7.4: The material budget for the SP scheme.

The figures in Tables 7.3 and 7.4, show a clear difference between the two schemes. The SP scheme is seen to perform better with the radiation length but there are ways to decrease the radiation length of the DC-DC scheme. The radiation length of the DC-DC scheme is a contribution of many components. The shield and the air-core inductor contribute alone to about

20% and 18%, respectively. The material of these two components of the DC-DC design can be reduced. The shielding can be reduced by using thin copper shields or using aluminium shields instead; aluminium has lower density and yields a longer radiation length. The inductor contribution can also be improved by using a different type of coil. An embedded planar coil could be a good candidate, it would be made of less material and can also reduce the shielding requirements.

The amounts of cabling used must also be carefully evaluated as both schemes are expected to use different cable routings. The SP scheme requires one line to power the hybrids on the staves and petals and one line to power the EoS card, while the DC-DC scheme requires a single line to power an entire stave or petal. Based on these arrangements, the total number of lines and cross sections are shown in Table 7.5. The difference in the figures is attributed to the extra 1200 feed lines in the barrel stave and 896 feed lines for the End-cap petals to separately power the EoS cards for the SP scheme.

| **Powering Scheme** | **Number of cables** | **Total cross section ( $cm^2$)** |
|---|---|---|
| DC-DC | 2096 | 247 |
| SP | 4192 | 258 |

Table 7.5: The cable requirements for the SP and DC-DC powering schemes. Cross section calculations assume a 2 $mm^2$ of copper per lead per 1 A[51].

### 7.5.5 Risk assessment and reliability

The highest risk when powering modules in series or parallel is the possibility of losing power to the whole chain, i.e from a short-circuit in the DC-DC powering scheme or an open circuit in the SP scheme. In either case, protection measures must be put in place. In SP, a Power Protection Board (PPB) has been designed to detect open-circuits and isolate faulty hybrids[56]. In the DC-DC converter design, the ASIC has been designed to deal with over-current, over-

temperature and input under-voltage [57]. There are also digital control lines which can control the buck converters to turn them off in the case of a faulty module.

## 7.6 Conclusion

Both SP and DC-DC schemes have been shown to be suitable for powering the new strip tracker. One of the two schemes has to be chosen, but more R&D work is required before this decision can be made. They will be thoroughly studied once a full stave with ABC130 chips is built. The powering scheme of choice will be the one that can be mass produced and is suitable for the entire strip tracker (strips and petals). Even though the SP scheme is presently superior to the DC-DC powering scheme in terms of efficiency and material budget, the DC-DC converters are still in the R&D phase and further work will improve their performance. Recent decisions have favoured DC-DC as the baseline solution with serial powering as a backup scheme[70].

# 8 Tests of the DC-DC low voltage powering scheme

The first set of readout modules (stavelet) arriving at CERN were powered with DC-DC converters. The stavelet was tested for performance (see chapter 9) to be later compared to the SP stavelet. This chapter investigates some of the issues that are only present with the DC-DC powering scheme. It looks at the electromagnetic field emissions of the converters, their effective shielding and also investigates the use of planar DC-DC converters, as opposed to the toroidal coil DC-DC converters that have been installed with the stavelet.

## 8.1 DC-DC buck converter

A buck converter is a type of a switched-mode power supply where the DC output voltage is lower than the DC input voltage. The buck converter relies on a flywheel circuit which is basically a circuit that continues oscillating after the stimulus has been removed (i.e. in this case, when the switch is off). A simplified schematic of the buck converter is shown in Figure 8.1 where it shows the switching transistor and the flywheel circuit (diode, capacitor and inductor).

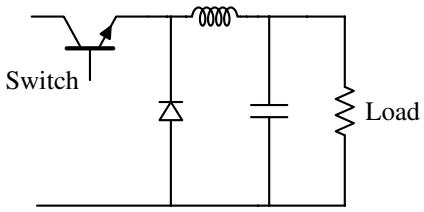



Figure 8.1: A typical schematic of a DC-DC buck converter.

When the switch is on, the current flows through the inductor. Initially, the current flow is restricted due to the storage of energy in the inductor. At this point, the capacitor is also charged and the current gradually increases. The diode plays no role when the switch is on as it is in reverse bias. Once the switch turns off, the magnetic field in the inductor collapses and current is generated which now flows in the opposite direction. The inductor should have stored enough energy to keep the current flowing while the switch is off. Due to the change in current direction, the diode becomes in a forward biased state allowing current to go through it thus completing the circuit. This switching behaviour results in a continuous output at the load but there remains a wave along the DC level with a small amplitude, this is known as a ripple waveform.

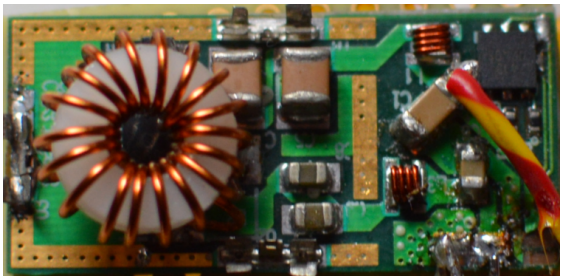


Figure 8.2: An image of the STV10 DC-DC buck converter.

The STV10 buck converter, which was used to power the modules of the DC-DC stavelet, is controlled by the commercial Linear Technology LTC3605 buck controller. The converter operates with a 10 V input and regulates an output of 2.5 V at a maximum current of 5 A and a switching frequency of 2 MHz. The converter, which was built to power the strip tracker

prototype readout modules, has a compact design and can operate in high, constant magnetic fields. The largest object on the converter is the air-core toroidal coil. An air-core coil instead of a ferromagnetic core coil, which can provide the same inductance with a smaller size, is required to achieve the compatibility with the constant 2 T magnetic field that will be present in the ATLAS inner tracker. The converter is designed to have an efficiency of 85% for a current of 2 A and an input between 7 V and 12 V. At maximum current the converter is 75% efficient. The ultimate and final DC-DC converter will not be using a commercial chip but a custom made radiation-hard ASIC[43].

## 8.2 Electromagnetic compatibility of the upgraded strip tracker

### 8.2.1 Motivation

The DC-DC low voltage powering scheme uses a coil to regulate its output. The coil is a major source of electromagnetic emissions which could introduce noise to the readout electronics. Shielding the toroidal coil using a copper coated plastic box or an aluminium box was seen to be effective but the material budget was a concern. In order to choose the correct shielding, the electromagnetic compatibility of the stavelet has to be investigated. Understanding the source of the noise and its nature can help decide what and how much shielding is necessary, while using the minimum amount of material. Initially, an external DC-DC converter was used to generate the EM fields. However, the coil generates the E-field and the H-field simultaneously. To investigate the effects of the fields separately, electromagnetic probes were used to generate the individual fields. The noise impact was then examined with 3-point-gain scans.

### 8.2.2 Field probes

Figure 8.3: The E and H near-field probes, manufactured by ETS-Lindgren. The magnetic field probe is in the middle and the two probes on the side are electric field probes (The left ball probe generates a wider field than the right stub probe).

The electric (E) and magnetic (H) field probes, shown in Figure 8.3, are commonly used in EMC diagnostic work. They are usually connected to a spectrum analyser and used to pick-up the EM emissions off circuits and electrical devices. The probes are essentially antennae working in the near-field. Loop antennae are used with magnetic fields and monopole antennae are used with the electric fields. A schematic of a simple loop probe can be seen in Figure 8.4. The electric field stub probe is a piece of coaxial cable with the conducting core exposed at the tip, the exposed tip acts as a monopole antenna to pick-up/emit an electric field. The absence of a loop helps reject the magnetic field. The loop probe is a closed circuit coaxial cable with a notch opening at the top of the loop to create a balanced electric field shield which enhances the rejection rate of the electric field.

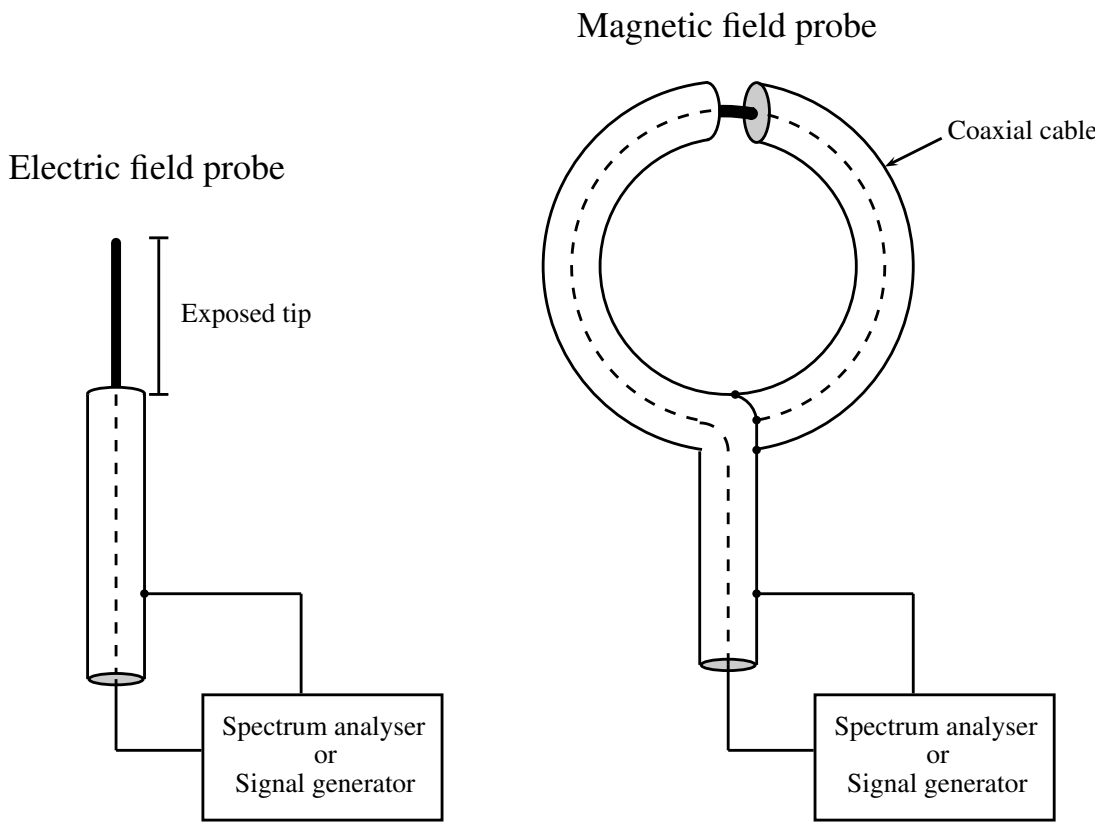



Figure 8.4: The schematics of the field probes. The exposed tip of the electric field probe picks up the electric field and the absence of a loop helps reject the magnetic field. The magnetic field probe has a notch opening in its closed circuit to create a balanced electric field shield which enhances the rejection rate of the electric field.

### 8.2.3 Noise injection setup

The simple setup, shown in Figure 8.5, provides the ability to test the effects of electric and magnetic fields on the stavelet separately. Field probes (loop probe for the magnetic field and stub probe for the electric field) are placed on top of the stavelet and connected to a signal generator. The generator drives the probes with a 2 MHz square wave to simulate the emissions of the DC-DC converter.

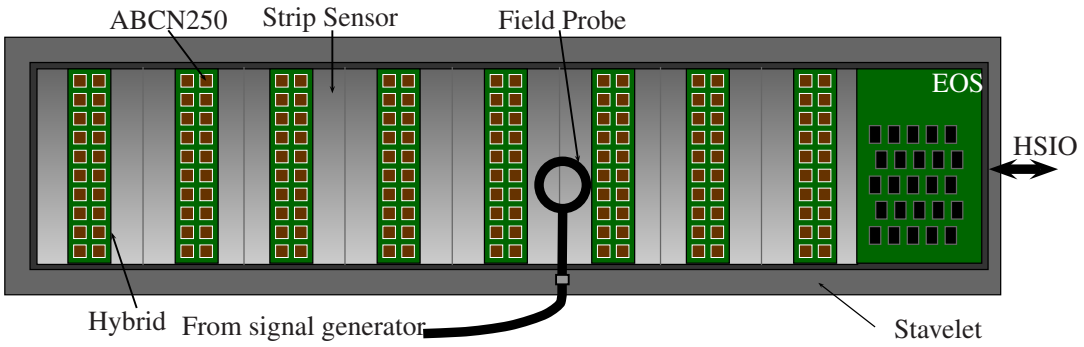



Figure 8.5: The noise injection test setup. The probe is placed on top of one of the modules to test the electromagnetic compatibility of the readout system.

The probes were driven to produce a field consistent with the field produced by the DC-DC converter. The power profiles of the converter's fields are described in the next section. The tests were performed on both a serial powered and DC-DC powered stavelets (the powering scheme are explained later in this chapter). Both were powered and biased (at 250 V) and 3-point-gain (1 fC) scans were performed.

### 8.2.4 DC-DC converter field profiles

The EM emissions are expected to be highest coming from the converter's inductor. Thereby, the emissions have to be properly identified to systematically inject them to the setup to understand

their effect on the readout electronics. The first measurements resulted in an electric field map of the DC-DC converter. The values in the map were read through a spectrum analyser connected to the stub probe on which was moved in the x-y plane. The probe was moved in 0.1 mm steps and the field intensity was recorded at each step. The map is shown in Figure 8.6.

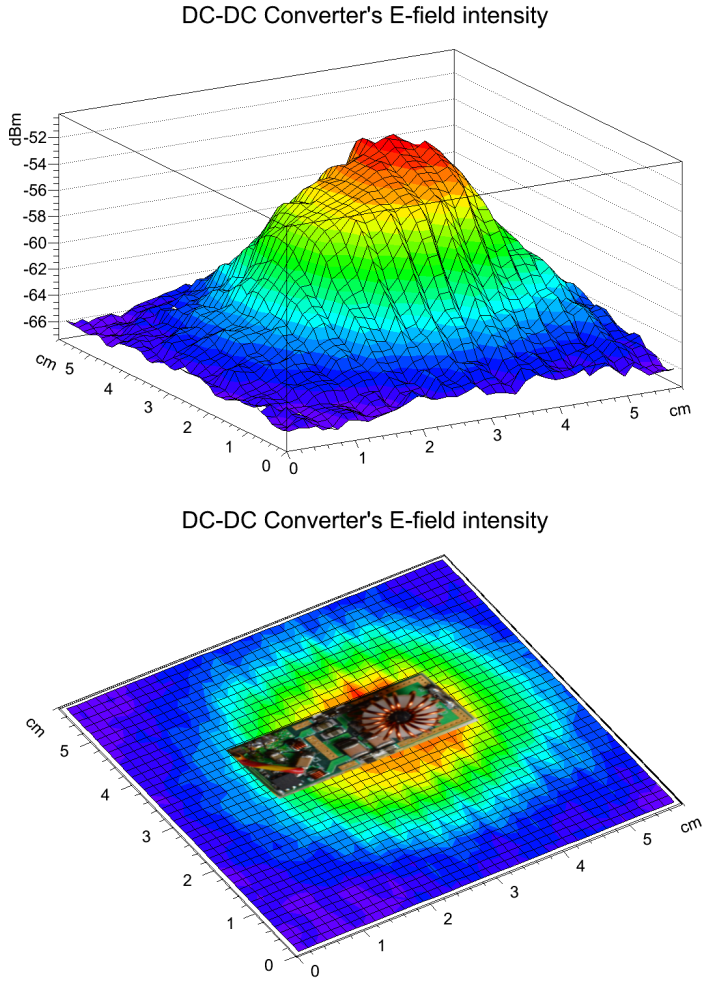



Figure 8.6: The DC-DC converter E-field intensity in the x-y plane. The E-field intensity is highest at the toroidal coil.

Due to the switching operation of the converter, higher order harmonics are expected to be

resonating at frequencies above the 2 MHz switching frequency. The electric and magnetic full power spectra of the converter are shown in Figure 8.7 and Figure 8.8, respectively. The spectra consist of a DC component corresponding to the mean value of the output signal and AC components at the fundamental switching frequency and its harmonics.

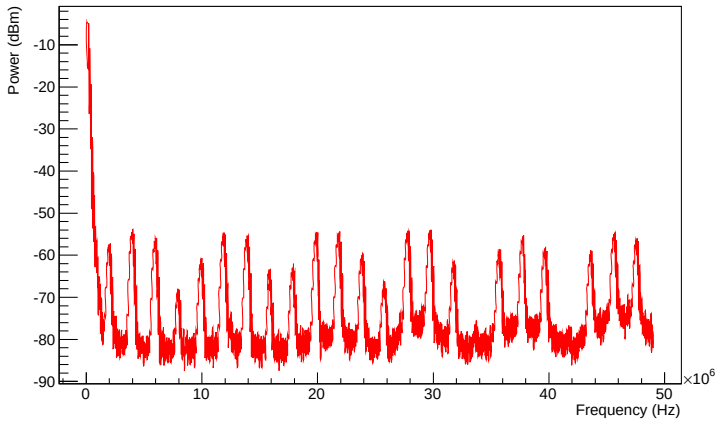



Figure 8.7: The DC-DC converters E-field power spectrum.

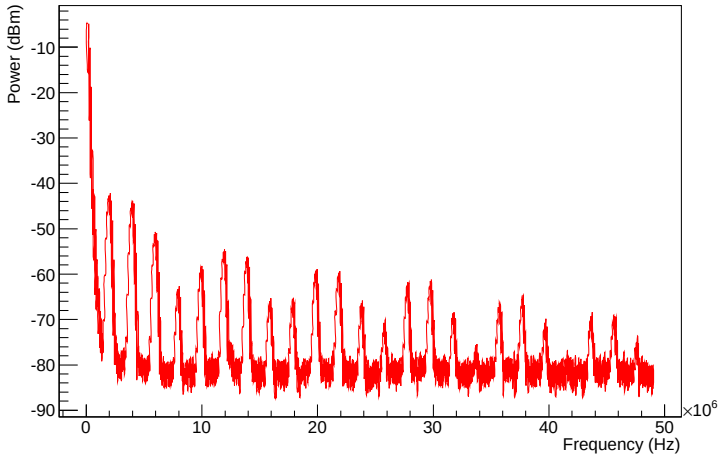



Figure 8.8: The DC-DC H-field power spectrum.

### 8.2.5 Noise injection results

#### Magnetic field noise testing

Noise was measured using a 3-point-gain scan from a 3 cm loop probe driven with the signal generator and placed on top of the stavelet. The noise that was injected at the module underneath the probe had a saddle shape reflecting the geometry of the probe. The higher noise pick-up through the long wire-bonds, as shown in Figure 8.9, indicates noise is being introduced via capacitive coupling[1]. Using a spectrum analyser and the stub probe confirmed the presence of an electric field generated by the loop probe alongside the magnetic field.

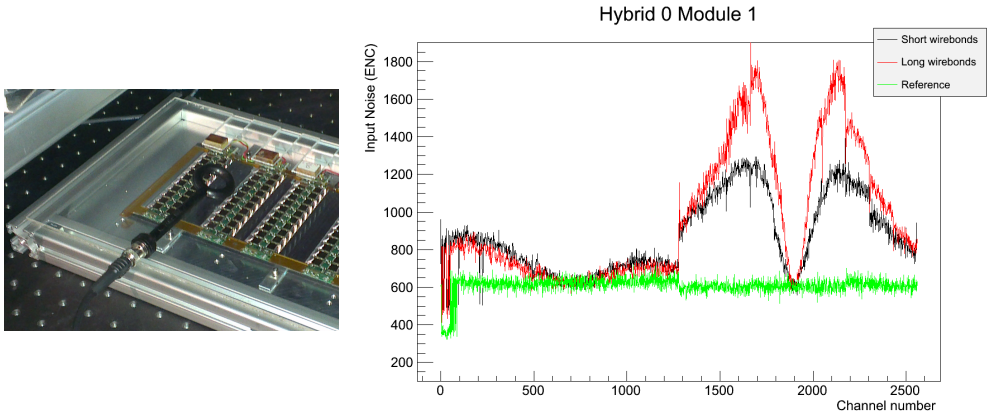



Figure 8.9: Left: The magnetic probe placed on top of the stavelet. Right: The plot of the input noise against channel number. The high noise are for the channels under the probe that has been generating a magnetic field. The RMS of the reference noise is 50 electrons.

To enhance the rejection rate of the loop probe, the probe was wrapped with copper tape and grounded to the stavelet. The success of the probe shielding[2] was confirmed with the disappearance of the noise as shown in Figure 8.10.

[1] Capacitively coupled noise injection is explained in section 8.2.7

[2] The magnetic field emission of the shielded loop probe was tested with another magnetic field probe. A spectrum analyser was connected to the secondary probe to make sure that the shield has not eliminated the magnetic field as well.

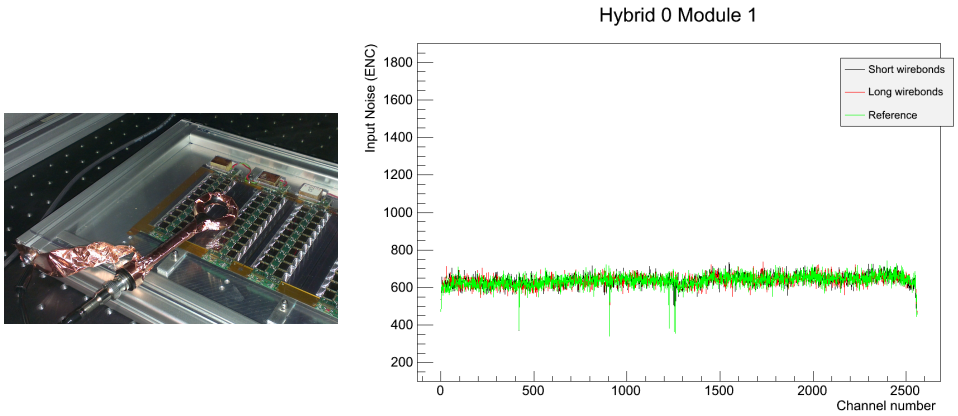



Figure 8.10: The same as Figure 8.9 but with a copper shield wrapped around the probe. The noise plot on the right show no added noise.

### Electric field noise testing

The disappearance of the noise confirms that the stavelet is not susceptible to an alternating magnetic field. The susceptibility to an E-field was investigated with an E-field stub probe (Figure 8.11). Due to the narrow field of the stub probe, the noise injection can be very localised. It was seen that by placing the probe in the middle of the hybrid no noise was detected, but as the probe became closer to the wire-bonds, the noise increases with the long wire-bonds picking-up the noise first, as shown in Figure 8.12. The geometry of the wire-bonds is shown in section 8.2.7.

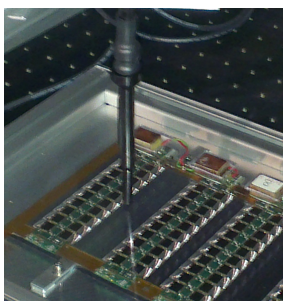


Figure 8.11: The E-field probe pointed at the stavelet.

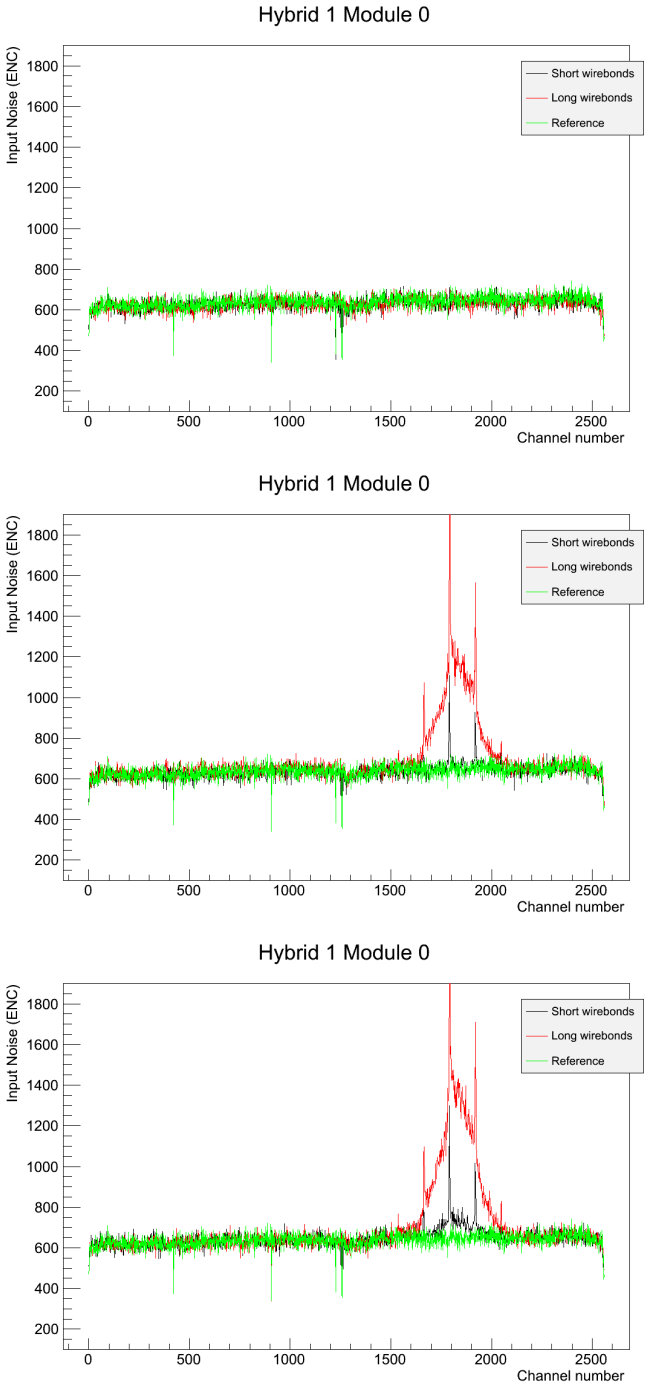



Figure 8.12: The noise from the E-field probe at different positions. Top plot: probe on top of the hybrid and between chips; no noise. Middle plot: probe on top of the chip and near the wire-bonds; noise mostly on the long wire-bonds. Bottom plot: probe on top of the wire-bonds; both long and short wire-bonds pick-up noise, but still the higher noise is on the long wire-bonds.

### 8.2.6 Shielding electromagnetic fields

#### Near and far fields

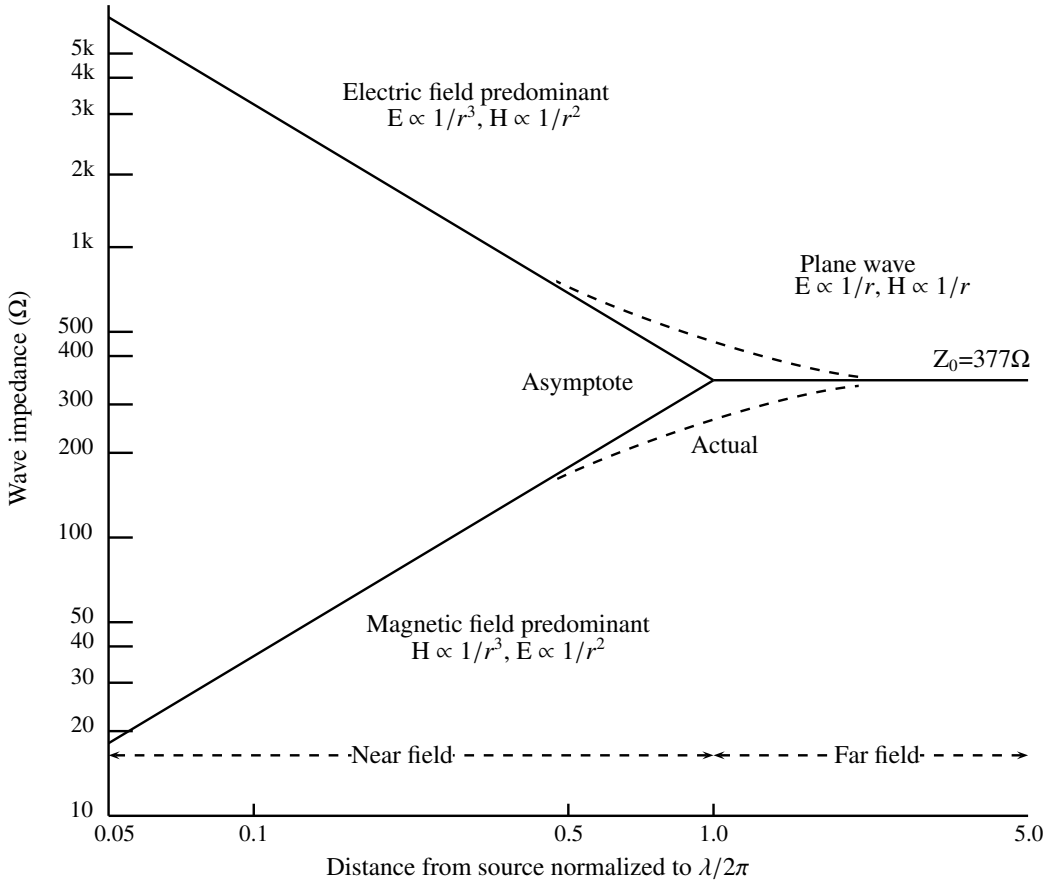



Figure 8.13: The wave impedance dependence on the distance from the source and the field's type[44].

Intense emissions of EM fields can greatly influence the noise levels of the readout electronics. Shielding is required to attenuate the EM emissions, thereby eliminating the unwanted noise. The shield provides protection to all the susceptible equipment located outside it. The field emissions can be classified into two regions, near-field and far-field. The near-field is the space less than $\lambda/2\pi$ away from the source. For frequencies of the order of few MHz, the near-field

is quite large (in the order of 10 m). The emission of the fields also depends on the source, if the source has high voltage and low current (e.g. a monopole) the field emissions will be predominantly electric while a source with a low voltage and a high current (e.g. a wire loop), emits fields that are predominantly magnetic. Figure 8.13 shows the impedance and attenuation for the two cases. In contrast to the far-field, the electric to magnetic field ratio within the near-field is not constant, because of their different attenuation rates. This is why they have to be treated separately.

#### Shielding effectiveness

Many factors dictate the effectiveness of a shield, such as the shield material, its shape and the frequency and direction of the field. The reflection and absorption losses, are the two factors that determine the effectiveness of the shield. The total shielding effectiveness is expressed as

$$S\,(\mathrm{dB}) = A + R + B, \tag{8.1}$$

where $A$ is the absorption loss, $R$ is the reflection loss and $B$ is the correction factor. Normally, $B$ can be neglected for electric fields.

When an electromagnetic wave passes through conductive material, the intensity falls exponentially due to the ohmic losses in the material. The attenuation of a wave intensity to $1/e$ is determined by the skin depth of the material. The absorption rate is expressed as

$$A = 20\left(\frac{t}{\delta}\right)\log(e)\ \mathrm{dB}, \tag{8.2}$$

where $\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$ is the skin depth. Such that:

$$A = 8.69t\sqrt{\pi f \mu \sigma}\ \text{dB}, \tag{8.3}$$

where $t$ is the thickness of the shield, $f$ is the frequency of the wave $\mu$ is the permeability of the material and $\sigma$ is the conductivity of the material.

The reflection loss $R$ on the other hand depends on the impedance of the shield and the impedance of the wave in the near-field. Electric fields usually have higher absorption losses due to their higher impedance. At $r < \lambda/2\pi$, the electric field impedance can be expressed as:

$$|Z_e| = \frac{1}{2\pi f \varepsilon r}, \tag{8.4}$$

where $r$ is the distance between the source and the shield, $\varepsilon$ is the dielectric constant and $f$ is the frequency. The impedance of the conductor or the shield can be expressed as:

$$|Z_s| = \sqrt{\frac{2\pi f \mu}{\sigma}} = 3.68 \times 10^{-7} \sqrt{\frac{\mu_r}{\sigma_r}}\sqrt{f}, \tag{8.5}$$

here $\mu(\mu_r)$ and $\sigma(\sigma_r)$ are the permeability(relative) and conductivity(relative)[3] of the material, respectively and $f$ is the wave frequency. The reflection loss can be expressed as (refer to Appendix A.1 for the derivation)

$$R = 20\log\frac{|Z_w|}{4|Z_s|}\ \text{dB}. \tag{8.6}$$

[3] $\sigma_r$ is the conductivity relative to the conductivity of copper which is $5.28 \times 10^7$ S/m.

where $Z_w$ is the wave impedance.

By substituting 8.6 with 8.4 and 8.5 ($Z_w = Z_e$), one gets:

$$R_e = 322 + 10 \log \frac{\sigma_r}{\mu_r f^3 r^2} \text{ dB}. \tag{8.7}$$

Similarly for the magnetic field ($Z_w = Z_m$):

$$Z_m = 2\pi f \mu r, \tag{8.8}$$

one gets:

$$R_m = 14.6 + 10 \log \left( \frac{f r^2 \sigma}{\mu} \right) \text{ dB}. \tag{8.9}$$

The reflection losses depend on the impedance of the wave and the impedance of the material. For electric fields, the material impedance ($Z_s$) is much greater than the wave impedance ($Z_e$) and the reflection rate is high. For the magnetic field, the opposite is true. $Z_m \gg Z_s$ and there are high reflection losses. Therefore, if the barrier is thin then the electric field will firstly be fully reflected due to $Z_s \gg Z_e$ and the magnetic field will pass through. Because of the thin barrier, absorption is very low so the magnetic wave propagates and arrives at the second boundary. At this point, the boundary impedance is reversed ($Z_m \gg Z_s$) and reflection occurs: this is known as multiple reflection. The correction factor for the multiple reflections can be expressed as

$$B = 20 \log(1 - e^{-2t/\delta}) \text{ dB}, \tag{8.10}$$

where $t$ is the thickness of the barrier and $\delta$ is the skin depth.

To conclude, at low frequencies the primary shielding for the electric field is the reflection loss while the absorption loss is the primary shielding mechanism for the electric field at high fre-

quencies. As for the magnetic field, the primary shielding mechanism is the absorption loss which mostly occurs at high frequency. At low frequencies, the shielding is very poor for the magnetic fields. However, this could be improved with the use of thin shields and relying on the multiple reflection loss.

### Shields for the DC-DC converter

The EM source (the toroidal coil) is predominantly magnetic but electric fields are still present. The skin depth of copper is ~46 μm at 2 MHz. Having a shield that has a barrier thickness of the order of few skin depths is problematic, due to the need to have the minimum amount of material. Because of this requirement and considering the switching frequency of the converter of 2 MHz to be a relatively low frequency, we can instead rely more on the multiple reflection losses rather than the absorption loss. As for the electric field, the shielding is reliant on the reflection and absorption losses.

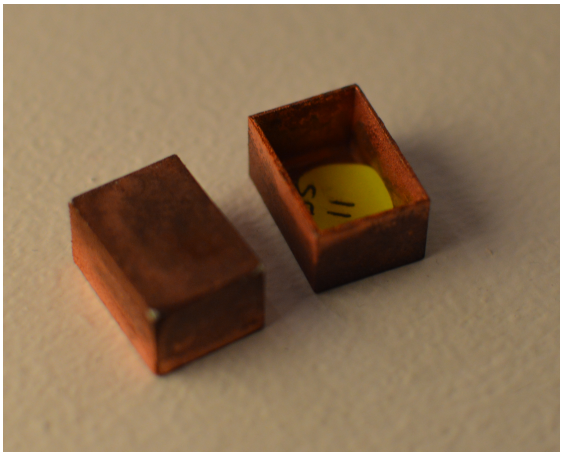


Figure 8.14: The EM double coated copper shields.

The shields shown in Figure 8.14, are flame sprayed shields. Copper powder is melted and sprayed onto a plastic box, this produces a hard coating with excellent conductivity. The qual-

ity and thickness of the coating is evaluated by weighing the shield and examining it under a microscope as shown in Figure 8.15 and Figure 8.16.

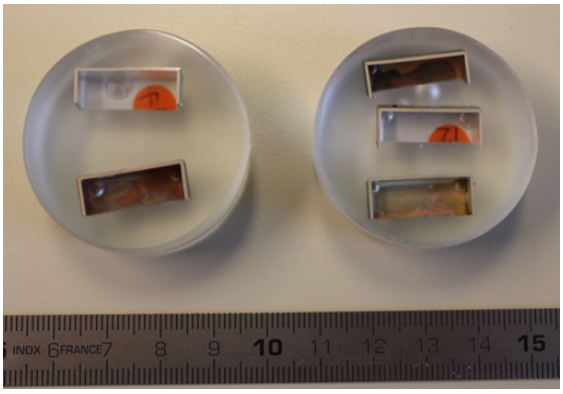



Figure 8.15: The shielding boxes are immersed in a special resin which is then cut, polished and viewed under a microscope.

There have been a variety of shields produced (different coating thickness, double and single sided coating, aluminium box or copper coated plastic boxes). Ultimately, the shield of choice needs to be have the lowest radiation length while providing the attenuation needed to eliminate all the noise injected to the electronic due to the coil emissions.

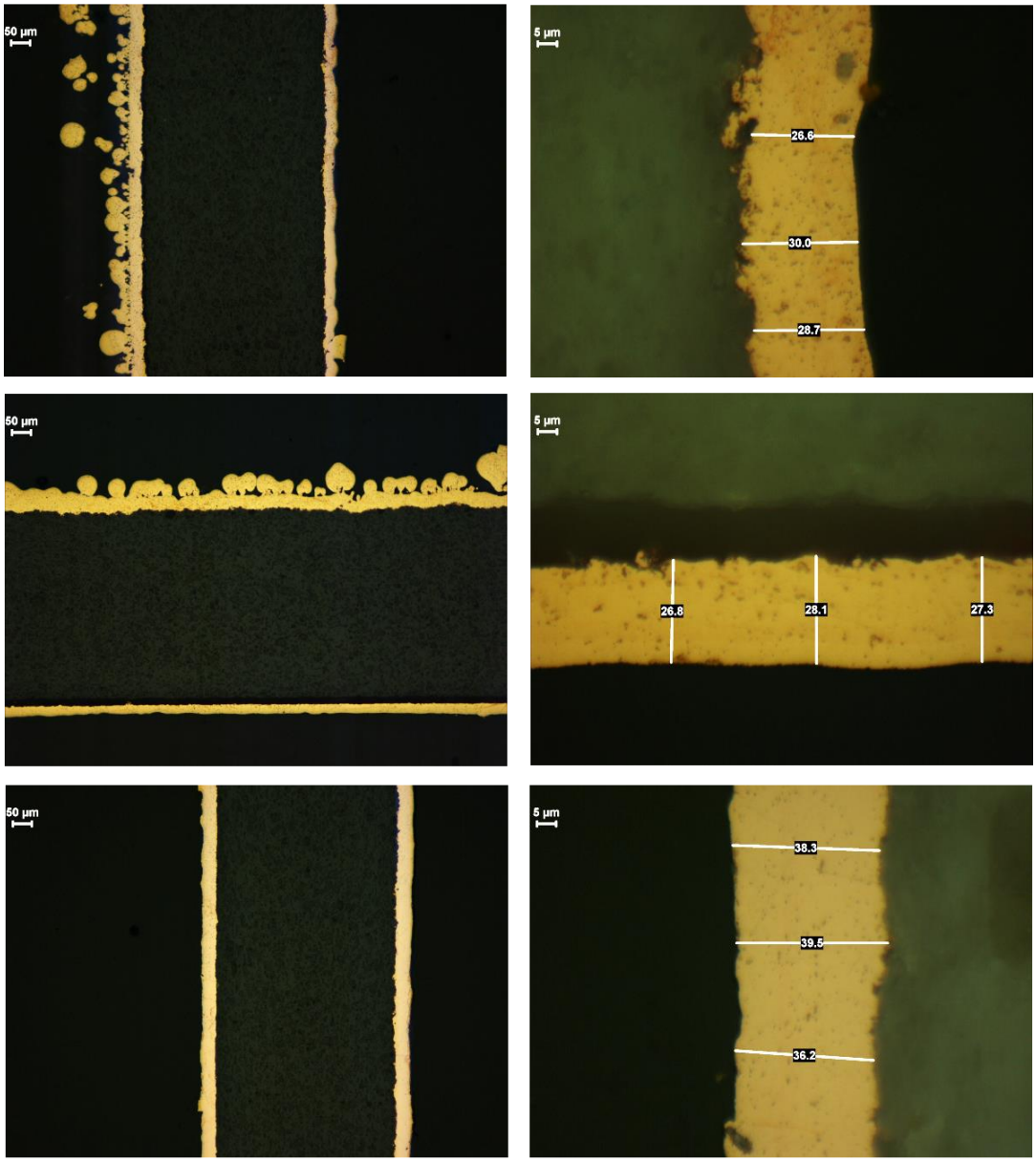



Figure 8.16: The microscope picture of a sectioned copper coated box. Uniformity of the coating is very good and the thickness is measured to be approximately 30 µm.

### 8.2.7 Simulation

To understand the coupling effect between the E-field and the wire-bonds, a model of the wire-bonds connecting the sensor to the readout chip has been built with Ansoft HFSS[45]. The model can be seen in Figure 8.17 and the real wire-bonds can be seen in Figure 8.18. By generating an E-field on top of the model, the field moves towards and surrounds the wire-bonds. The long wire-bonds are seen to be mostly interacting with the field and shielding the short wire-bonds, until they fan out at the sensor side. The field is also seen coupling more with the wire-bonds at the edges of the model. As has been seen with the noise measurements in Figure 8.12.

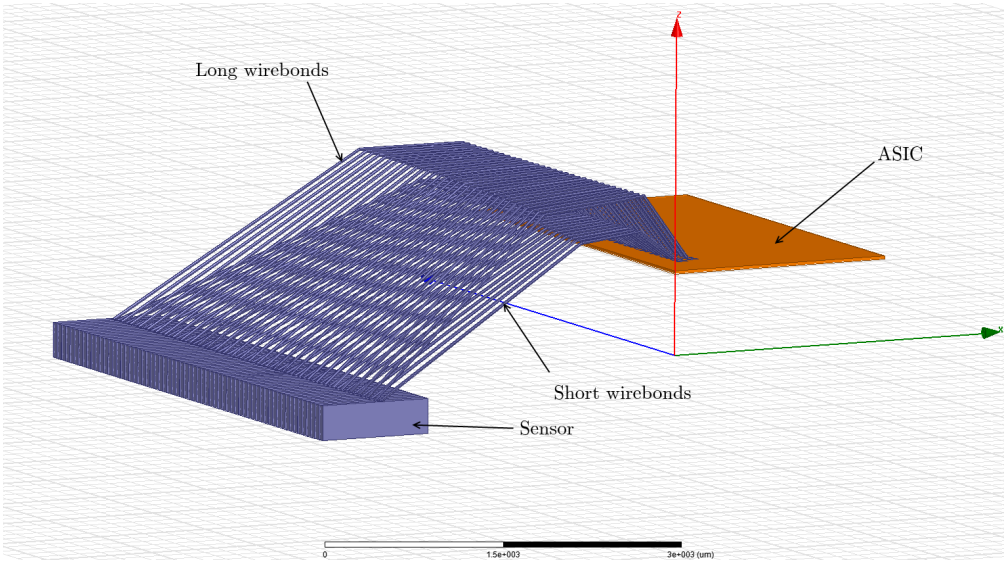



Figure 8.17: A model of the wire-bonds drawn with HFSS[45]. The wire-bond geometry is ~4.5 mm in length, the bond angle is ~12° and the diameter is 25 µm.

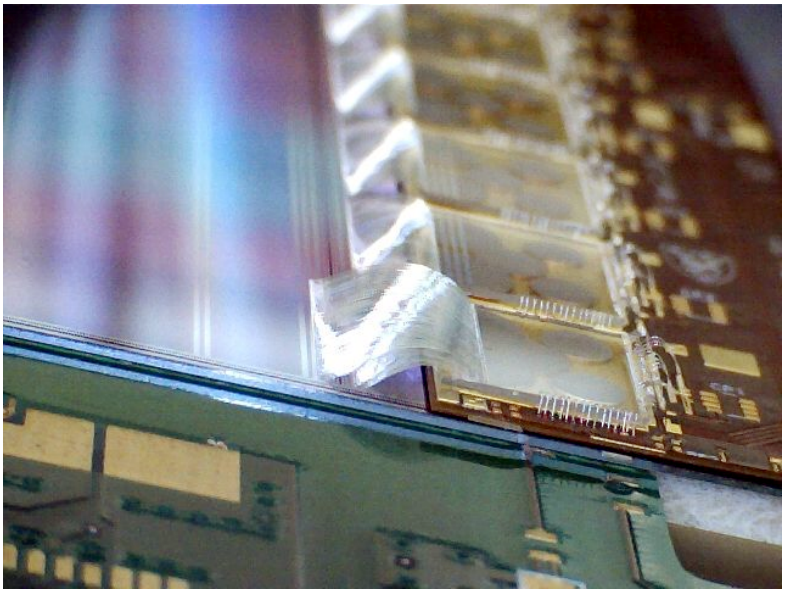


Figure 8.18: An image of the wire-bonds connecting dummy readout chip to the sensor.

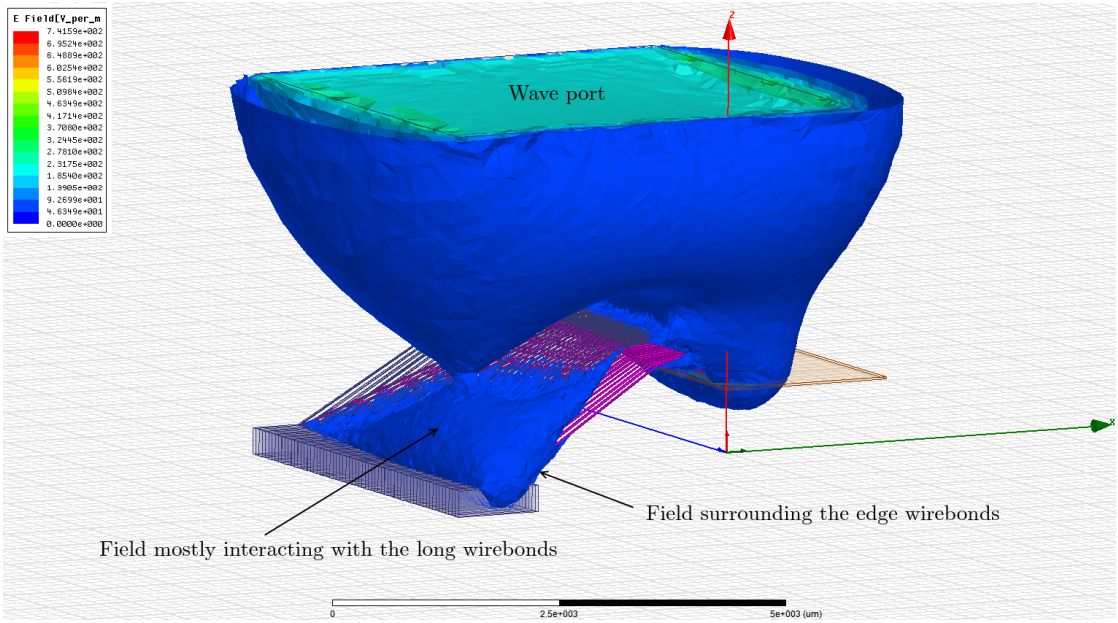



Figure 8.19: The simulation results of the E-field interaction with the wire-bonds. The simulation included a wave port which simulates an alternating E-field. The E-field is seen to move towards and couple with the wire-bonds.

### 8.2.8 Conclusion

The noise plots in section 8.2.5 have been very helpful in identifying the source of noise and its behaviour. The H-field tests have shown that by introducing an alternating magnetic field, anywhere on the stavelet, no noise can be detected. This is different to what previous tests[46] on hybrids have shown, where the entire noise level for the readout channels shifts up. The reason for the non-susceptibility can be attributed to the improved grounding of the stavelet. It was seen, however, that the stavelet is highly susceptible to electric fields. The E-field results have shown high noise pick-up from the stub probe. Moving the probe confirmed that the noise was due to capacitive coupling with the wire-bonds. This can be seen in the results in Figure 8.12 where the noise is only picked up when the probe is at close proximity to the wire-bonds, given the very small field generated by the stub probe. The results also show the higher pick-up at the long wire-bonds in addition to noise spikes at every 128 channels. This is because of the shape of the electric field and its interaction with the wire-bonds.

The results from simulation have shown that the higher noise pick-up at the long wire-bonds are due to the fact that they are crossing over the short wire-bonds and preventing them from coupling with the electric field. In addition, each ASIC is wire-bonded to 128 strips. The space between every 128 strips allows the electric field to enclose the edges of the wire-bonds, which results in the high peaks of noise.

The presence of a magnetic field has shown no effect on the electronics. This means the shielding must predominantly attenuate the E-fields. The high reflection losses of the electric field at a conducting barrier, means a very thin shield can be used, satisfying the minimum material requirement and attenuating the electric field enough not to be seen by a 3-point gain scan. The major constraint is the uniformity of the shield for the very thin coatings used.

## 8.3 Planar DC-DC converter

### 8.3.1 Motivation

An air core coil is an inductor which does not rely on a ferromagnetic core to provide an inductance. Air core inductors are able to operate in high magnetic fields but are usually larger than ferromagnetic core inductors for the same value. Planar air core coils are very appealing because of their smaller volume and ease of fabrication: they can be embedded in the PCB layout of the converter. Mutual inductance can also be exploited with the use of multilayer planar coils which can offer higher inductance without the increase in the area of the coil. Planar coils are believed to be able to achieve the same performance as toroidal coils with less material used to create the coil itself and the material used for shielding.

### 8.3.2 Planar coil methodology

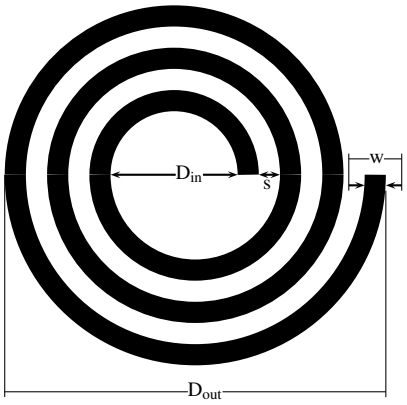



Figure 8.20: The typical geometry of a planar spiral coil.

In a single layer planar coil the inductance is controlled by the number of turns and the diameters of the coil. The inductance is directly proportional to the diameters and the number of turns (i.e. a large inductance means a larger area); a problem in case of limited PCB area. The

empirical formula for a single planar coil can be expressed as[47]:

$$L = \frac{\mu_0 N^2 D_{avg}}{2}\left(\ln\frac{2.46}{\rho} + 0.2\rho^2\right), \tag{8.11}$$

where $\mu_0$ is the vacuum permeability, $N$ is the number of turns, $D_{avg}$ is $(D_{in} + D_{out})/2$ and $\rho$ is the fill factor $(D_{out} - D_{in})/(D_{out} + D_{in})$. The use of a multilayer planar coil introduces mutual inductance which can greatly affect the overall inductance of the coil. The coupling coefficient of a multilayer inductor has to be determined in order to calculate the mutual inductance. The coupling coefficient $K_C$ is a measure of how well the layers of the coil are coupling together. It can be calculated using the following empirically derived formula[48]:

$$K_C = [N^2(0.184X^3 - 0.525X^2 + 1.038X + 1.001) \times (1.67N^2 - 5.84N + 65) \times 0.64]. \tag{8.12}$$

The mutual inductance $M$ is then

$$M = 2K_C\sqrt{L_1 L_2}. \tag{8.13}$$

Assuming the two layers are identical, then an accurate expression for the total inductance would be:

$$L_{total} = L_1 + L_2 \pm 2M. \tag{8.14}$$

Just as in any other mechanical or acoustic resonant system, there must be a damping factor. In this case the damping factor is affected by two losses, the resistive and radiative losses. The first is the result of the ohmic properties of the metal, and since the coil resonates at high frequencies the current flows on the surface of the metal due to the skin effect. With conductivity $\sigma$, track

width $w$, length $l$, and skin depth $\sqrt{2/\mu_0\sigma\omega}$, the ohmic resistance can be expressed as:

$$R_{res} = \sqrt{\frac{\mu_0\omega}{2\sigma}}\frac{l}{w}.$$

A more accurate result can be achieved if the true nature of the exponential decay of the electric field is used

$$R_{res} = \frac{l}{\delta\sigma\omega(1-e^{-\frac{t}{\delta}})},$$

where $\delta$ is the skin depth and $t$ is the track thickness. The radiative losses on the other hand are due to the magnetic dipole flowing around in loops, and it is safe to assume that the electrical dipole oscillating along the axis of the coil can be neglected since the coil is flat. The radiative losses, $R_{rad}$, are given by:

$$R_{rad} = \sqrt{\frac{\mu_0}{\epsilon_0}}\left[\frac{\pi}{12}n^2\left(\frac{\omega r}{c}\right)^4\right].$$

where $\mu_0$ and $\epsilon_0$ are the permeability and permittivity of free space, respectively, $n$ is the number of turns, $r$ is the radius and $c$ is the speed of light.

The resistances are responsible for the losses occurring at the coil thus they are used to calculate the damping factor, which is expressed as

$$\Gamma = \frac{R}{2L}.$$

How well the coil operates can be quantified by the Q-factor. Ripple currents are lower for higher Q-factors. The Q-factor is given by:

$$Q = \frac{\omega_0}{2\Gamma} = \frac{2\pi fL}{R}, \tag{8.15}$$

and can be calculated from the resistive and radiative quality factors:

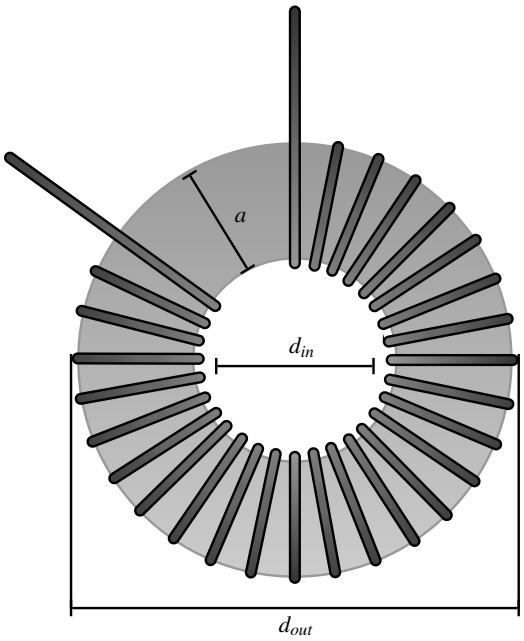
$$Q_{abs}^{-1} = Q_{res}^{-1} + Q_{rad}^{-1}.$$

Typically, the absolute quality factor will be governed by the radiative quality factor since $Q_{res} > Q_{rad}$.

### 8.3.3 Material budget

The material budget for the DC-DC powering scheme is investigated in section 7.5.4. The circuit for the planar coil and toroidal coil converters is expected to be identical. Therefore, a comparison need only consider the coils themselves. Assuming both coils are made of copper then the amount of material can be determined by simply the volumes of the two coils. The STV10 toroid coil is a 220 nH inductor. Using the equation in Figure 8.21 the exact dimensions of such a coil to achieve a 220 nH toroid are: 23 turns ($N$), an inner radius ($r_{in}$) of 2 mm, an outer radius ($r_{out}$) of 4.5 mm and a thickness ($a$) of 2.5 mm.

The STV10 toroid uses a 190 μm thick and 200 mm long copper wire. Thereby, the 220 nH toroid coil is made of ~23 $mm^3$ of copper. In contrast, to match the inductance of the toroid, a dual-layer spiral coil would have the following dimensions: 3.5 turns, outer diameter of 7.7 mm, an inner diameter of 3.1 mm and a 0.5 mm spacing between the two coils and would use ~5.55 $mm^3$ of copper, which is a substantial reduction compared to the toroid coil.




$$L = \mu N^2 \left(\frac{a}{\pi}\right)\left(\frac{d_{out}}{d_{in}}\right)$$

Figure 8.21: The toroidal coil geometry. The equation (right) is used to calculate the inductance value of the toroidal coil. In the equation, $\mu$ is the permittivity, $N$ is the number of turns and the other variables are the dimensions of the toroid (left).

### 8.3.4 Comparison with simulation

Modelling the coils in Ansys Maxwell[49] allows the prediction of the coils' electrical properties. The models can be used to verify the inductance value that has been calculated using the empirically derived equations. The solutions obtained from the Maxwell package are based on the eddy current simulation which was found to be most suitable for modelling inductors. The solution would allow the resistance of the coil to be calculated, which is a function of the skin-depth, and the inductance of the coil. These two are then combined to calculate the Q-factor of the coil. Ansys Maxwell will be used to simulate a wide variety of designs which will ultimately be judged by their Q-factor. The convenience of simulation over lab testing saves time, effort and cost. Simulation can automatically be set-up to go through a series of designs and provide

good results.

Using the dimensions of the coils from section 8.3.3, the toroidal coil was simulated at a solution frequency of 2 MHz. The simulated magnetic field can be seen in Figure 8.22. The resulting inductance and resistance were 209 nH and 69 mΩ, respectively. The inductance is within 5% of the measured value which is expected.

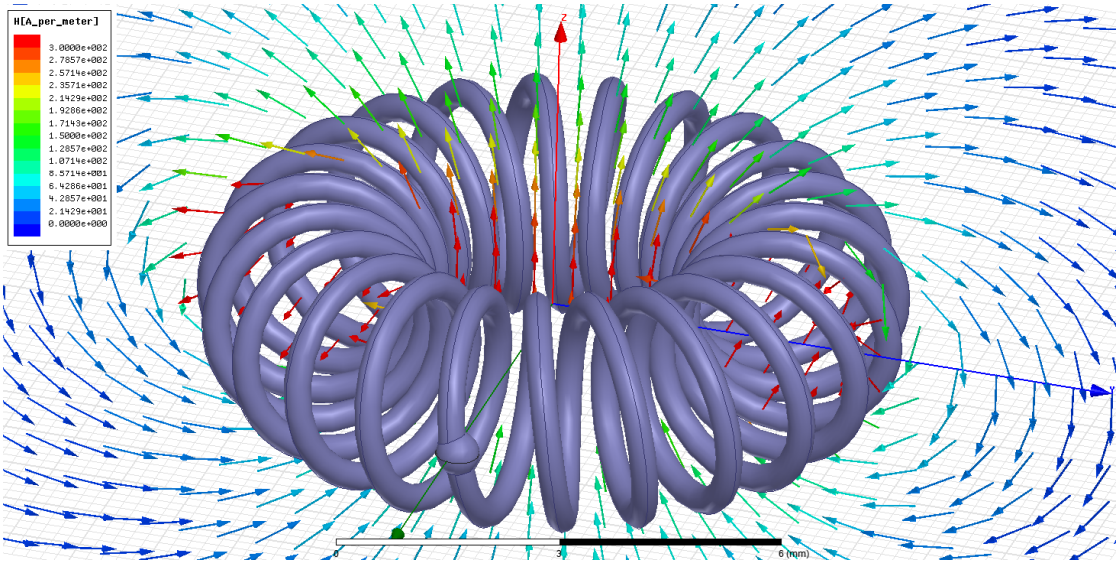



Figure 8.22: A model of a toroid coil with the simulated magnetic field.

Similarly with the spiral coil, the dimensions calculated in section 8.3.3 are used. A single planar coil with the same dimensions can be seen in Figure 8.23. The dual-layer spiral coil with a 0.5 mm spacing between the two layers is shown in Figure 8.24. The simulated magnetic field of the dual-layer coil can be seen in Figure 8.25, the resulting inductance and resistance are 203 nH and 116 mΩ, also within the 5% uncertainty of the measured value.

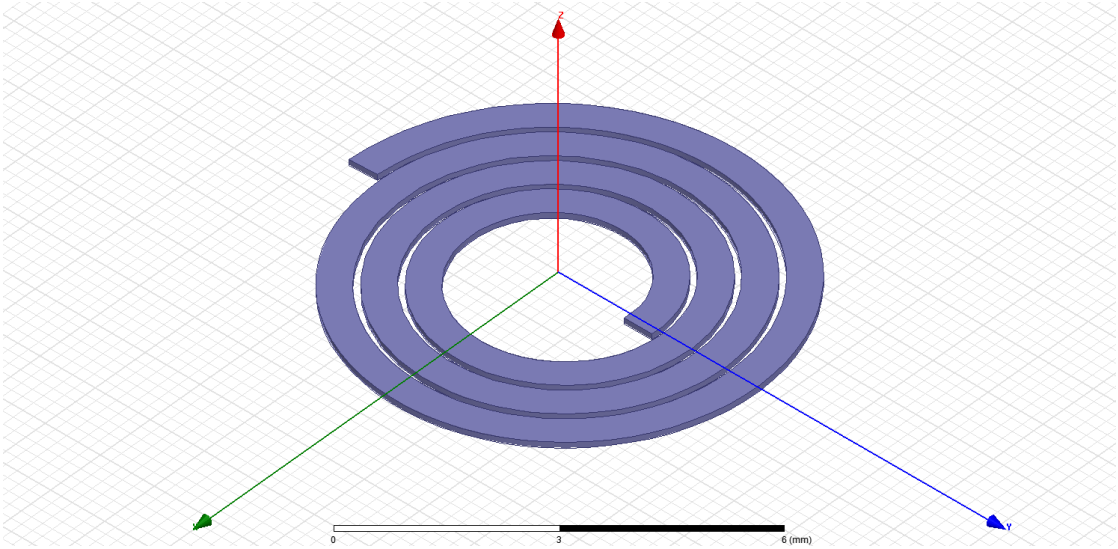



Figure 8.23: A 3D model of a single spiral coil. N = 3.5, $r_{in}$ = 3.1 mm, $r_{out}$ = 7.7 mm, $w$ = 0.5 mm and $s$ = 0.1 mm.

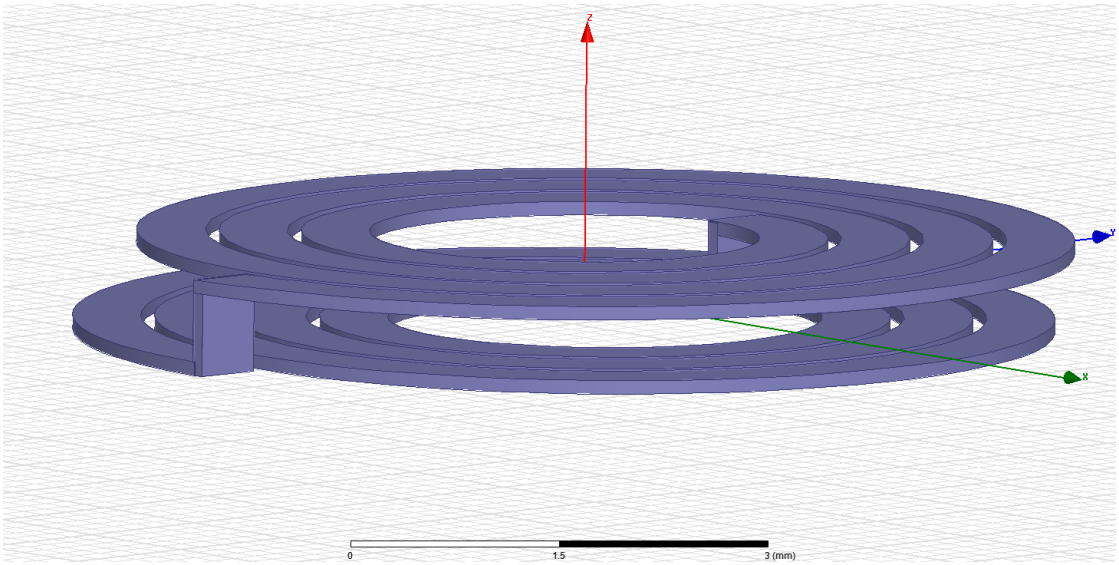



Figure 8.24: A 3D model of a dual-layer spiral coil. Spacing between two coils = 0.5 mm.

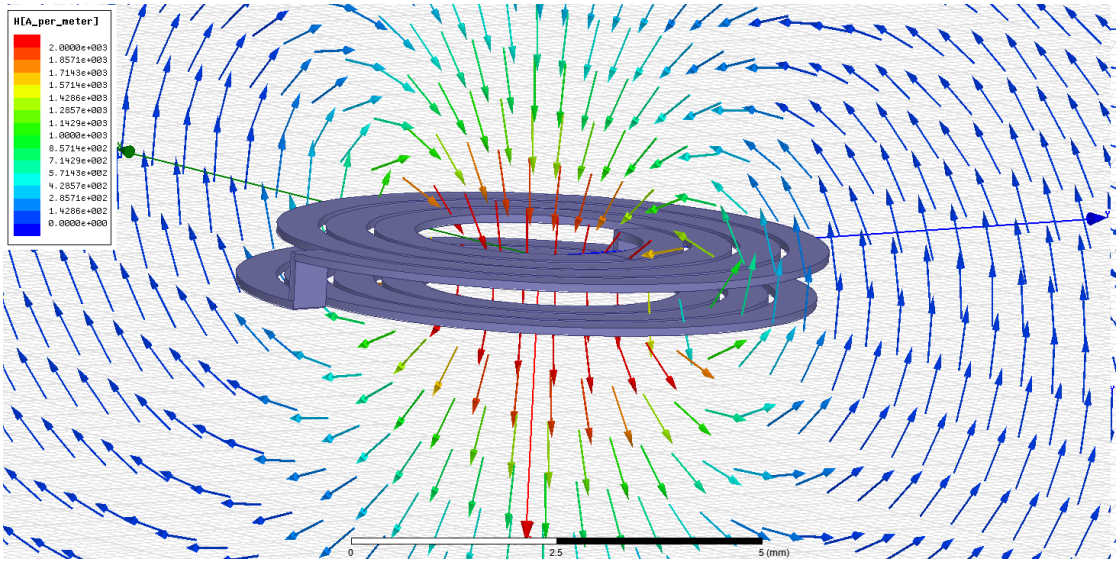



Figure 8.25: The simulated magnetic field of the dual-layer spiral coil.

In addition, the Maxwell package allows the geometry information such as volume and surface area to be easily extracted. The latter is particularly important for its relation to the resistance of the coil since due to the skin-depth effect, the greater the surface area the lower the resistance. The resistance of the coil is quite important due to its relationship to the Q-factor. The resistance is responsible for the energy losses in the coil, thus lower resistance means lower Q. The resistance here, however, is not the DC resistance of the coil but the resistance or the impedance of the coil at the operating frequency, which is in this case 2 MHz.

Using the values obtained from the simulation we can calculate the Q-factors using equation 8.15.

$$Q_{toroid} = \frac{2\pi(2\times10^{6})(209\times10^{-9})}{69\times10^{-3}}, \qquad Q_{spiral} = \frac{2\pi(2\times10^{6})(203\times10^{-9})}{116\times10^{-3}}$$

$$= 29.3, \qquad = 22.7.$$

A higher Q-factor is calculated for the toroid but the difference is not significant. There is definitely room for improving the planar coil Q-factor, but manufacturing limitations (track width, thickness, etc.) have to be set first in order to evolve the design around them.

### 8.3.5 Efficiency and noise performance of the planar DC-DC converter

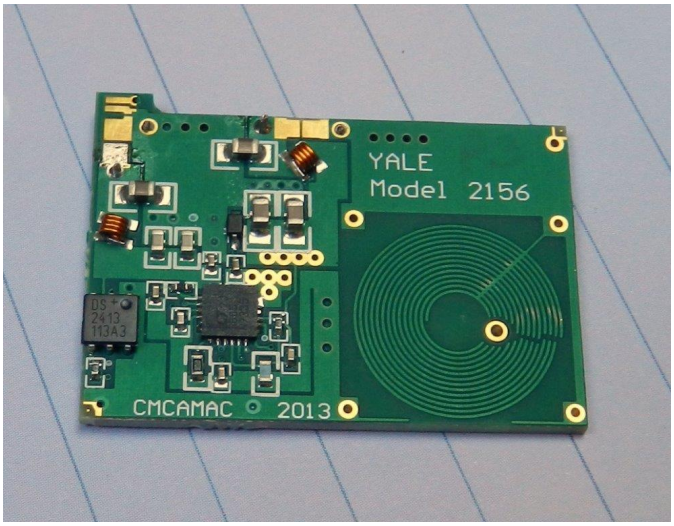



Figure 8.26: A planar coil PCB produced by Yale University[69].

A variety of planar coil DC-DC converters were designed and built at Yale University. The circuit is identical to the toroidal coil DC-DC converter with the exception of the built-in planar coil. The converters performance is judged by the efficiency of the converter and the impact of the noise on the readout modules. It must at least match the performance of the toroidal coil converter.

#### Noise performance of the planar DC-DC converter

DC-DC converters can add noise to the readout system in two different ways: noise due to EM emissions and noise related to the converter's power delivery (i.e. ripple current). The latter

has been tested at the University of Liverpool[50]. The results have shown a very promising performance for the powering of a single readout module using the planar coil converter. Slightly better noise results; about 10 electrons less (from ~600) for the measured ENC compared to the toroidal coil noise input ENC. This was done with the planar converter connected to the module but placed a few centimetres away from the sensors. Placing the converter at close proximity to the sensors exposes the module's vulnerability to EM emissions. An unshielded coil is expected and has been confirmed to introduce noise to the readout electronics, therefore copper tape was used to shield the coil. The copper tape was successful in reducing the ENC from ~1200 electrons down to ~600 electrons. This noise performance is considered to be acceptable but is still slightly higher than that of the toroidal coil.

#### Efficiency of the planar DC-DC converter

The toroidal DC-DC converter was designed to have an efficiency between 75% and 85%. The efficiency is associated with many factors but the only difference between the toroidal and planar converters is the coil. There should be no major difference between the efficiencies if the planar coil has an inductance equal to the toroidal coil. An unshielded planar coil converter has shown an efficiency of ~80% but a decline in efficiency was observed with a shielded coil. The measured efficiencies of the planar converter against input voltage can be seen in Figure 8.27.

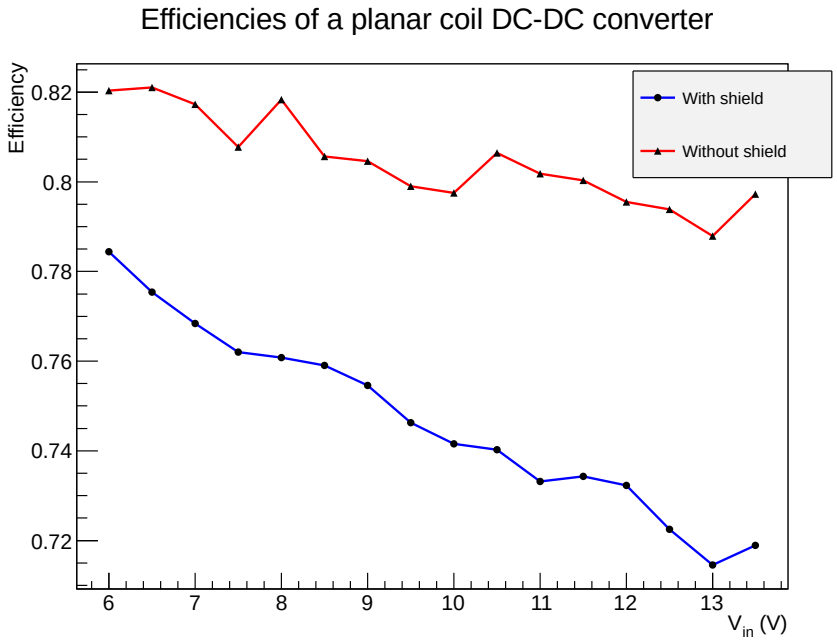



Figure 8.27: The efficiency of the shielded and un-shielded planar coil converter as a function of the input voltage.

### 8.3.6 Shielding

Shielding is an essential element of the DC-DC coil design. This became exceptionally important after the electromagnetic field susceptibility of the stavelets was tested and confirmed. The smaller size of the planar coils allow them to be embedded within the PCB of the converter with the possibility of embedding the shield in the PCB as well. Whether the shield is embedded or not, it is still expected to be much smaller in size than the toroidal coil shield. This means that the tilt angle of the barrel staves can be reduced. The close proximity of the shield to the coil has, through eddy currents, some ramifications particularly while it eliminates the EM emissions, the electrical behaviour of the coil is distorted and the inductance is changed. The effect of the shields on the coil's inductance can be seen in Figure 8.29. A schematic of the coil and

the shielding plates can be seen in Figure 8.28.

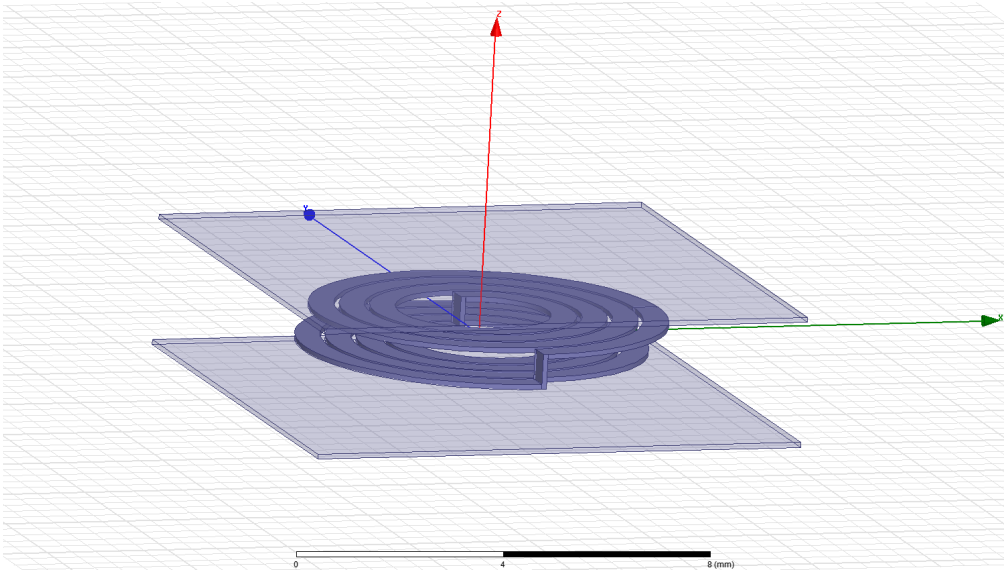


Figure 8.28: The planar coil with two copper shields one on each side.

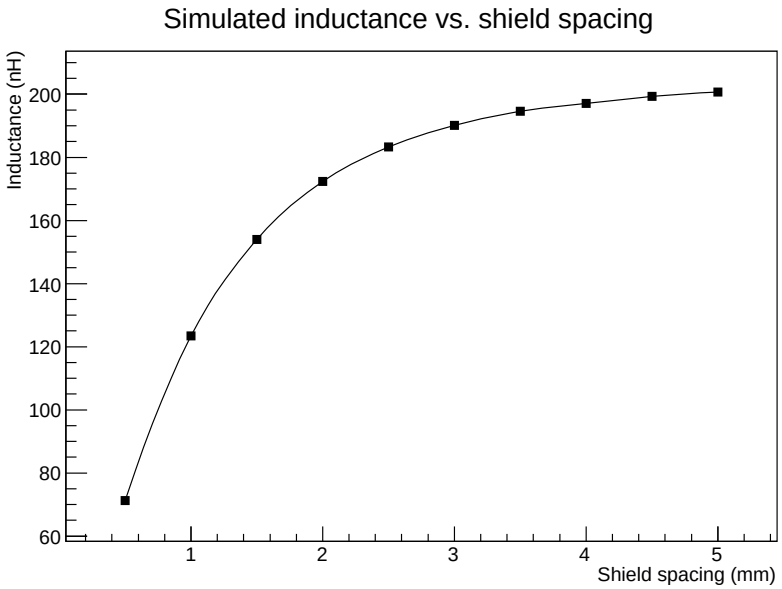



Figure 8.29: The simulated inductance value plotted against the shield spacing.

The relationship between the inductances of the shield and coil have shown the importance of including the shielding in the layout design of the inductor. The empirical formulae from Section 8.3.2 were all derived for shield-less coils therefore they are not applicable for modelling shielded inductors, but they remain a good starting point and the design will be improved with simulation. This will be an iterative modelling process with the aim to find a planar spiral coil inductor that can sit between two copper sheets and achieve the desired inductance with a high Q. One way to decrease the eddy current effects is to use patterned or slotted shields, as shown in Figure 8.30. This decreases the area over which eddy loop currents can be produced. The

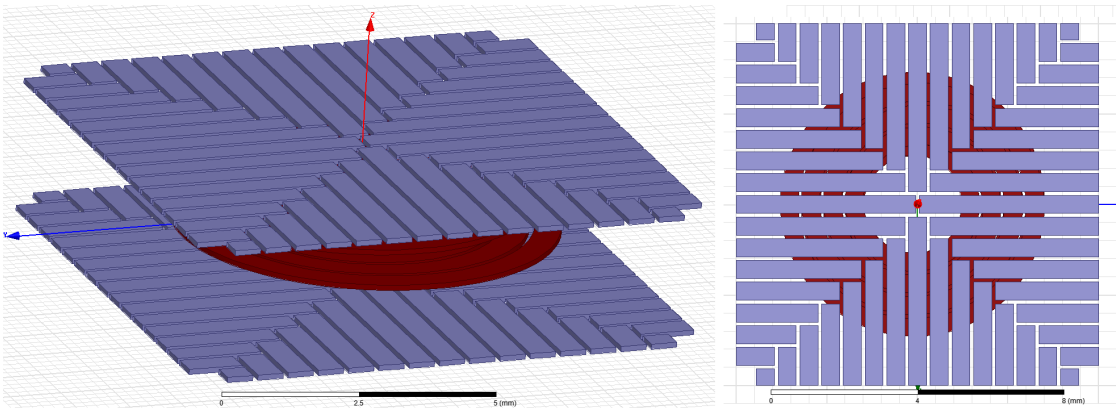


Figure 8.30: A patterned shield to decrease the eddy current effects on the coil.

inductance value of the coil with the patterned shield was therefore seen to be less affected. This is shown in Figure 8.31. However, the effectiveness of the patterned shield is not expected to be very good in terms of the E-field attenuation. Nevertheless it demonstrates the importance of considering the eddy currents. Ultimately, the shield has to be grounded and cover the entire coil, as shown in Figure 8.32. The coil inside the box is expected to have an inductance of 260 nH, but the impact of the shield reduces this to ~216 nH and with a resistance of 122.25 mΩ the coil has a Q-factor of 22.2, which is acceptable.

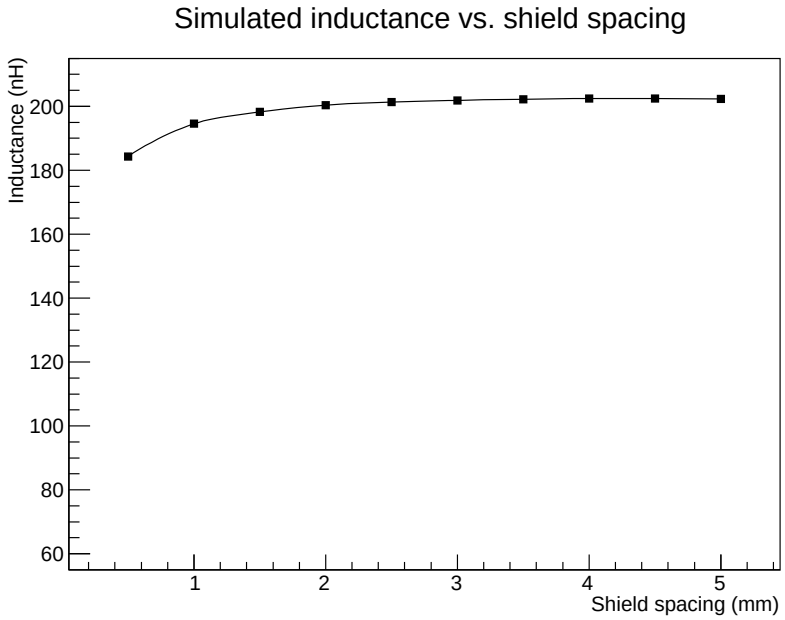



Figure 8.31: The simulated inductance plotted against the patterned shield spacing.

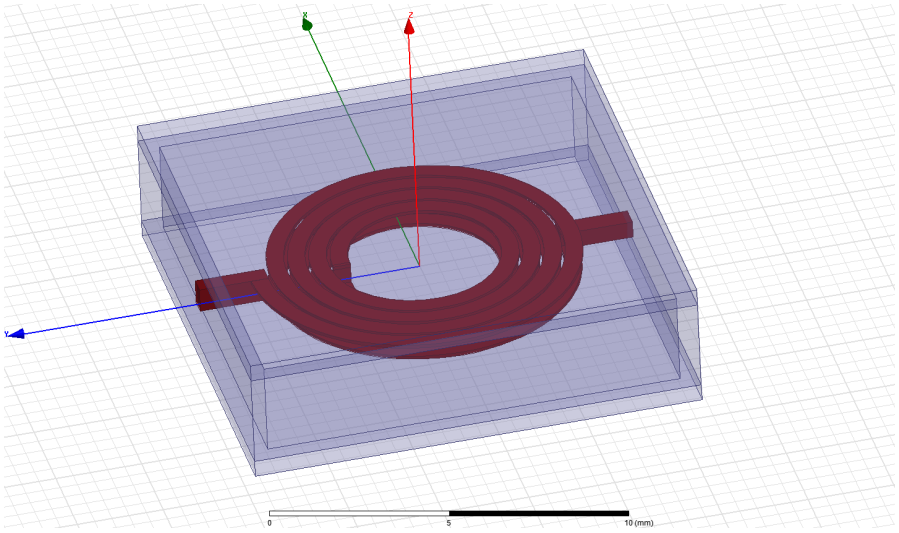


Figure 8.32: A fully shielded planar coil with a simulated inductance of 215.85 nH. N = 3.5, $D_{in}$ = 4.3 mm, $w$ = 0.5 mm, $s$ = 0.1 mm and 0.5 mm spacing between the two layer.

# 9 The Stavelet

## 9.1 Stavelet description

The concept of the stave in the new strip tracker layout reduces the radiation length by minimizing the material used for cooling and powering and also minimizes the costs of production and installation. The stavelet is a proof-of-concept device: it is a shortened stave with a fewer number of readout modules. Despite the variations in the number of modules, at the heart of the stave/stavelet there is a 96 mm square silicon strip sensor fabricated in an n-in-p Float Zone (FZ) technology[36], consisting of a $n^+$ implant on a p-bulk. The sensors are divided into four columns with 1280 strips each. The single sided sensors are glued on both sides of a composite support structure. The cooling pipes are incorporated inside the structure and kapton flex circuits, known as bus tapes, lay between the sensor and the structure. The bus tape is responsible for routing the signals and power from the modules and the End Of Stave (EoS) card. The sensor is serviced with a hybrid glued on the sensor itself. The hybrid contains two columns of ABCN250 ASICs with 128 readout channels each and is controlled by the Basic Control Chip (BCC), which allows a distinct configuration for every hybrid. The BCC also provides AC decoupling for the LVDS control signals; a crucial function when powering the stave/stavelet serially. Finally, the EoS collects and buffers the signals from all the hybrids to facilitate the communication between the stave/stavelet and the data acquisition system (DAQ).

The final design of the stave will have the ABC130 readout chip replace the ABC250 chip. However, there will be half the number of ABC130 chips since it has double the number of inputs, as will be explained in Chapter 10. The BCC will also be replaced with a Hybrid Controller Chip (HCC) [].

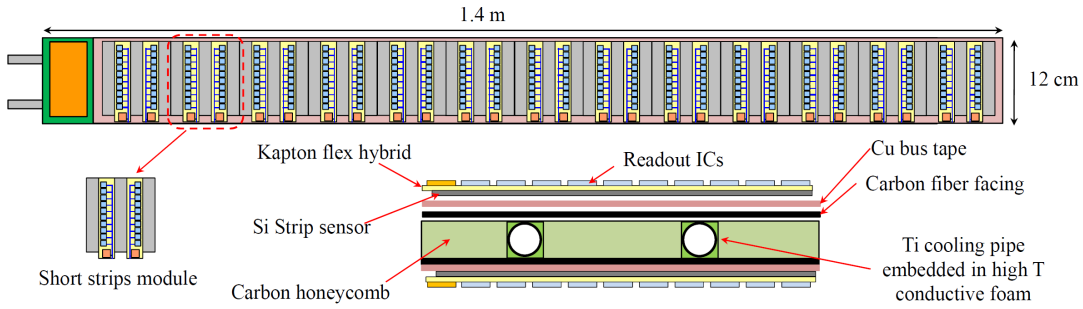



Figure 9.1: A sketch of the layout and cross-section of the stave[58].

Two versions of the stavelet were constructed to evaluate the two proposed powering schemes (see section 7). Both stavelets are single sided with four modules[1] each and use chilled water for cooling.

### 9.1.1 DC-DC stavelet

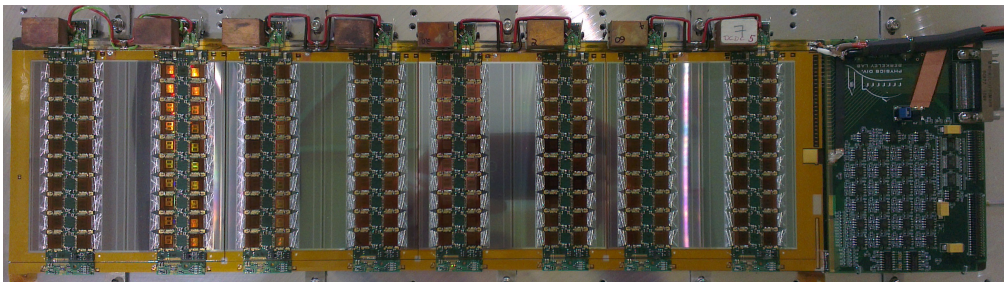


Figure 9.2: A picture of the DC-DC stavelet.

[1] Two hybrids make one module.

In the DC-DC stavelet the hybrids are individually powered with a STV10 DC-DC converter (refer to Section 8.1). The ABCN25 requires 2.5 V to operate but the DC-DC converters were set to provide 2.6 V to compensate for the power lost in wire-bonds between the converter and the hybrid. The converter is supported with a small aluminium extension that is glued to the upper side of the hybrid, this also improves the converter's cooling. In order to accommodate the power requirements of the DC-DC converters, the EoS power feed lines had to be bypassed with a copper wire to be able to handle the higher current and the bus tape had to be modified to add parallel power traces. The power to the DC-DC converters comes from an external commercial power supply.

### 9.1.2 Serial powered stavelet

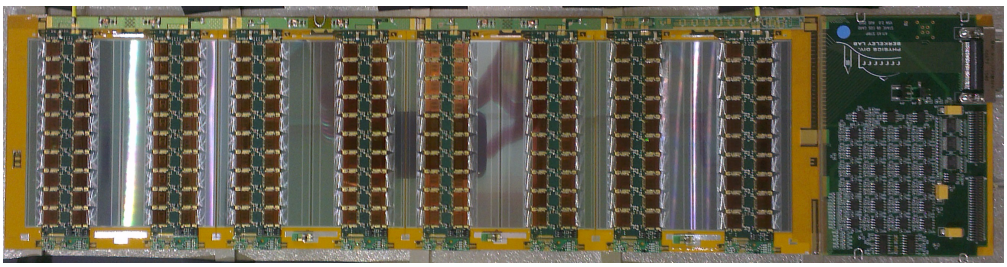


Figure 9.3: A picture of the serial powered stavelet.

The serial powered stavelet has a constant current running through the 8 hybrids. Each hybrid uses its share of the current to maintain a fixed 2.5 V drop across it. The bus tape (Figure 9.4) delivers the current on a single line as opposed to the parallel lines used for the DC-DC powered stavelet. The SP stavelet is powered with an external current source.

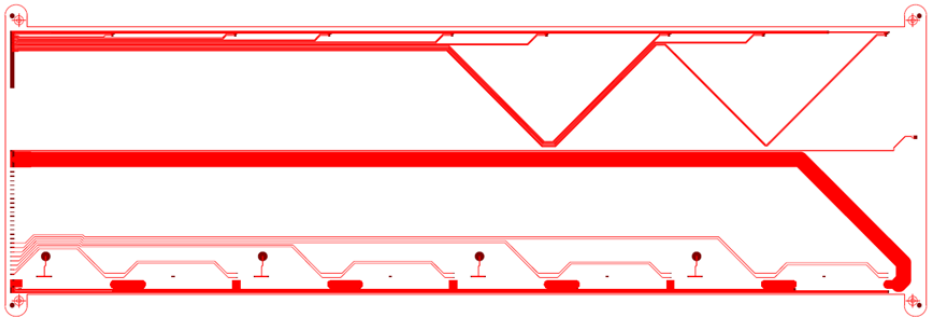


Figure 9.4: The SP bus tape. For DC-DC, the power section is cut off and replaced by a custom one[59].

## 9.2 Analogue tests

Analogue tests are used to evaluate the performance of the readout system and determine the correct configuration for the system. In the following sections, the tests performed to evaluate the stavelets and the DAQ system facilitating these tests will be explained and discussed.

### 9.2.1 Data acquisition software

The DAQ software used to readout the stavelet is based on the old SCTDAQ system. This system used the legacy VME hardware MuSTARD[61], CLOAC[62] and SLOG[63] and was capable of reading a few ABCN25 hybrids but was not scalable to readout a full stavelet. The new system uses a generic DAQ board, the High-speed IO board (HSIO), which was initially designed at SLAC[64]. The board has a Virtex-4 FPGA at its heart and incorporates a large number of IO ports. To be compatible with the HSIO, the SCTDAQ had to be updated. To take advantage of the high speed Ethernet interface on the HSIO, the SCTDAQ was upgraded to handle packet based communication.

### 9.2.2 Strobe delay tests

The strobe delay tests define the configuration to ensure that the discriminators are always synchronous with the calibration signal. A discriminant that is too quick or too slow will miss the signal. To avoid this, the strobe delay test changes the phase of the charge injection signal relative to the trigger command. The delay is relative to the system's clock. A 6-bit register is used to record the delay giving a range of delay from 0 to 63 (every DAC step is ordinarily ~0.8 ns). To ensure a 100% hit efficiency while performing the test, a 4 nC charge is injected and the discriminator threshold level is set at 2 nC. The value of the delay is chosen at the peak of the response, as shown in Figure 9.5.

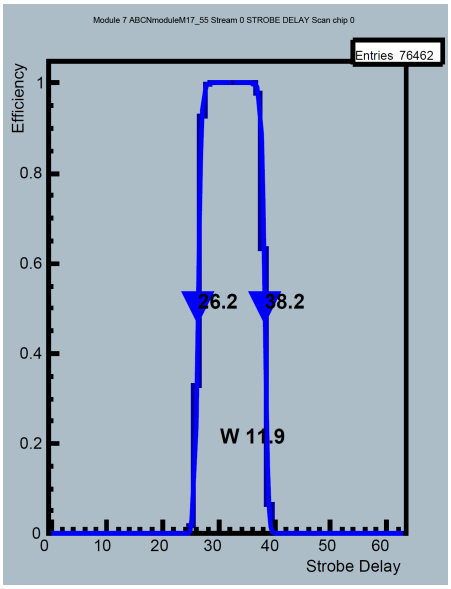



Figure 9.5: An example of strobe delay occupancy plot obtained from the SCTDAQ software.

When a module is calibrated at a certain temperature, at low temperatures threshold variation can appear between the channels. A possible cause for this is the leakage current in the shaper DAC[66]. To overcome this problem, the DAQ software offers two strobe delay options that

set the delay setting at 40% and 25% of the working region, respectively. Using a delay setting closer to the rising edge was shown to reduce the effect of the Large Gain Spread (LGS) where different chips will have varying gain responses, this is particularly relevant at cold temperatures where LGS was seen to have a higher influence on the chips. The 40% strobe delay plot is illustrated in Figure 9.6.

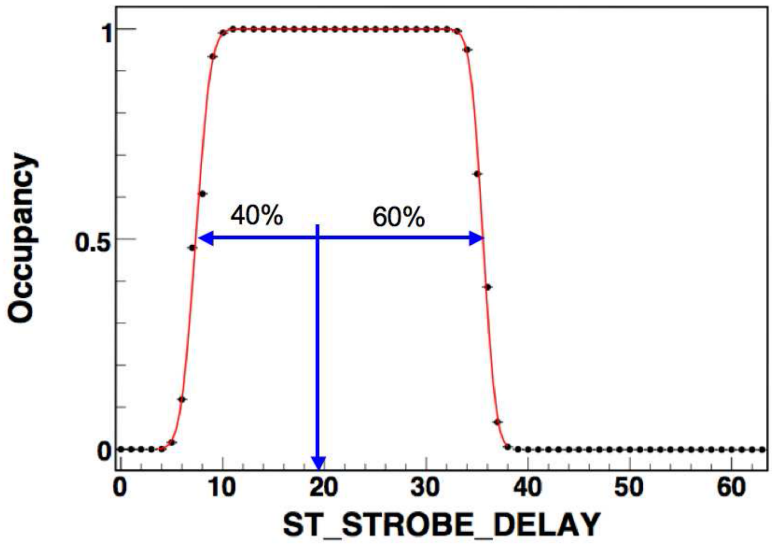



Figure 9.6: A strobe delay occupancy plot. The optimal strobe delay setting is chosen at 40% of the working region[66].

### 9.2.3 Threshold scan

Threshold scans form the basis of all analogue tests. The scan reports the occupancy of each channel (with or without an injected charge) against the threshold level. This is then fit with an error function, known as S-curve. The threshold at which the occupancy is 50% is known as $V_{t50}$ and is measured in mV. The threshold scan reports the value of the $V_{t50}$ and the width of the channel distribution from the S-curve. An S-curve of a chip can be seen in Figure 9.7.

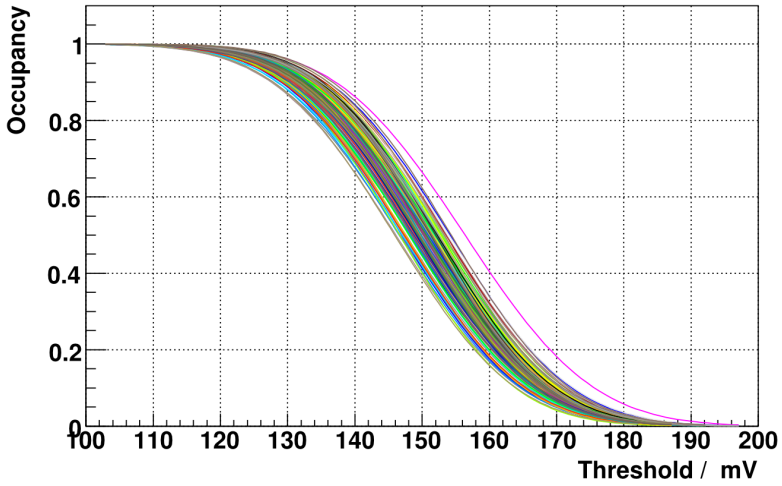



Figure 9.7: The threshold scan for all channels on a single chip.

### 9.2.4 Trim Range

The response of channels varies from one channel to the other. Trimming is used to make sure that the variation between channel responses is minimized. It is a crucial test to ensure the stability of the system, especially after irradiation. Threshold scans are performed for eight possible trim ranges. The $V_{t50}$ values, obtained from threshold scans, are plotted against trim DAC values to estimate of the best trim value.

### 9.2.5 Three point gain scans

The three-point-gain scan performs three threshold scans for three levels of injected charge. SCTDAQ offers two charge injection options, 1 nC and 2 nC with a respective threshold scan of 0.5 nC, 1 nC, 1.5 nC and 1.5 nC, 2 nC, 2.5 nC. For every given charge, the threshold scan measures the output of a channel while varying the threshold level. The gain of each input channel (slope mV/fC) and the discriminator offset (mV at 0 fC) are then determined from a linear fit of $V_{t50}$ for the three injected charges, as shown in Figure 9.8. The input noise is

calculated by measuring the output noise and dividing it by the gain. This gives the noise in fC, to obtain the Equivalent Noise Charge (ENC) the noise charge is multiplied by the number of electrons in 1 fC, which is 6241.

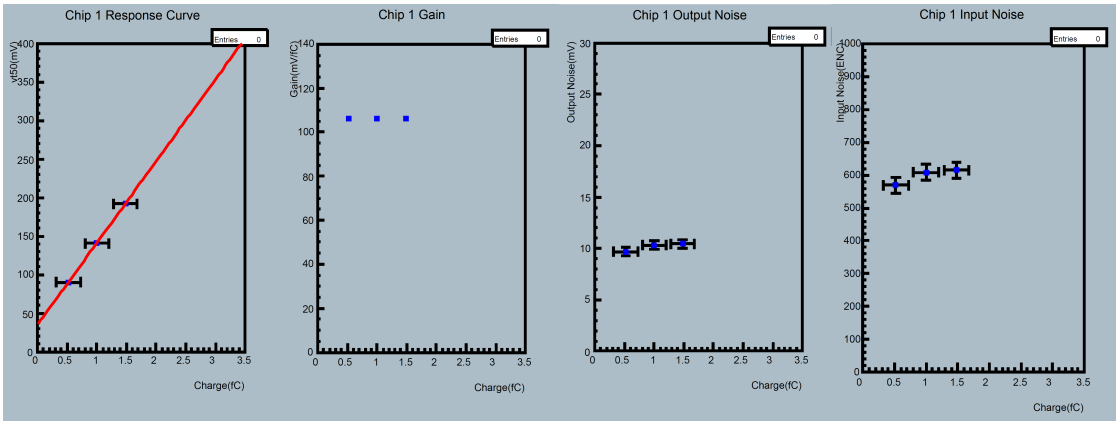



Figure 9.8: The plots from a three-point-gain scan. From left to right: (1) The response curve, a linear fit of the $V_{t50}$ values for the three injected charges. (2) The gain, measured for the three injected charges. (3) The output noise, measured for the three injected charges. (4) The input noise, measured for the three injected charges.

### 9.2.6 Double Trigger Noise tests

The Double Trigger Noise (DTN) tests help identify spurious hits related to readout activity which might be correlated to optical and electrical pick-up. The test sends two triggers with a controlled time spacing in-between, while maintaining a fixed threshold level. The first trigger probes the real occupancy of the detector and the second trigger reports on the occupancy as a result of the previous trigger. The time spacing between the triggers is varied to properly examine the readout effect.

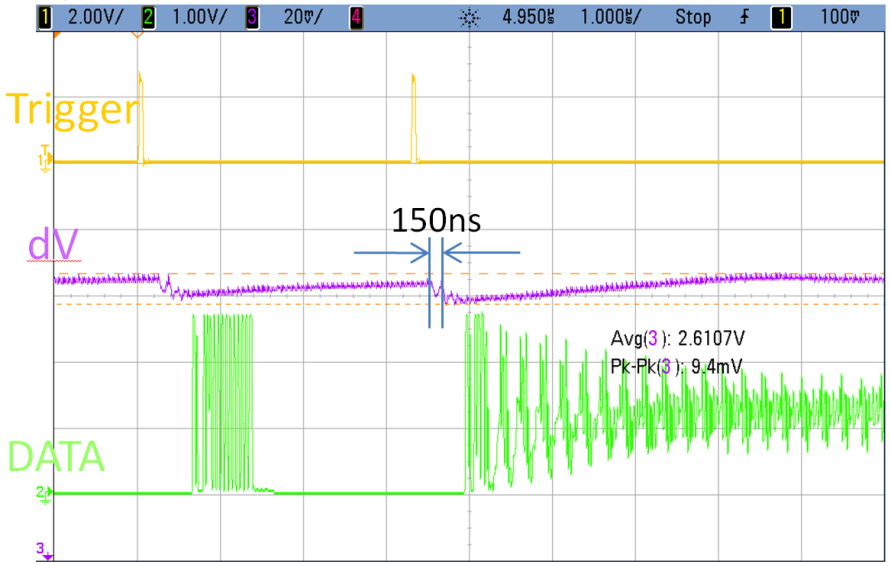



Figure 9.9: The double trigger noise test viewed with an oscilloscope[59]. The middle trace is from a differential probe connected between the power rails. The other traces are labelled.

Figure 9.9 shows the data lines of a stavelet probed with an oscilloscope. The first trace in the scope view shows when the trigger pulses come in and the third trace shows the data being generated as a result of the trigger. After the first trigger, the module returns a fixed length zero occupancy event but on the second trigger a longer length event was reported. The DTN test was able in this case to detect the signal which has found its way back to the front end. The second trace shows the differential voltage between the two power rails; another indication of the signal finding its way back to the front-end.

## 9.3 Stavelets' operating conditions

Four controllable parameters affect the operation of the stavelet: the high voltage (to bias the sensors), the low voltage (to power the readout electronics), the level of cooling and the humidity. The first two: high voltage and low voltage have been tested to verify their effect on the stavelet.

The effect has been quantized with the means of a three-point-gain scan to measure the input noise. It is expected that the stavelet will report different noise levels and behaviour while varying these conditions as the four sensors in every stavelet have different configurations and different electrical characteristics. The configurations and characteristics are summarized in Table 9.1 and 9.2 for DC-DC and SP stavelets, respectively.

| | | | @ 250 V | | |
|---|---|---|---|---|---|
| | **FZ type** | **Isolation (concentration)** | **Capacitance** | **Leakage current** | **Depletion voltage** |
| Module 0 | FZ2 | p-stop ($1 \times 10^{13}$) | 2.63 ± 0.02 nF | 10.0 ± 0.08 µA | 145 ± 1 V |
| Module 1 | FZ1 | p-stop ($4 \times 10^{12}$) | 2.95 ± 0.02 nF | 0.24 ± 0.002 µA | 240 ± 2 V |
| Module 2 | FZ2 | p-stop ($1 \times 10^{13}$) | 2.63 ± 0.02 nF | 9.29 ± 0.08 µA | 130 ± 1 V |
| Module 3 | FZ2 | p-spray ($2 \times 10^{13}$) | 2.63 ± 0.02 nF | 6.62 ± 0.05 µA | 130 ± 1 V |

Table 9.1: The DC-DC stavelet sensor information.

| | | | @ 250 V | | |
|---|---|---|---|---|---|
| | **FZ type** | **Isolation (concentration)** | **Capacitance** | **Leakage current** | **Depletion voltage** |
| Module 0 | FZ1 | p-stop ($4 \times 10^{12}$) | N/A | N/A | 202 ± 2 V |
| Module 1 | FZ2 | p-spray ($2 \times 10^{12}$) | 2.61 ± 0.02 nF | 6.63 ± 0.05 µA | 140 ± 1 V |
| Module 2 | FZ2 | p-spray ($2 \times 10^{12}$) | 2.63 ± 0.02 nF | 16 ± 0.13 µA | 110 ± 1 V |
| Module 3 | FZ1 | p-spray ($4 \times 10^{12}$) | N/A | N/A | 202 ± 2 V |

Table 9.2: The SP stavelet sensor information. The measurements were taken at the point of assembly and some sensors had missing information.

In the following sections, the results from the high voltage and low voltage scans are discussed.

### 9.3.1 High Voltage Scans

The noise measurements of the high voltage scans were done while ramping up and ramping down the voltage. The scan started at 20 V and reached 300 V with 20 V steps while performing

a three-point-gain scan at every step. The plots in Figure 9.10 and Figure 9.11 show the scan results for the DC-DC and SP stavelets, respectively.

The scans show a clear relationship between the noise and the sensor's isolation configuration. P-spray sensors show a relatively small change in noise while varying the high voltage while the p-stop sensors show a high difference in noise (~300 electrons) between partial depletion and full depletion. There is also a mismatch between the depletion voltage specified in Tables 9.1 and 9.2 and the value extracted from the noise measurements. Module 3 from the SP stavelet has a lower depletion voltage and module 2 from the DC-DC stavelet has a larger one. In addition, a distinctive feature can be seen from the DC-DC stavelet scans which shows a "'hysteresis"' effect. The ramp-up noise is lower than the ramp-down noise. The fact that this is seen only in the DC-DC stavelet and not on the SP stavelet, means that it cannot be attributed to the sensors but is a characteristic of the stavelet design. This is presently under investigation and measurements of the temperature of the readout chip during ramp-up and ramp-down are being undertaken for the two stavelets.

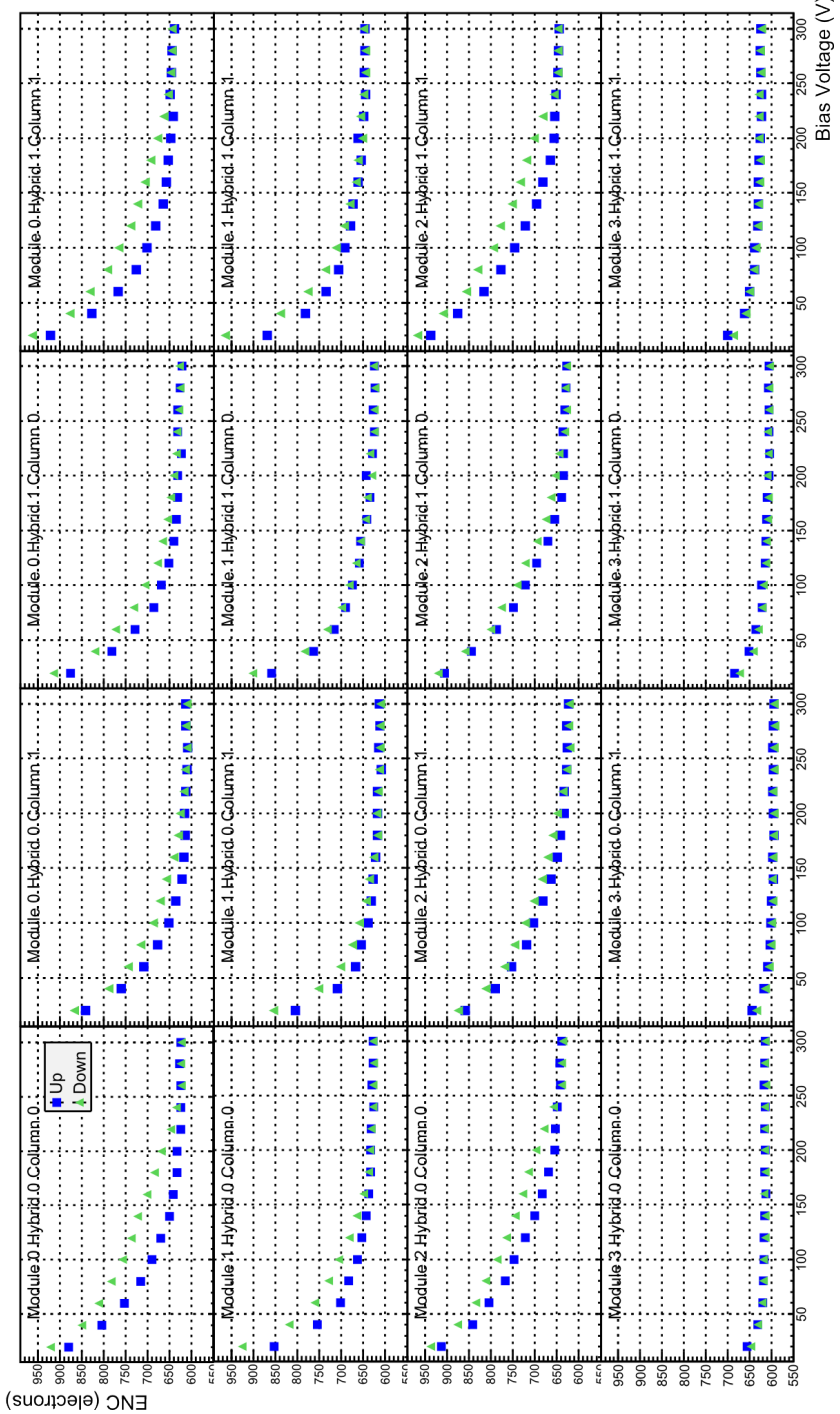



Figure 9.10: The DC-DC stavelet high voltage scan (Input noise (ENC) vs. Bias Voltage (V)): 20 V to 300 V with 20 V step. Up/Down is the ramping of the bias voltage. Each of the plots report the noise for every column (16 in total), the vertical axis for all the plots has a range from 550 to 950 ENC.

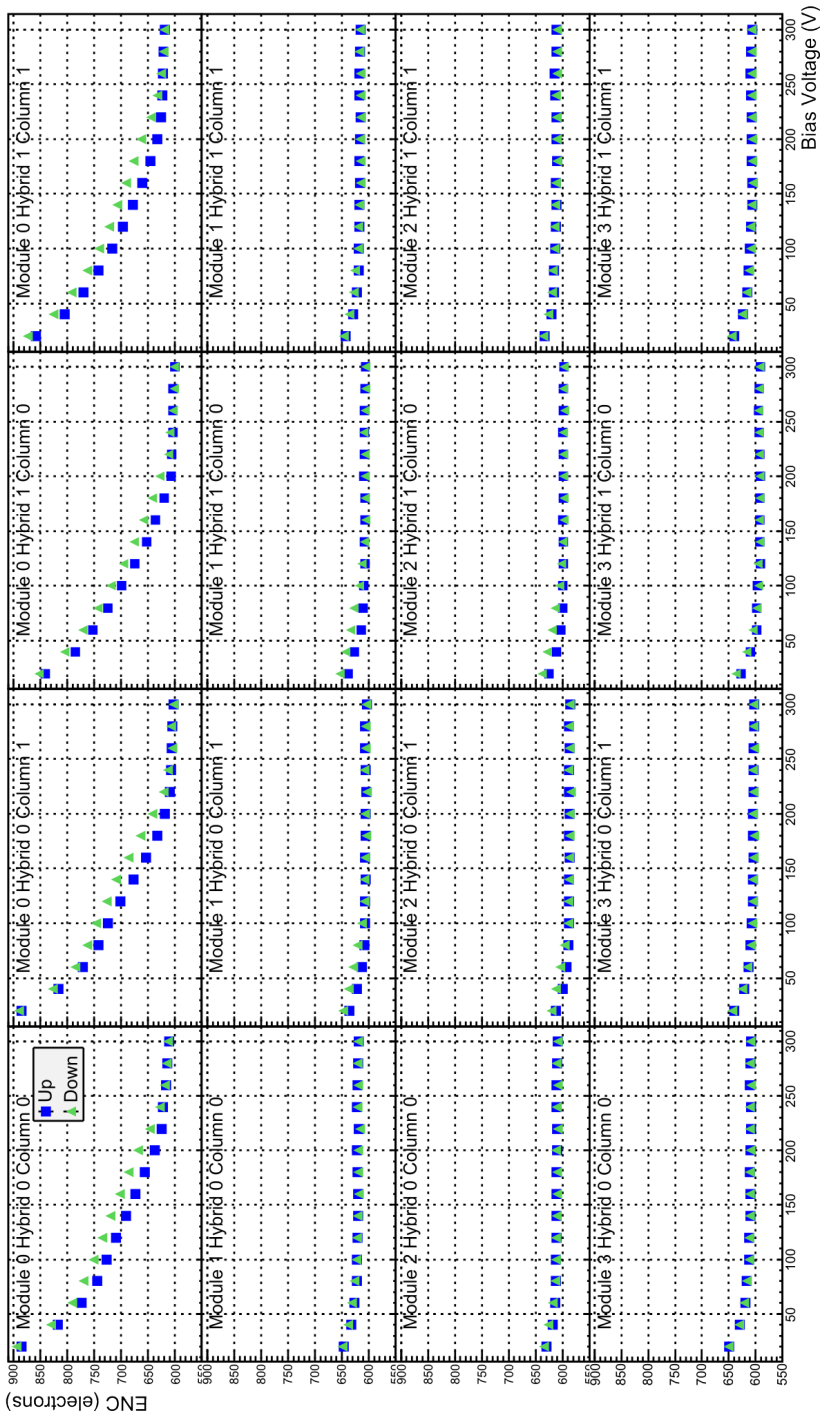



Figure 9.11: The SP stavalet high voltage scan (Input noise (ENC) vs. Bias Voltage (V)): 20 V to 300 V with 20 V step. Up/Down is the ramping of the bias voltage. Each of the plots report the noise for every column (16 in total), the vertical axis for all the plots has a range from 550 to 900 ENC.

### 9.3.2 Low Voltage/Current Scans

The SP and DC-DC stavelets are fundamentally different when it comes to low voltage powering, hence the tests described here are performed in two different ways. For the DC-DC stavelet, a low voltage scan from 9 V to 11 V with a single 3 point gain scan at every 0.2 V was performed. For the SP stavelet, a current scan from 9.5 A to 11.5 A with a single 3 point gain scan at every 0.1 A step was performed. The results of these scans can be seen in Figure 9.12 and Figure 9.13. For the DC-DC stavelet the voltage scan values fall within the recommended input voltage for the DC-DC converters. The voltage scan have shown no clear noise dependence on the LV value. On the other hand, the current scan for the SP stavelet show a noise-current dependence. There is a clear increase of upto 20 electrons between the noise at 9.5 A and the noise at 11.5 A for some modules. Thus from the noise point of view, it is advisable to operate the SP stavelet at the lowest recommended value of 9.5 A.

Along with the HV scans, two modules (module 0 and 3) have shown higher noise compared to the central modules. This feature could be associated with the path of the cooling pipes and the effectiveness of the cooling at the edges of the stavelet.

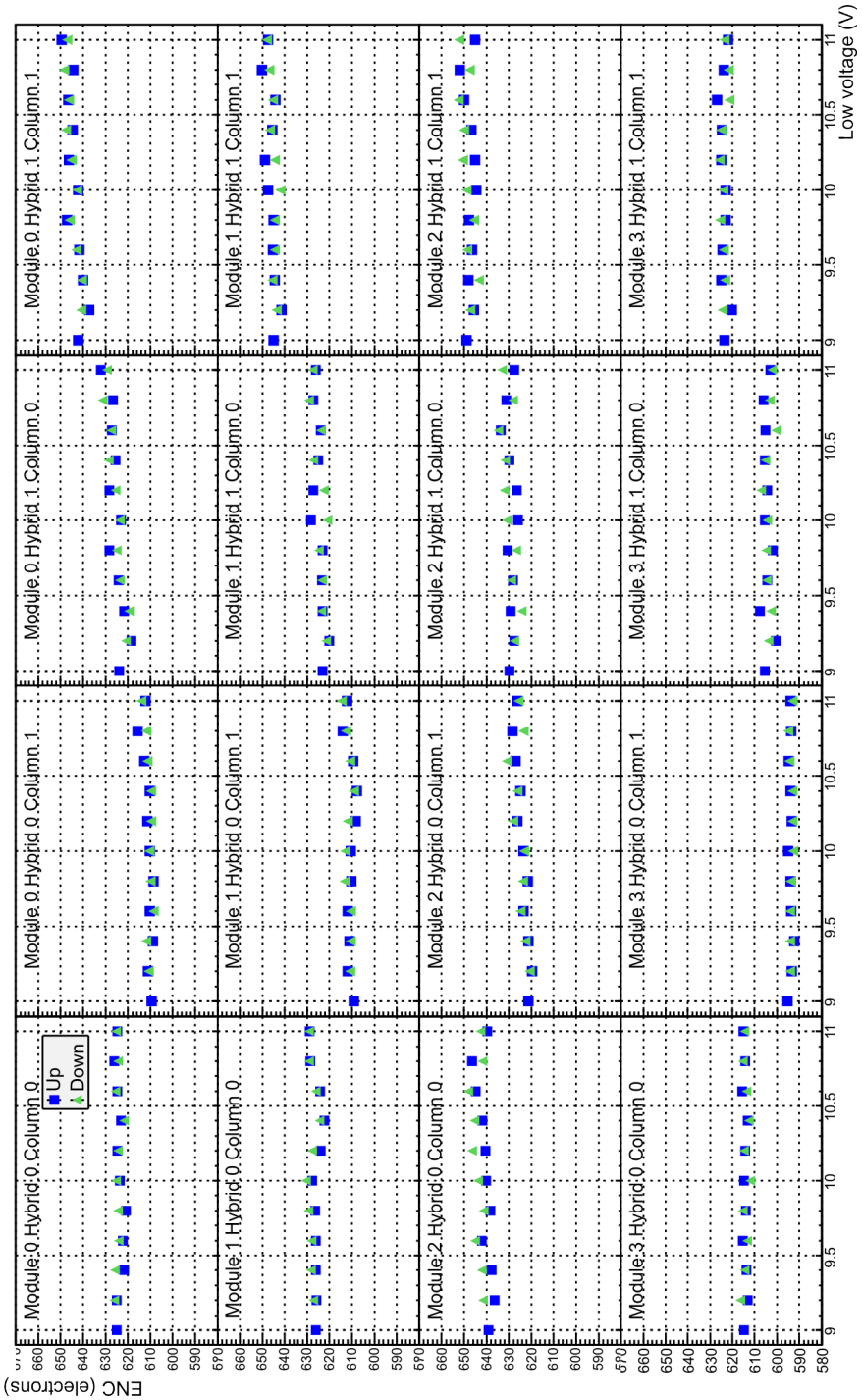



Figure 9.12: The LV scan on the DC-DC stavelet (Input noise (ENC) vs. Low Voltage (V)): 9 V to 11 V with 0.2 V step. Up/Down is the ramping of the LV supply. Each of the plots report the noise for every column (16 in total), the vertical axis for all the plots has a range from 580 to 670 ENC.

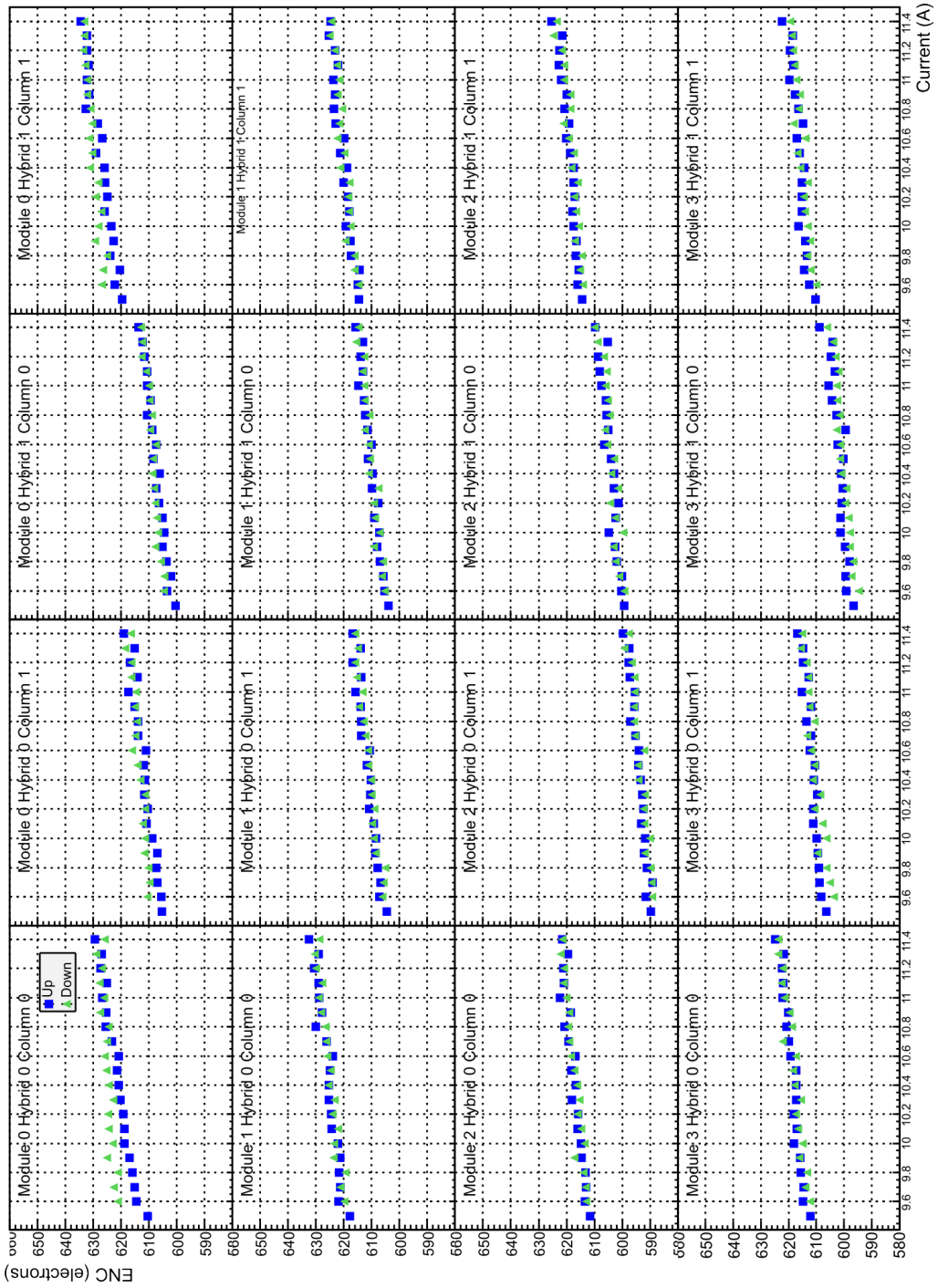



Figure 9.13: The current scan on the SP stavelet (Input noise (ENC) vs. Current (A)): 9.5 A to 11.5 A with 0.1 A step. Up/Down is the ramping of the current supply. Each of the plots report the noise for every column (16 in total), the vertical axis for all the plots has a range from 580 to 660 ENC.

# 10 Digital Design of the ABC130 readout chip

## 10.1 ATLAS Binary Chip (ABC) ASIC concept

The ATLAS Binary Chip (ABC) is a readout chip responsible for processing signals coming from the silicon strip sensors. The ABC ASIC has a set of analogue and digital requirements which it must provide. The analogue part, also known as the Front-End (FE), provides the following functionality:

1. Pre-amplification and pulse shaping: converting the injected charge at the strip sensor to voltage signals.
2. Amplitude discrimination: using comparators to only allow signals that are above a pre-defined threshold level to be processed by the digital part.

While the digital part should provide the following functionality:

1. Data latching from the FE channels and storage in a pipeline until needed.
2. Moving the data off the pipeline into a derandomizer buffer when a trigger signal is received.
3. Compressing the data from the derandomizer buffer using special Data Compression Logic (DCL).

4. Transmitting compressed data off the chip in compliance with the ATLAS protocol.
5. Error reporting in the case of
    a) Data unavailability.
    b) Buffer overflow.
    c) Configuration error.
6. Overcoming single chip failures.

The entire chip design must be able to provide all the required functions after full irradiation as expected at the ATLAS inner detector.

### 10.1.1 ABCD3TA

The ABCD3TA is the chip used in the current ATLAS strip detector. The chip was processed with DMILL[1] technology, a radiation hard technology comprising of CMOS, P-JFET and NPN transistors together with rad-hard resistors and capacitors. The DMILL process, which became available at a late stage of the ABCD chip development, allowed the combination of digital and analogue features on a single chip.

The SCT module is designed to be readout via two optical links. The twelve chips on the module have to share the two links where data from every six chips are multiplexed and routed to one link. No external readout controller chip was used and thus the readout control had to be integrated into the ABCD3TA chip design.

The chips route the data serially via a token-ring daisy-chain. Each chip can be configured as a master, slave or end. Redundant connections also exist to accommodate a chip failure and chips can be reconfigured accordingly.

[1] Durci Mixte sur Isolant Logico-Lineaire

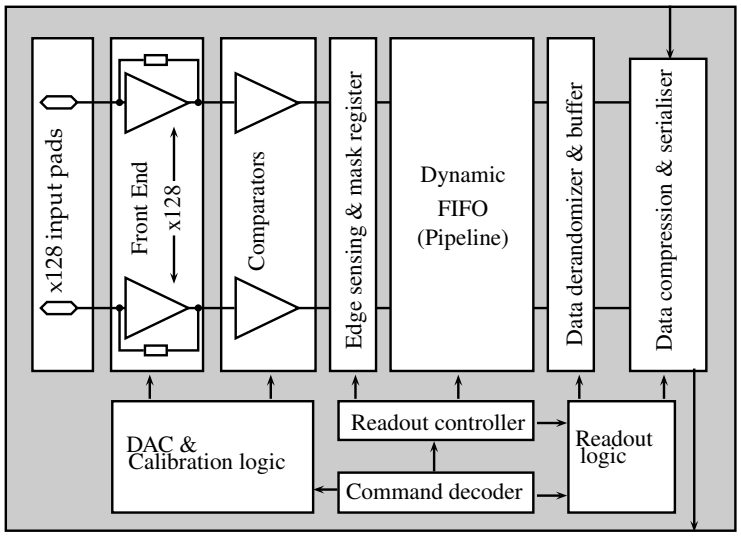



Figure 10.1: A block diagram of the ABCD3TA chip.

The ABCD3TA block diagram is shown in Figure 10.1. The data is prepared as follows:

1. At the collision rate, data from the silicon strip is kept in a pipeline waiting for an L1 trigger. The length of the pipeline corresponds to the latency of the L1 trigger which is assumed to be 3.3 μs.
2. With every L1 trigger, one event[2] is stored into the derandomizer buffer. Events reaching the end of the pipeline without an L1 trigger are discarded. The derandomizer buffer was chosen to be 8 events deep since according to Monte Carlo simulation, this guarantees less than 1% overflow losses in the buffer[71].
3. L1 triggering provides the first step towards data compression. Two other steps are then implemented, the first of which is only reporting addresses with valid hits and the second is reporting a single address for hits on neighbouring or adjacent channels.

The Data Compression Logic (DCL) examines hit patterns from a single event. A hit pattern is

[2] One event is made of three BC around the L0 trigger signal

a 3-bit pattern of three consecutive Bunch Crossings (BC) for one strip. The events are translated into 128 3-bit clusters and compared against a selectable criteria (Table 10.1). This allows the DCL to examine the three BCs of an event in parallel. If a channel row matches the criteria its 7 bit[3] address is created and added to a packet. If an adjacent hit is detected the ADJ bit is flagged. If no more hits are found the END bit is added.

| **Selection criteria** | **Hit pattern (First bit is the oldest)** | **Usage** |
|---|---|---|
| Hit | 1XX or X1X or XX1 | Detector alignment |
| Level | X1X | Normal data taking |
| Edge | 01X | Normal data taking |
| Test | XXX | Test mode |

Table 10.1: The data compression logic criteria: 0 is no hit, 1 is hit and X is don't care state.

### 10.1.2 ABCN250

The ABCN250 is a prototype chip which is intended to help with the development of the stave/module readout systems for the ATLAS strip tracker upgrade. The chip which is mostly based on the ABCD3TA design is being used to help solve future ATLAS upgrade problems such as power delivery and data transmission. The chip was fabricated with the 250 nm CMOS technology by IBM. The final readout chip ABC130 that will be used in the ATLAS strip tracker upgrade will use the 130 nm technology. The reason for using the 250 nm technology is due to the fact that (a) at that time, 130 nm technology was not yet available (b) with the 250 nm, functional blocks from the ABCD3TA chip can be reused, like the front end, memory blocks etc.

The ABCN250 block diagram in Figure 10.2 clearly shows the similarity between this chip and the ABCD3TA design. The main difference is the addition of the power management block,

[3] 7 bits are enough to address the 128 strips

which comprises of two alternative shunt regulators and a serial regulator.

The other changes for the ABCN250 are:

- 2.5 V power supply.
- On-chip power regulation systems.
- Increased data bandwidth of 160 Mbps.
- Positive or negative input charge.
- Bonding pads arrangement and chip size.
- Pipeline length of 6.7 μs.
- Derandomizer length up to 42 events (128 bits long × 3 BC per event).
- Memory self test.
- Single Event Upset (SEU) flags (flagged when an SEU is detected at a cache register).

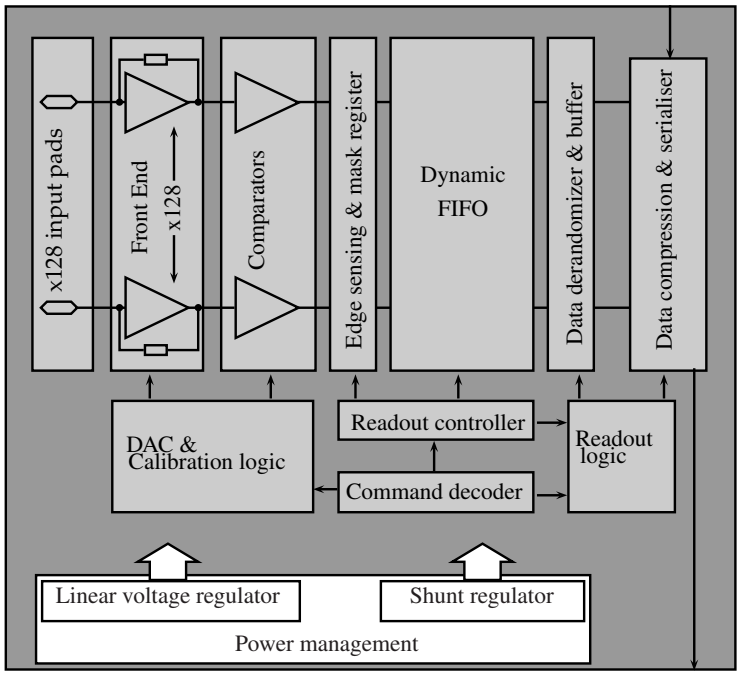



Figure 10.2: A block diagram of the ABCN250 chip.

In addition to the minor chip layout change, the chip readout schema has also changed with the introduction of an external readout controller, the Module Controller (MC). The MC's responsibility is to group and collect data from the chain of chips.

## 10.2 Motivation for ABC130

The ABC130 is designed to allow multi-trigger data flow control (refer to Section 4.2) and to cope with the new upgraded electronics system. The implementation of new data transfer protocols and new powering schemes in addition to the increased number of readout channels requires a significant redesign of the readout ASIC. The ABC130 will contain all the required functions to process 256 strips of a silicon detector employing binary readout architecture.
The main changes to the ABC130 from its predecessors are:

- 256 input channels.
- 130 nm CMOS technology.
- 1.3 V external power supply.
- Three trigger types, L0, R3 and L1 control the data flow[4].
- Fixed length data structure with multiple data types.
- Xon/Xoff flow control between chips allowing the chips in the chain to signal each other indicating when they are ready to transfer data.
- Readout mode compatible with an external Control Chip.
- Bonding pads arrangement, chip size fitting to the hybrid prototype.

[4] L0 is a trigger signal broadcast to all chips at a fixed latency after the event.
R3 is a region of Interest Readout Request: a signal sent to a fraction of the detector. It requests the readout of events tagged by the R3L0ID.
R3L0ID is an 8 bit address used to identify the events requested by the R3 signal.
L1 is a trigger signal for the entire detector, it requests events tagged with the L1L0ID.
L1L0ID is an 8 bit address used to identify the events requested by the L1 signal.

- SEU errors handling.
- I/O and register scan through JTAG.
- Fast cluster finder logic.

## 10.3 Digital design

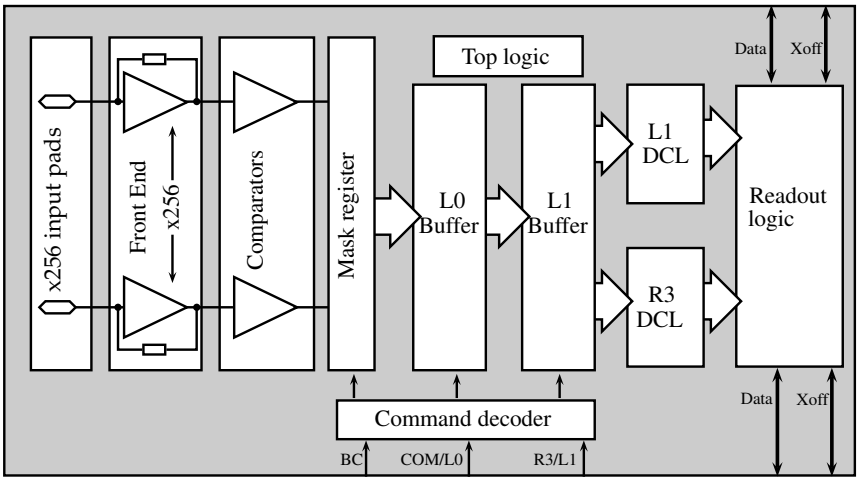



Figure 10.3: A block diagram of the ABC130 chip.

With every BC 256 channels are read through the analogue front-end of the channel and are sampled into the L0 buffer; a pipeline with a latency of 6.7 μs. At the reception of an L0 trigger an event (3 consecutive time slots) is moved into the L1 buffer. The data at this point waits for an L1 or an R3 coming from the Hybrid Controller Chip (HCC). At the reception of an R3 signal, which requests a specific event addressed by an L0ID, the event moves into the R3 Data Compression Logic (DCL) for processing. Similarly, when an L1 signal arrives an event is called with an L0ID and moved into the L1 DCL. Both L1 and R3 work with the sequence of an event, looking at the transitions of channels between BCs, represented as X1X, 01X, XXX where X is

the don't care state, 1 is a hit and 0 is a no hit. The R3 DCL reports a maximum of 4 hit clusters[5] per event while the L1 DCL reports all clusters in an event. Every DCL reports the clusters in a packet with the channel number (the address of the cluster) and some cluster information (e.g. hit pattern). The packets are stored in FIFOs internally within the DCLs waiting for the Readout Logic block to read and process them when ready.

The ABC130 design also includes registers that allow the control of the following configurations:

- Analogue front-end.
- Channel calibration.
- Channels mask.
- Prioritization of packets.
- Control of the bidirectional data lines.
- The detector slow-control data.

### 10.3.1 Packet structuring

The readout logic block that is responsible for packet building can create four kinds of packets. All of the four packets share the same header but with different payloads, as shown in Tables 10.2 and 10.3. The R3 packet can contain upto four addresses of four different hit clusters, from the middle BC of the L0 trigger event. The 1BC-L1 packet can contain addresses of up to three clusters including a three bit value indicating a hit or a no hit. If a cluster is greater than 4 channels wide, it is reported as multiple clusters and if more than 3 clusters exist in the event, more packets are produced. The 3BC-L1 packet reports the address of the first hit plus three BC hit patterns of four consecutive channels. This packet, which is selectable by a configuration register, is intended for timing studies. The last packet reports the contents of 32-bit configuration registers.

[5] A cluster is a hit which extends across multiple channels

The priority of the packets are in this order:

1. Adjacent chip
2. R3
3. L1
4. Internal registers

The packets from adjacent chips are already formatted and are simply channelled through the serialiser.

The readout logic block also uses the Xoff mechanism on chip links that can prevent adjacent chips from transmitting packets when the current chip is not ready to receive any. In addition, to facilitate the serializing feature of the chip, the Readout logic block contains two sets of bi-directional links for communicating with neighbouring chips allowing the transmission of data to either one of its two adjacent chips. The data can be configured to flow in one direction or the chain of chips can be split in to two loops which would allow bypassing malfunctioning chips without interrupting the entire chain.

| Start bit | Chip ID | TYP | L0ID | BCID | Payload |
|---|---|---|---|---|---|
| 1 | 5 | 4 | 8 | 8 | 34 |

Table 10.2: The ABC130 readout packet with 26 bits header and a 34 bits payload.

## 10.4 Data compression logic

### 10.4.1 Introduction

The Data Compression Logic (DCL) deals with the raw strip data, performs a wide range of algorithms and produces a compressed packet that describes the hits on the strips. For the ABC130 design, there are two DCLs related to two different trigger signals, L1 and R3. In this section,

| Type | | | | | | | |
|---|---|---|---|---|---|---|---|
| R3 | Ad | Ad | Ad | Ad | Of | SB | |
| | 8 | 8 | 8 | 8 | 1 | 1 | |
| 1BC-L1 | Ad | Hit | Ad | Hit | Ad | Hit | SB |
| | 8 | 3 | 8 | 3 | 8 | 3 | 1 |
| 3BC-L1 | Ad | Hit | Hit | Hit | Hit | Ud | EB |
| | 8 | 3 | 3 | 3 | 3 | 13 | 1 |
| Register | Data | Ud | EB | | | | |
| | 32 | 1 | 1 | | | | |

Table 10.3: The ABC130 packet payload types. (Ad=Address, Of=Overflow, SB=Stop Bit, EB=End Bit and Ud=Undefined).

both DCLs will be explained with particular emphasis on the design of the R3 DCL which was my personal contribution to the ABC130 digital design.

### 10.4.2 Level-1 (L1) logic

L1 examines the data of an event in parallel. It treats the 256 channels as two groups of 128 bits (odd and even channels). The DCL takes three channels (same row, different BC) and compares them against selectable criteria. The same criteria which were implemented in the ABCD3TA design (Table 10.1).

If the three bits match the criteria, the DCL can do one of the following:

1. Process the middle BC: the 8 bit address is created and the 3 bit cluster pattern of the hit is retrieved. The retrieved 3 bit cluster is then compared against the same selectable criteria and if there is a match, the 8 bit address along with three bits of '1' (or '0' in case of a mismatch) are added to the packet. The DCL repeats this procedure until all hits are detected and reported. Every 3 hits make one 1BC-L1 packet. More packets are produced if needed.

2. Process all three BC: the 8-bit address is created. Three BC data of four consecutive channels are added to make the 3BC-L1 packet. Sufficient packets are sent until the two groups of 128 channels are all examined.

### 10.4.3 Regional readout request (R3) logic and design

#### Requirements

The R3 DCL is required to process each of the 256-bit for 3 BC ($3 \times 256$bits) and report the location of hits with cluster widths of less than four channels, with a maximum report of four hits per event. The DCL must also report the position of the first channel in a cluster for one or two channel wide clusters and the position of the second channel for a cluster extending over three channels.

Additionally, the DCL must have the option of only processing events with a 0 to 1 transition (i.e. a new hit appearing only on the second BC). The packet produced by the R3 DCL must have the format shown in Figure 10.4.

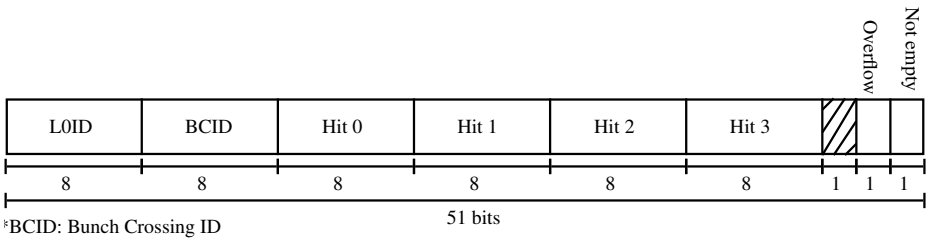



Figure 10.4: The R3 DCL packet structure.

### R3 DCL Block Diagram

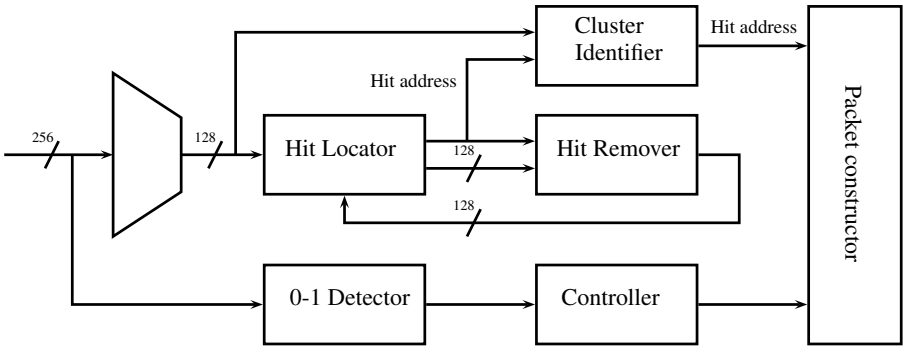



Figure 10.5: The R3 DCL block diagram.

In order to minimize the resources used by the DCL, mainly reducing the number of flip-flops (memory units), lookup tables (logic gates) and the number of clock cycles it takes to report a hit, the DCL is designed to handle the event data in two passes. Handling first the odd channels (1,3,5 ... 255) followed by the even channels (0,2,4 ... 254). Once the event data has been routed through the multiplexer and the 0-1 Detector (if enabled) is triggered, the 128-bits of the even channels are passed to the Hit Locator to seek the position of the first hit. This position is sent to the Cluster Identifier which examines the width of the cluster and forwards the address of the hit to the packet constructor, after it has made the decision whether to discard, leave or amend the address. The Hit Locator also strips the tail off all the hits (i.e. reduce the cluster size to 1) and forwards the headers of the hits with the position of the first hit to the Hit Remover. This simplifies the removal of the reported hit. Whenever a hit is removed the 128-bits are sent back to the Hit Locator to report the position of the second hit in line. This goes on until no hits are left. Once all the hits are detected from the even segment, the controller commands the multiplexer to route in the odd segment and repeats the same procedure. Finally, the packet constructor collects all the hit positions and creates the packet. The functionality is illustrated in the flowchart and the top block diagram in Figures 10.6 and 10.5, respectively.

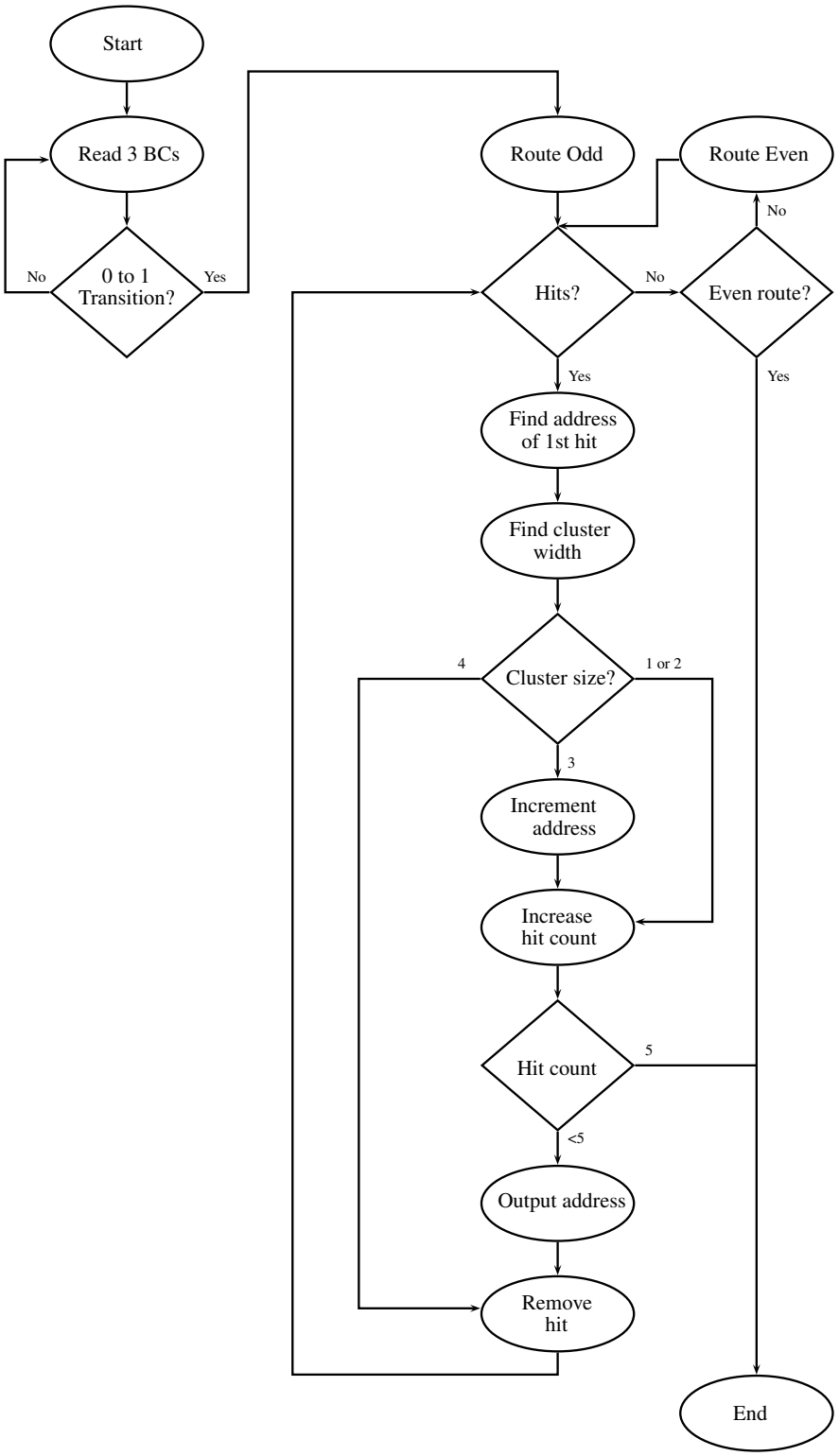



Figure 10.6: The R3 DCL flowchart.

### Hit Locator

The Hit Locator is both a hit identifier and a priority encoder. The hit identifier processes the event data and compresses the hit clusters into single bits, representing the header of the cluster. As illustrated in Figure 10.7.

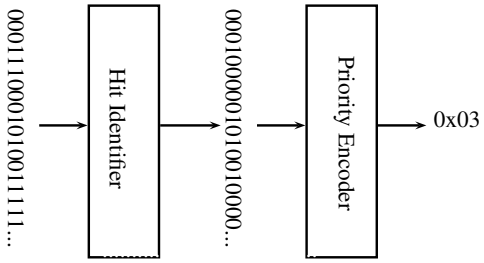



Figure 10.7: A block diagram of the Hit Locator data-flow. The data goes from left to right, the Hit Identifier reduces all clusters to a width of 1 which the priority encoder can process. The Priority encoder then reports the location of the first hit.

This is then passed to a priority encoder that reports the position of the first '1'. The Hit Locator has two inputs with 2 WR (Write) signals and is used in conjunction with the Hit Remover to process all the hits.

### Hit Remover

The Hit Remover operates with a simple process where it takes the position of a hit and outputs the same 128-bits input without the hit in the position provided. This is done using a priority decoder that outputs 128-bits with only the bit that corresponds to the position from the Hit Locator set to '1'. This is then XORed with the input from the Hit Locator to remove the hit. This is illustrated in Figure 10.8

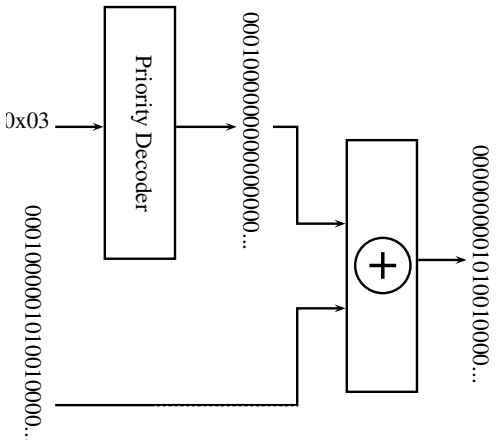



Figure 10.8: A block diagram of the Hit Remover data-flow. The data goes from left to right, an address is passed to the priority encoder which produces 128 bits with a '1' set at the input address. The bits are then XORed with data containing hit locations, this results in bits identical to the hit location data minus the hit at the input address (Hit at position 3 in this case).

### Cluster Identifier

The Cluster Identifier takes the hit position from the Hit Locator and using a multiplexer retrieves the cluster 4-bit bitmap from the original 128-bits. The bitmap is then examined with simple logic to determined whether it should be discarded or not, and whether the address should be amended, as shown in Figure 10.9. The address is amended when the cluster is 3-hits wide and the DCL has to report the address of the second hit not the first.

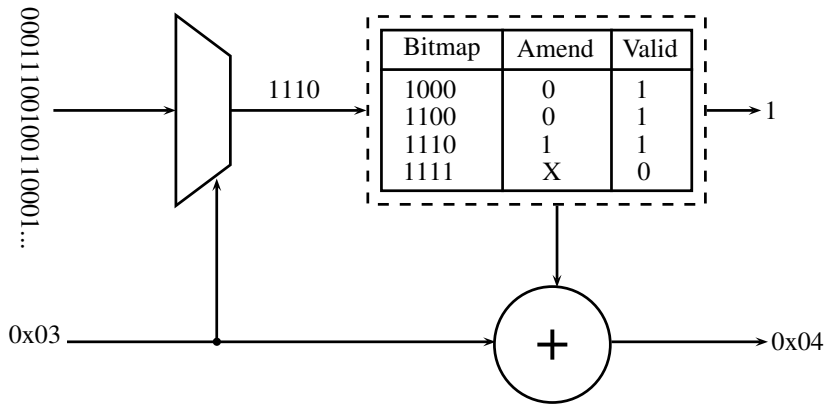



Figure 10.9: A block diagram of the Hit Remover data-flow. The data goes from left to right, the hit data is demultiplexed by retrieving the cluster at a specific address and comparing it with a lookup table.

### 0-1 Detector

The 0-1 Detector takes in 3 BCs, registers the last two events and discards the first. If there is a single 0 to 1 transition between the two data sets then the controller will be triggered to start the processing of the event. The detector is made of two memory blocks that are examined using a simple logic algorithm:

$$\overline{A} + B = C,$$

where A and B are the binary states of the memory blocks and C is the decision (output). The block also has an enable feature which can be externally controlled.

### Controller

The Controller takes care of the blocks' behaviour and their intercommunication. It is essentially a state machine which has the following functions:

- Controls the WR (write) signals to the Hit Locator.
- Notifies the Packet Constructor whenever a cluster is ready.

- Indicates when the packet is ready. Used as a FIFO write signal.
- Resets the system's buffers.
- Controls the routing of the main multiplexer. (Odd, even).
- Controls the overflow flag by counting the number of hits detected.
- Controls the not empty flag.
- Indicates the system's inhibit state and ignores any new events coming in when the inhibit flag is high.
- Monitors the FIFO status at the output.

These functions are achieved with the state machine diagram shown in Figure 10.10.

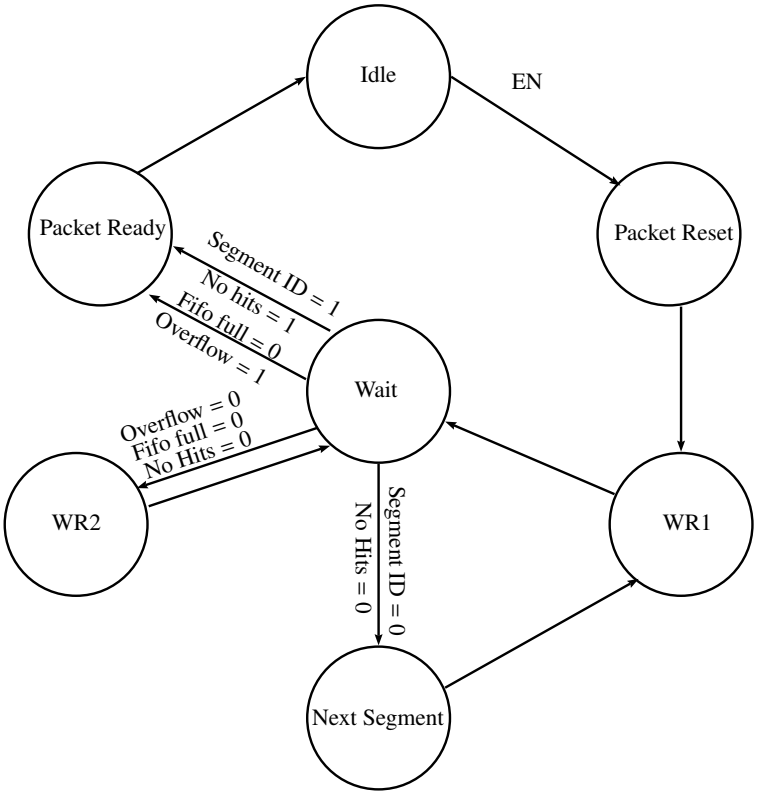



Figure 10.10: The R3 Controllers state machine.

### Simulation

Before the implementation of the R3 block into the ABC130 final design, the block had to be tested thoroughly on its own. The R3 DCL top block view and pin description are shown in Figure 10.11 and Table 10.4, respectively. The first tests were performed using a Verilog test-bench. Other blocks were created to provide the necessary inputs to the R3 DCL block and also to monitor its output. The test waveform results can be seen in Figure 10.12. The results show the successful creation of a valid packet and the successful operation of the 0-1 Detector block which ignores data when no change in hits has been detected.

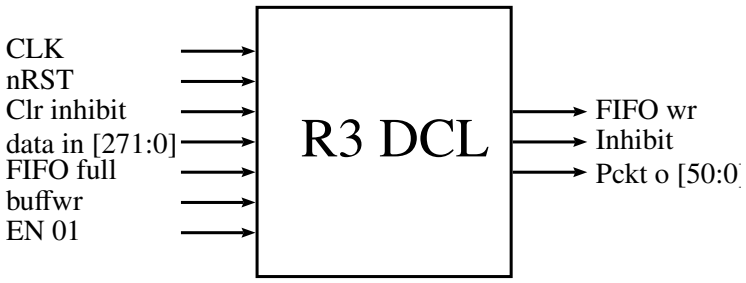



Figure 10.11: The R3 DCL inputs and outputs.

| Name | I/O | Width | Description |
|---|---|---|---|
| CLK | Input | 1 | Main Clock (40 MHz) |
| nRST | Input | 1 | Reset (Active low) |
| Clr inhibit | Input | 1 | Clear Inhibit |
| data in | Input | 272 | Event data (BCID 8 bits, L0ID 8 bits and actual Event data 256 bits) |
| FIFO full | Input | 1 | FIFO full status |
| buffwr | Input | 1 | Buffer write signal |
| EN 01 | Input | 1 | Enable 01 Detector |
| FIFO wr | Output | 1 | FIFO write signal |
| Inhibit | Output | 1 | DCL inhibit status |
| Pckt o | Output | 51 | Packet |

Table 10.4: The R3 DCL I/O description.

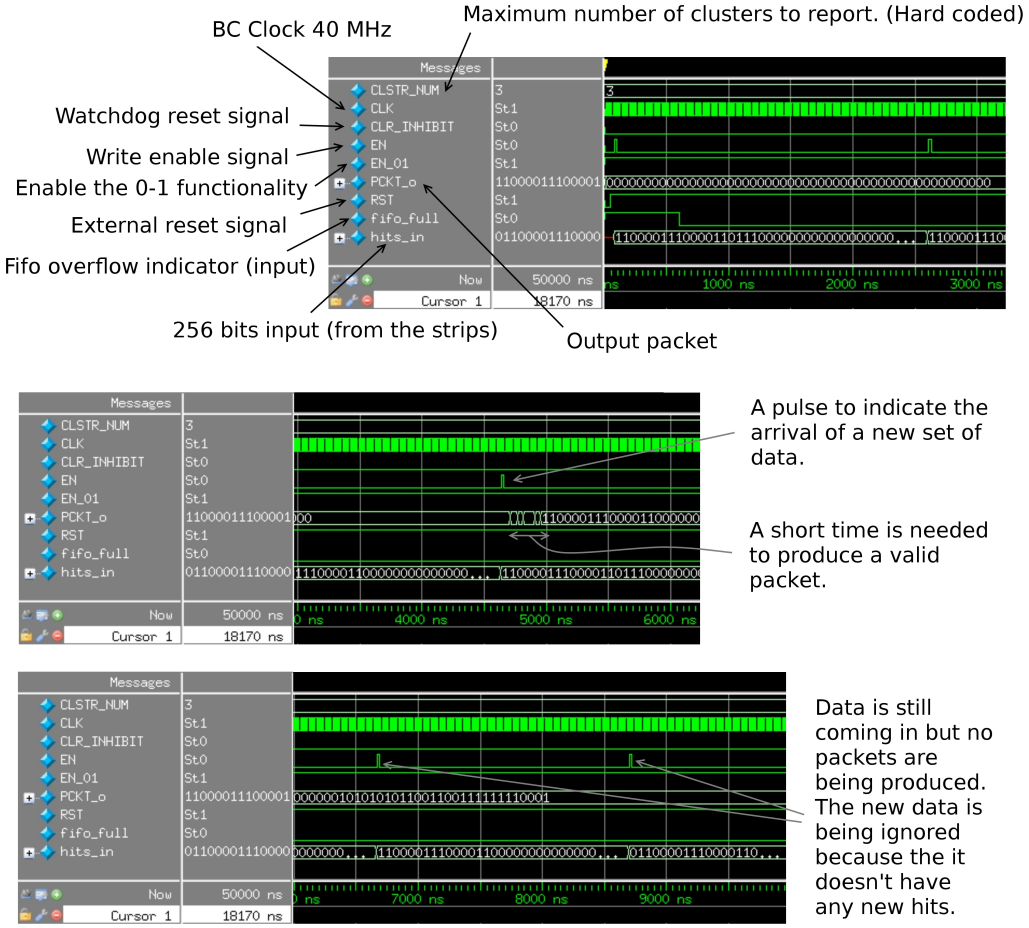



Figure 10.12: The results of the digital waveform simulation. The simulation shows the different input and output signals of the R3 DCL and how they are processed to produce a packet.

Probing the DCL even further requires a more dynamic event generator and possibly a better representation of the simulation results. This could be achieved by creating a Verilog event generator, however, a better approach would be testing the design on an FPGA development board. This, firstly, tests whether the code is fully synthesizable and also produce a more realistic model of the proposed system. The event data is generated with a pseudo-random-code generator

on a PC connected to the board via a USB link. A C program is responsible for generating and analysing the packets from the development board. The FPGA used was the Xilinx Spartan 6 LX45. The hardware simulation set-up can be seen in Figure 10.13.

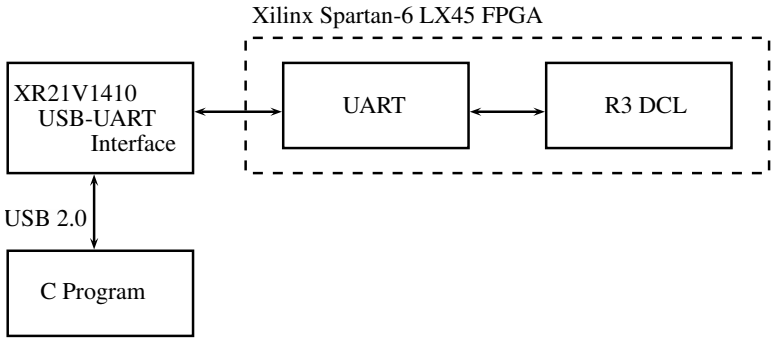



Figure 10.13: The hardware simulation block diagram.

The C program runs continuously, generating random events and sending them via the USB link. This can be seen in Figure 10.14. The program analyses the data being sent and prints out the positions of the clusters. The hit locations and the packet data are printed along with the event data.

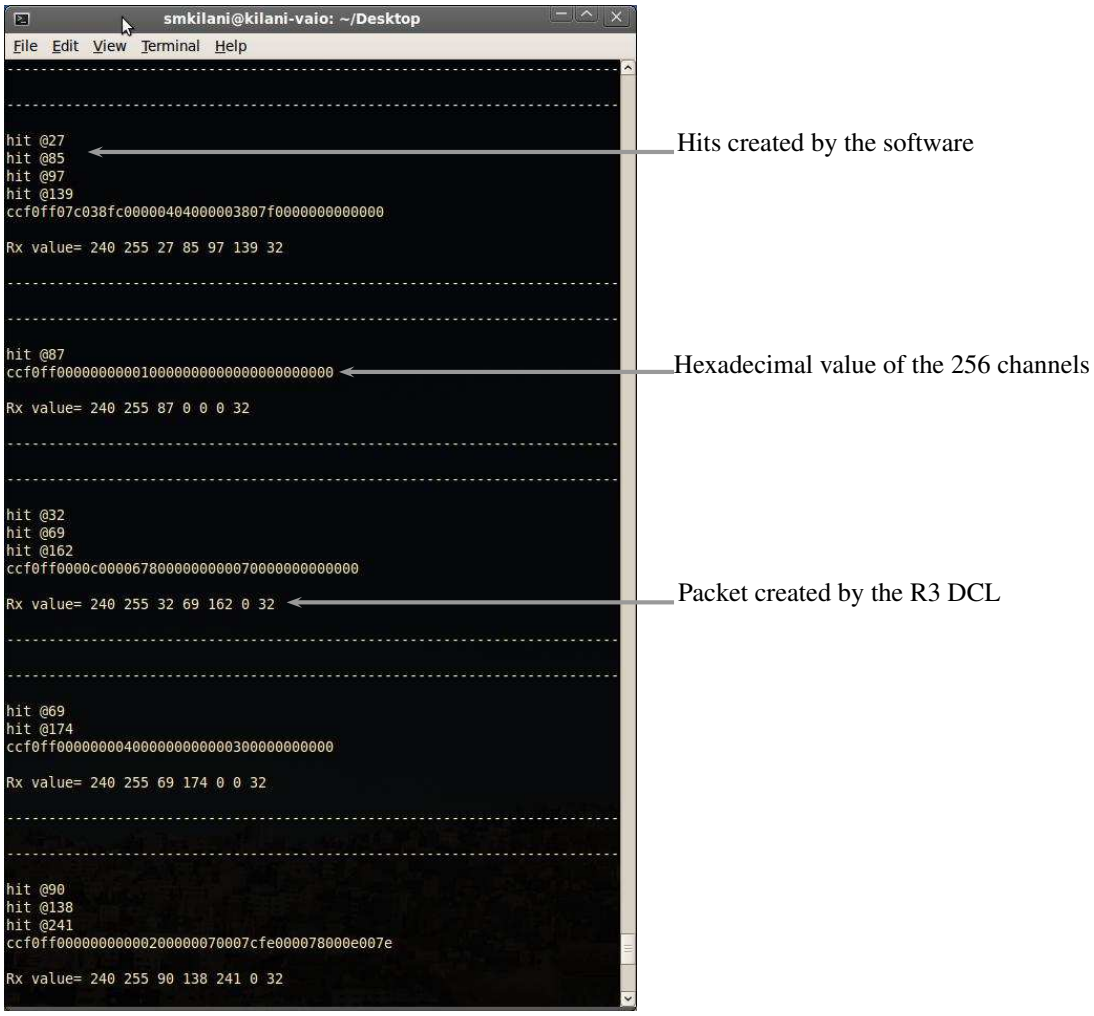



Figure 10.14: A screenshot of the simulation program. The program generates random hits, sends them to an FPGA board which would then return a packet with the results.

The hits created by the software are the positions expected to be reported back by the FPGA. The hits are embedded into a hexadecimal string along with a fixed L0ID and BCID. The return response from the FPGA includes the L0ID, BCID, the locations of a maximum of 4 hits (if less than four the other locations would be 0). The remaining bits are used for the flags. The FPGA return response has the same packet structure as seen in Figure 10.4.

## 10.5 Final tests of the ABC130

The final tests of the ABC130 digital design required a more complex test-bench to ensure that:

1. The logic blocks, which were designed by different people, communicate with each other properly.
2. More than one ABC130 chip can be included in the test-bench, to test the external communication features.
3. A powerful signal generator that can simulate large event data sets.

These testing requirements have been achieved with a test-bench scripted in MATLAB[67]. The chip design has passed the rigorous digital and analogue testing, a number of chips have recently been fabricated and they are currently under test.

# 11 Conclusion

In this thesis three areas critical to the successful implementation of the upgraded ATLAS detector have been researched. They are:

1. **Laser charge injection into strip sensors**:

   The injection of large charges into the detector was proven to be an insightful experiment. A deep understanding of the electrical characteristics of the strip sensors was achieved which helped create a comprehensive electrical model that simulates the behaviour of the sensor.

   The analysis has also found that damage can occur when large amounts of charge are injected into the sensor. The damage was limited to a few strips and it is believed that it is the result of the PTP (Punch Through Protection) failing to drain the extra charge. In this case, the electric field can no longer be sustained and it breaks down. Furthermore, tests on the absorption efficiency of the sensor have shown that a single strip absorbs about 40% of the charge injected by a laser. The other 60% is lost to reflection and charge sharing between neighbouring strips.

   Further work is still needed to properly evaluate the performance of the PTP structure, particularly in monitoring the current going through the PTP as a function of voltage across the coupling capacitor (i.e. where the electric field breaks down).

2. **Tests of the inner detector powering schemes**:

   The noise tests performed on the DC-DC and SP stavelets have shown no clear or decisive difference in results, thus, in terms of module noise performance, both schemes are good candidates. However, the EM emissions from the DC-DC converters have been shown to inject noise through the readout input channels when the coil of the converter is not shielded. This has led to the study of the EM susceptibility of the stavelet. The tests have identified the source of noise. The results have shown that the stavelet is completely immune to the magnetic fields but the noise pickup from the E-field was very high. The E-field is generally easier to attenuate. A very thin shield (with an overall thickness ~10 μm) would be sufficient to fully attenuate E-field emissions from the converter's coil. Furthermore, promising results have been obtained using a planar coil for the converter instead of the current toroidal coil. The planar coil also has less material and has been seen to have good performance and low EM emissions, but further R&D is still needed.

3. **Digital design of the ABC130 (strip readout chip)**:

   The digital design of the R3 DCL has been successfully incorporated into an ASIC. It has been successfully simulated as part of the overall digital design. The chips have been recently fabricated and they are currently under test.

The work on the laser charge injection tests has been shown to be broader than originally anticipated. Although the results obtained were beneficial to the analysis presented in this thesis, they can be further improved with more precise measurements. This can be achieved by designing advanced apparatus that can measure small and fast signals more precisely.

On the powering schemes, even though the tests performed and described in this thesis have shown no major problems with the serial powering scheme, other groups have encountered

problems that were not present with the DC-DC powering scheme. In general, it is widely believed that the DC-DC powering will be chosen for the upgraded detector and thus the work will be mostly focused on it. A larger focus will be on the planar coil converters. Once the exact dimensions of the DC-DC converter are set, the planar coil can be redesigned to fit the exact specification and the converters will be tested again.

# A Useful information

## A.1 Reflection loss derivation

The intensity of an incident wave transmitted from a medium of impedance $Z_1$ to another with impedance $Z_2$ can be expressed as

$$E_1 = \frac{2Z_2}{Z_1 + Z_2} E_0. \tag{A.1}$$

and

$$H_1 = \frac{2Z_1}{Z_1 + Z_2} H_0, \tag{A.2}$$

where $H_0$ and $E_0$ are the magnetic and electric field intensities of the incident wave and $H_1$ and $E_1$ are the intensities of the transmitted wave. In the presence of a shield barrier, the wave encounters two boundaries. $Z_1$ to $Z_2$ then $Z_2$ to $Z_1$. Therefore the transmitted wave can be given by

$$E_t = \frac{2Z_1}{Z_1 + Z_2} E_1. \tag{A.3}$$

and

$$H_t = \frac{2Z_2}{Z_1 + Z_2} H_1. \tag{A.4}$$

For thick shields (i.e. thicker than the skin depth) and by substituting A.1 and A.2 into A.3 and A.4

$$E_t = \frac{4Z_1Z_2}{(Z_1 - Z_2)^2}E_0. \tag{A.5}$$

and

$$H_t = \frac{4Z_1Z_2}{(Z_1 + Z_2)^2}H_0. \tag{A.6}$$

In the case of the barrier surrounded by an insulator, then the reflection loss for both the electric field and magnetic field would be the same. The electric field will reflect when entering the barrier and the magnetic field will reflect when exiting the barrier. Thus when $Z_1 \gg Z_2$ equations A.5 and A.6 reduce to

$$E_t = \frac{4Z_2}{Z_1}E_0. \tag{A.7}$$

and

$$H_t = \frac{4Z_2}{Z_1}H_0. \tag{A.8}$$

By substituting the wave impedance $Z_w$ with $Z_1$ and the shield impedance $Z_s$ with $Z_2$ the reflection loss for either E or H is

$$R = 20\log\frac{|Z_w|}{4|Z_s|}\ dB. \tag{A.9}$$

## A.2 Capacitance measurements

The most widely used capacitance measurement method uses AC signals to extract the capacitance. The capacitance is measured from the impedance and frequency of the applied AC signal. The following equations are used:

$$V = e^{j\omega t},$$

$$I = j\omega C e^{j\omega t},$$

$$Z = \frac{V}{I},$$

$$\therefore C = -\frac{1}{\omega Im(Z)}.$$

### A.2.1 How to extract capacitance

The capacitance can be extracted with two models: Parallel and series, as shown in Figure A.1.

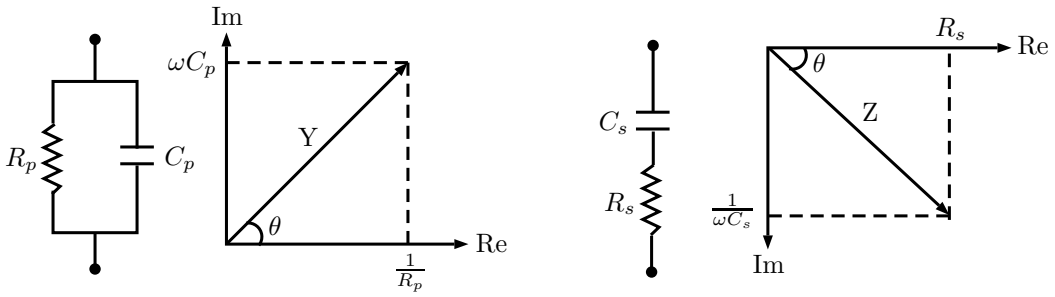



Figure A.1: The parallel (left) and series (series) capacitance extraction models.

### Parallel model

When the parallel model is used, the following equations are utilised:

$$Y = \frac{1}{Z} = \frac{I}{V} = \frac{1}{R_p} + j\omega C_p.$$

$$C_p = \frac{Im(Y)}{\omega}.$$

$$R_p = \frac{1}{Re(Y)}.$$

### Series model

When the series model is used, the following equations are utilised:

$$Z = \frac{V}{I} = R_s + \frac{1}{j\omega C_s}.$$

$$C_s = -\frac{1}{\omega Im(Z)}.$$

$$R_s = Re(Z).$$

### How to choose?

A device under test (DUT) is seen by the capacitance meter as in Figure A.2

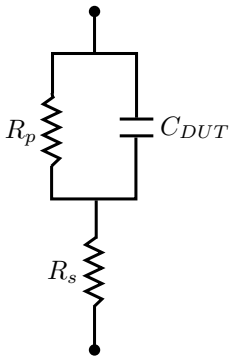



Figure A.2: The schematic of a DUT. The values for $R_p$ and $R_s$ determine the capacitance extraction model to be used.

To determine the capacitance extraction model, the values of $R_s$ and $R_p$ have to be examined. If $R_s \ll R_p$ and $R_s \ll \frac{1}{\omega C_p}$ then parallel model is used. Otherwise, the series model is used.

## A.3 ATLAS12

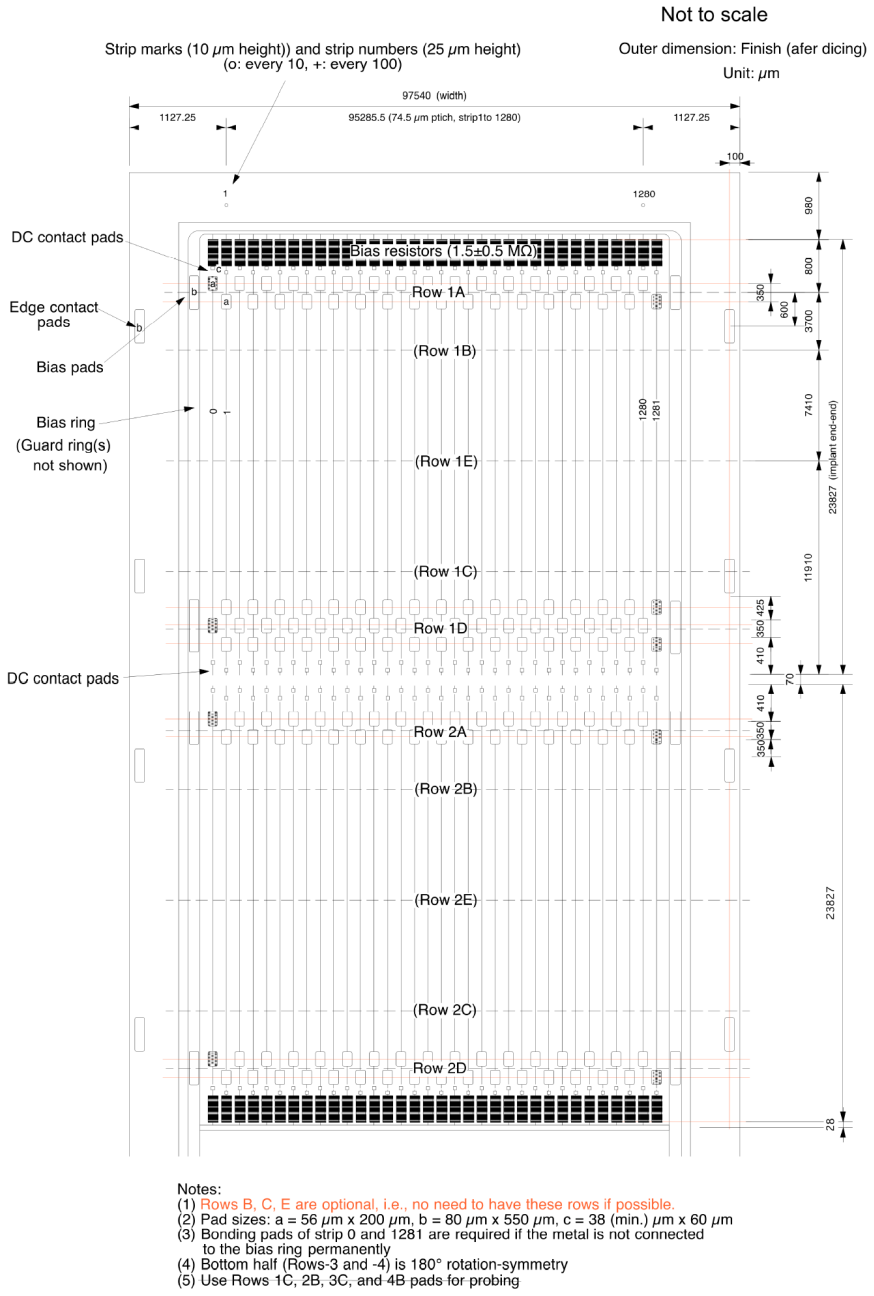



Figure A.3: The strip and bond pads layout in ATLAS12 [38]

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# List of Figures

# List of Tables