Functional Testing of the ATLAS SCT Barrels

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Abstract

The ATLAS SCT (semiconductor tracker) comprises 2112 barrel modules mounted on four concentric barrels of length 1.6m and up to 1m diameter, and 1976 endcap modules supported by a series of 9 wheels at each end of the barrel region, giving a total silicon area of 60 square metres.

The assembly of modules onto each of the four barrel structures has recently been completed. In addition to functional tests made during the assembly process, each completed barrel was operated in its entirety. In the case of the largest barrel, with an active silicon area of approximately 10 square metres, this corresponds to more than one million instrumented channels.

This paper documents the electrical performance of the four individual SCT barrels. An overview of the readout chain is also given.

1. Introduction

ATLAS[1] will be the largest detector to operate at CERN's Large Hadron Collider (LHC). The ATLAS SemiConductor Tracker (SCT) is part of the ATLAS Inner Detector. The SCT Barrel comprises four concentric barrels of length 1.6m which support a total of 2112 barrel modules. The two SCT Endcaps each comprise a series of 9 disks supporting a total of 988 endcap modules. This paper documents the "as built" performance of the four SCT barrels and the techniques used to test the modules.

1.1. *The Barrel Module*

The ATLAS SCT Barrel Module[2] comprises a VHCPG (Very High Thermal Conductivity Pyrolitic Graphite) baseboard glued between two planes of single sided silicon microstrip detectors. Each plane comprises a pair of AC coupled p-in-n silicon sensors with 80 micron strip pitch, produced by Hamamatsu Photonics [3]. Small angle stereo geometry is used to provide positional information in two dimensions, an angle of 40 mrad being engineered between the two sides.

Each module is read out by 12 ABCD3TA ASICs [4] mounted on a copper/kapton hybrid [5]. Manufactured in the radiation hard BiCMOS DMILL process, each chip provides sparsified binary readout of 128 channels. The amplified and shaped input signal is compared to a programmable threshold having two components: a single 8-bit DAC applied across the whole chip, and a channel specific 4-bit (trim) DAC designed to compensate for channel-to-channel variations. The resulting hit pattern is transferred into a binary pipeline, 132 cells deep. Upon receipt of a Level 1 Accept (L1A) trigger, the pipeline output is transferred into a derandomising buffer that

can store up to 8 events. In addition the ASIC has a four bit L1A counter and an eight bit Bunch Crossing (BC) counter: the output data includes a record of these counters such that data from all parts of the SCT may be assembled into one event record. The design also includes charge injection circuitry to facilitiate calibration of the front end.

1.2. *Barrel Services*

Electrical and optical services are brought to the modules by means of "harnesses". Each harness comprises 6 doglegs, 6 pairs of Low Mass power Tapes (LMTs), 12 data fibres and 6 control fibres.

The clock and command signals are transmitted to the module in the form of a biphase mark encoded optical signal [6]. This is received by a PIN[7] diode and converted into separate LVDS [1] clock and command signals by the DORIC[8] chip. In turn the module generates two LVDS data streams, each one being used by the VDC[8] chip to modulate the output of a VCSEL[9] diode such that data are sent off-detector in optical form. Hence each module is associated with three optical fibres which terminate in an opto package mounted on the dogleg. This package houses the DORIC and VDC chips in addition to the PIN and VCSEL diodes.

An evaporative cooling system is used to remove the heat generated by operation of the SCT. One barrel cooling unit services 48 modules (four rows). The two inner rows of each cooling unit end in a common outlet manifold, the two outer rows being inlets, connected directly to capillliaries. At the end of each outlet row, just before the manifold, a pair of thermistors is attached to the pipe. In additon to the provision of temperature monitoring, these also serve as inputs to the power supply interlock system such that, if the cooling system may fail, the power is cut off to prevent overheating of the detector modules[10].

[1] Low Voltage Differential Swing

1.3. *Macro-assembly*

Barrel modules were shipped to the macro-assembly site from each of the four production clusters and were tested upon receipt to verify that they had not been damaged in transit. Based upon these electrical results, and results from the production cluster, modules were carefully graded and selected to be mounted on each barrel.

A pair of custom robots [12] were used to locate the detector modules onto the barrels. This choice was made primarily due to the very restricted clearances between each module, its neighbours and their support structures, which dictated that each module could only be moved into position by following a tightly controlled path[11]. Before each module is mounted, a carefully controlled layer of thermal grease is spread onto the cooling block, part of the cooling unit, to ensure good thermal contact is made. Figure 1 shows the last module being mounted onto barrel 3, the innermost barrel and the first to be completed.

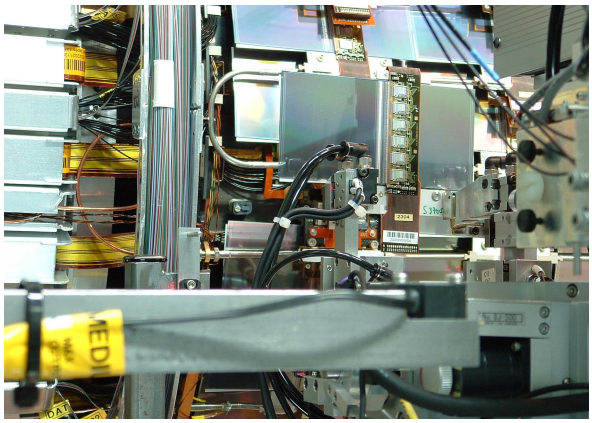

Fig. 1. Mounting the last module on Barrel 3.

At the peak of the macro-assembly programme, running two shifts, each robot could mount 36 modules per day. Only five modules were damaged during macro-assembly (0.2%). In the event that after electrical testing a module needed to be removed and replaced, this was also done by means of the robot.

1.4. *Data Acquisition System*

The module power supplies[13] and readout hardware used were a subset of those to be used in ATLAS. Macro-assembly provided the first opportunity to use these systems on a large scale.

The Data Aquisition System (DAQ) is centred around the ATLAS Silcion/Pixel Read Out Driver, (ROD) a 9U VME64X module common to both subdetectors. This comprises five Digital Signal Processors and memory in addition to several functional blocks implemented within Field Programmable Gate Array logic. Each ROD is connected to a Back Of Crate card (BOC) which provides the interface between the electrical and optical domains: different versions of the BOC exist for the SCT and Pixel subdetectors. Within each readout crate there is also a Timing Interface Module (TIM), which distributes clock and trigger information to the RODs by means of a custom crate backplane, and a Single Board Computer which communicates with TIM and the RODs by means of the VME bus.

Each ROD has four Slave DSPs and one Master DSP. The MDSP is used to broadcast L1A triggers to the modules, whilst the slaves are used primarily to decode and histogram events returned to the ROD by the SCT modules. At the highest level, tests are controlled by the SctRodDaq software.[14]

2. Functional Tests

At convenient breaks during the macro-assembly schedule, several rows of recently mounted modules were cabled up to be tested. One cooling unit would be started, servicing four adjacent rows, and a group of typically 24 modules within these rows would be powered to nominal operating conditions. The functional test sequence described below would now be performed for all powered modules. Throughout the testing, attention was paid to the temperature difference between the module (hybrid) and the cooling pipe to verify that they are in good thermal contact with one another.

With a few exceptions, [2] no attempt was made to re-optimise the configuration of the ABCD3TA chips: the trim and mask settings used during barrel testing were those previously determined during the module reception tests. The key analogue tests performed after macro-assembly were also part of the module reception test, so a direct comparison could be made to spot any deterioration in module performance. After any discrepancies had been investigated, the test process would be repeated until all modules had been tested.

2.1. *Basic Tests*

(a) **Configure and Probe** When first powered, SCT modules return the 40.08 MHz clock signal divided by two on each of their datalinks. A configuration command sequence is sent to the modules to put the ABCD3TA chips into data taking mode, followed by a L1A trigger (probe). The data returned by the modules are captured on the ROD and analysed. Modules which have been successfully configured should return an event. Any modules which still return the clock/2 signal did not receive the configuration commands, most likely due to mapping errors which, once identified, can be easily corrected.

(b) **Hard Reset and Probe** A "Hard Reset" signal is now sent to the modules by means of the LV power supply system followed by a L1A trigger (probe). If the reset signal is received correctly, the modules will revert into their default state and the clock/2 signal will once more be returned through the datalinks. Any modules which return events did not receive the hard reset signal.

(c) **RX Threshold Test** At this point in the sequence, communication with the modules has been established, however further optimisation may be required such that data reception remains reliable for longer events. The most important of these adjustments is the RX threshold of the data receiver chip on the BOC, the threshold used to discrimininate the

[2] In a handful of cases, individual channels were found to cause readout errors, and had to be masked off.

optical data signal as it is converted into electrical form. A known pattern is read back from the ABCD3TA chips several times for each of a range of RX thresholds. The resulting histogram is analysed to determine the range over which the pattern may be reliably discriminated, and the RX threshold is adjusted to a point well within the safe region.

(d) **NMask Test** As a final check of the optical communication scheme, a sequence of known patterns of varying length are written to the ABCD3T mask register. Each pattern is read back several times to fill one bin of a histogram and a simple analysis is performed to verify that the expected result is obtained. Hence this test demonstrates the correct operation of the mask register, and that data reception is reliable across the expected range of event sizes.

2.2. *Digital Tests*

(a) **Pipeline Test** This test uses a trigger sequence comprising a soft reset command, which resets the pipeline and counters, followed a controlled interval later by a L1A trigger. By varying the delay between the two commands the pipeline structure is scanned. There are two possibilities for failure of an individual pipeline cell within an ABCD3TA chip: it may be stuck ON, leading to excess occupancy, or OFF, leading to inefficiency. In either case the defect remains associated with a particular block within the pipeline structure. The modules used during barrel macro-assembly had been preselected to have no more than 2 defects of this type.

(b) **Full Bypass Test** The hybrid and chip designs incorporate features such that, in the event that a chip should fail during operation of ATLAS, it may be bypassed such that data from the remainder of the module may be read out. This test cycles through all such possibilties to ensure that these features are functional.

(c) **Chip Counter Test** The L1 and BC values reported by the two sides of a module are captured and compared across a range of values to verify that they are the same. As the clock and command signals are common to both sides, any differences between the counters would indicate that one of the counters is faulty. As the ability to associate events by means of the counters is of paramount importance in ATLAS, all modules found to have faulty counters were replaced [3].

2.3. *Analogue Tests*

(a) **Three Point Test** A series of threshold scans is performed for injected charges of 1.5, 2.0 and 2.5fC. In each case a complementary error function is fitted to the data: the mean corresponds to the threshold at which 50% efficiency is achieved for pulses of the designated magnitude and the sigma is a measure of the output noise (in mV). The gain of each channel is calculated from a linear fit to the fit results for the three scans. The output noise from the scan taken with 2.0fC injected charge is divided by the gain to determine the input noise (in fC or ENC). By comparing the input noise calculated for each channel with typical values, it is possible to identify several types of defective channels including those which are not connected to the far sensor (partbonded) and those which are not connected to either sensor (unbonded). Attention is also paid to the RMS spread of the gain and offset parameters within each chip: unusually large values would suggest that the module had not been trimmed properly, such as may happen if the wrong configuration had been loaded to a module due to a mapping error.

(b) **Noise Occupancy Test** A threshold scan without charge injection is performed to determine the noise occupancy of each module as a function of threshold. Analysis of the data permits an estimation of the (Gaussian) noise of each module by means of a linear fit to a graph of ln(occupancy) vs Q^2_{thr} (fC^2). Deviation from this line, notably at higher

[3] The Chip Counters were not part of the Module Reception Test

thresholds, may be indicative of non-Gaussian behaviour such as the presence of common mode noise. The occupancy due to noise at the nominal operating point of 1fC is taken as a reference point for purposes of comparison.

(c) **Double Trigger Noise Test** Two L1A triggers separated by a specified number of clock periods are sent to the modules. The first event of each pair is thrown away leaving the second to be histogrammed. The spacing of the two triggers is varied from 120 to 160 clock periods, to determine the occupancy of the modules at various points during the readout cycle. A trigger spacing of 132 is of particular interest as this is equal to the depth of the readout pipeline: the second event records the occupancy of the module as the readout cycle of the first event starts. The VCSELs used to transmit the events off-detector operate at 850nm, a wavelength for which silicon has good quantum efficiency. Although the optical system is in principle fully enclosed, any encapsulation failures could provide a direct path for readout signals to be injected back into the detector.

(d) **Synchronous Trigger Noise Test** The Synchronous Trigger Noise Occupancy Test aquires and analyses data in a similar similar manner to the Noise Occupancy Test, however L1A triggers at 100kHz frequency are now distributed synchronously across the entire system. Although the ROD firmware can format events at this rate and pass them up the DAQ chain, the histogramming code cannot presently keep up: only a fraction of the events may be histogrammed. A comparison between the standard and synchronous noise occupancy distributions will give an indication of any extra noise present only when running at high trigger rates.

(e) **Sensor Leakage Current** Last but not least, once DAQ tests have been completed, the detector bias is raised to the expected operational limit for the barrel under test to verify that the active area has not been damaged during assembly.

In addition to the tests made during macro-assembly, each completed barrel was operated in its entirety. Barrels 3, 4 and 6 were fully tested at Oxford (the macro-assembly site), with barrel 3, the first to completed, receiving an additional test at CERN to verify that it had not been damaged during transit. Scheduling constraints dictated that barrel 5 had to be shipped before a complete test could be made, hence it was only tested upon its arrival at CERN.

3. Results

During testing, a handful of the datalinks were found to have failed. A likely explanation may be susceptibility of VCSELs [4] and VDC chips to electrostatic discharge (ESD). As a damaged opto package could not be replaced [5] in such cases it was decided to use the module's built in redundancy features. With a standard barrel module, 11 out of 12 chips may be read through one datalink. For barrels 4, 5 and 6 a number of modules were modified by the addition of a simple kapton flex circuit on top of the hybrid such that all 12 chips could be read out through the remaining good link. At the time of assembly, this mode of operation was not supported by the DAQ system, so only 11 chips of each modified module could be tested.

Whilst testing Barrel 3, the Double Trigger Noise Test identified two instances of light leakage from opto packages. In both cases the increase in occupancy affects only a few channels and can be tolerated in ATLAS. The opto packages of all remaining barrels were visually inspected before modules were mounted, a small number being resealed. Only one more light leak was found, at an even lower level than the original two.

Out of the 2112 modules mounted on the four barrels, 14 were removed and replaced due to problems detected during testing: 3 modules had BC or L1A counter faults; 3 modules caused readout errors which could not be cured by masking off an acceptable number of channels [6] ; 3 modules were

[4] An ESD pulse may damage the "Distributed Bragg Reflector" within the VCSEL, leading to a marked reduction in its light output.

[5] short of replacing a complete harness

[6] A module was replaced if, as operated in ATLAS, data from one or more chips would not be usable

removed and replaced by "modified" modules at locations where only one datalink was operational; 2 modules had one dead chip; 1 module lost its bias connection after the full barrel (cold) test; 1 module had high noise; 1 module had excessive leakage current.

The input noise values for each barrel are summarised in Figure 2. For barrels 3, 4 and 6 tested "cold" at Oxford, the median input noise is around 1480 ENC. The median input noise for barrel 5, only tested "warm" at CERN, is slightly higher at 1600 ENC. Approximately 80 ENC may be accounted for by the temperature difference of around 13^{o}C: the remainder is not unexpected given a number of small differences between the two test environments.

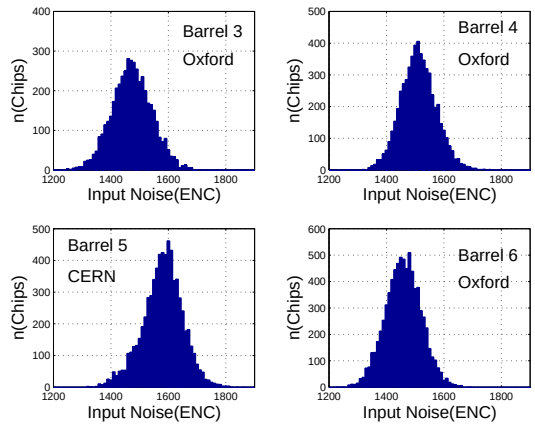

Fig. 2. Input Noise measured by Three Point Gain

A summary of channel defect statistics for the four barrels after faulty modules had been replaced is shown in Table 1. A significant contibution to the total number of defects are the 1536 "Not Tested" channels: these correspond to the chips on the modified modules which could not be read out at the time of the tests. Following revisions to the DAQ and ROD software, these channels are expected to be recovered. Hence it can be seen that more than 99.7% of the channels are fully functional.

4. Conclusions

ATLAS SCT Barrel Macroassembly has been successfully completed, with four barrels delivered to CERN according to schedule. A pair of robots were used to mount 2112 modules on the barrels, a process which incurred only minimal losses (5 modules including "suspects"). A total of 14 modules needed to be replaced. More than than 99.7% of the 3.2 million readout channels in the resulting SCT barrel are fully functional.

5. Acknowlegements

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Table 1
Channel Defect Statistics

Barrel	Total Channels	Not Bonded	Dead	Not Tested	Part Bonded	Noisy	Other	Total Defective or Untested
3	589824	180	357	384	91	460	11	1483
4	737280	55	245	256	16	242	27	841
5	884736	173	770	256	97	492	30	1818
6	1032192	385	2513	640	197	1936	49	5720
Total	3244032	793	3885	1536	401	3130	117	9862

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