SCT Timing working document

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ABSTRACT

This document is a preliminary and incomplete draft on the calibration and synchronization of the timing of the SCT. It is made available for comments by the SCT community.

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1. INTRODUCTION

Many front-end readout elements receive timing, trigger, synchronization and test-pulse signals. The phases of all these signals have to be adjusted in order to sample the input signals optimally, read out the proper event, and maintain a coherent bunch-crossing identifier (BCID) number and hence synchronization across the experiment.

There will be a large number of delay elements to be adjusted and monitored, which may require a lot of time and effort. Therefore, some automatic procedures should be defined to set up the timing for various modes of operation: beam collisions, cosmic rays and running with test pulses for test or calibration purposes.

The signals referred to above are:

- bunch-crossing (BC) clock for signal timing
- level-1 accept (L1A) for readout trigger
- bunch counter reset (BCR) for pipeline synchronization

The following front-end timings have to be adjusted:

- BC clock phase (to ensure optimal sampling of the input signal)
- L1A arrival time (to ensure readout of the correct bunch crossing)
- BCR arrival time (to ensure a coherent BCID across the detector)

These timing adjustments are required for the signals received by the front-end electronics at each detector readout module. The adjustment of BC clock phase is over a range of 1BC (25ns), with an accuracy of (better than) 1ns required. The adjustment of L1A and BCR arrival time is to identify the correct clock cycle, which requires a resolution of 25ns.

It is convenient to separate the calibration of the front-end timings into a global part and a local part. The global part is of the whole SCT relative to the time of the event's primary interaction. The adjustments are carried out using the TTC system and are described in ref. L1TDR. The local part of the calibration is the internal synchronization of the SCT such that all the detector readout modules are correctly aligned in time relative to each other. The timing adjustments for each readout channel are made in the SCT off-detector electronics using the scheme of Nickerson and Weidberg (ref. SYN94, SYN96, SYN98).

The rest of the present document is an attempt to cover the internal synchronization in more detail! The goal is to synchronize the timing across the SCT better than 1ns with respect to the LHC clock.

2. OVERVIEW OF INTERNAL SYNCHRONIZATION

Each front-end module must receive the clock at the appropriate time. The time relative to the LHC machine clock will depend on many factors, such as location with respect to the interaction point and propagation delay through the electronics.

The time of flight of particles from the interaction point to the detector elements varies from 1ns up to 3ns within the SCT barrel alone. For data taking, the clock timings must be corrected for particle

flight times. The goal for internal synchronization is that all clocks arrive at the front-end modules within 1ns of each other, excluding flight paths, leaving one overall adjustment.

A method to align the timing is to scan the time of each clock line when there are collisions in the machine and use some feature of the data to decide the correct clock phases. Whilst ideal for final tuning, this scheme has the disadvantage of requiring beam. The rate of suitable cosmic rays through the detector is insufficient to allow the correct timing of each clock to be established with any precision on a reasonable time scale (discussed in ref. SYN96).

The scheme of Nickerson and Weidberg (ref. SYN94) will be used to address the issue of how to cross-synchronize modules within the SCT without the need for collisions in the machine. Each module is able to operate either from its own clock, or from its neighbour's clock (also intended to provide redundancy in case of failure), and send it back along the out-going data links. In 'clock through mode' the received clock (divided by two) is returned along the data link, so that by comparing the phase of the returned clock and the returned neighbour clock, the relative time of arrival at the front-end of all adjacent pairs of clocks can be determined and adjusted to be correct.

The phase of the returning clock is measured with respect to a local clock at the data receiver. Ideally, we would like to measure directly at the front end the time difference between neighbouring clocks, but the detector will be inaccessible. Nonetheless, the objective is achieved because the off-detector measurement of a pair of clocks is delayed by the same data link.

By arranging neighbours in a chain, large groups of detector modules can be made internally self-consistent in terms of synchronization. In the case of the SCT barrel, the current plan calls for groups of 24 modules from two full staves to be connected in a ring. However, this crosses $z = 0$ and may break the ground insulation between the two halves of the detector. An alternative is for groups of 12 modules from two half staves to be connected in a ring.

For the SCT end-caps, it is natural to identify the chains of clock pairs with the rings of the detector. This gives rings of 40 and 52 modules for synchronization (and redundancy). These larger numbers increase the build-up of errors around the ring but sub-groups can be used. The synchronization scheme is not affected if a pair of neighbouring clocks comes from different Readout Drivers (RODs) and their associated Back-of-Crate (BOC) cards.

Cross synchronization of the groups of measured neighbours will be given by measurements of propagation delays made during assembly of the detector. Assuming that the fibre lengths can be controlled to 5cm and that the uncertainty in the propagation delays through the driver and receiver electronics is less than 4ns (which should be conservative), all the clocks will arrive at the front end within 5ns of the nominal time. If the errors are random, this yields 1ns precision for the mean propagation delay for each group of 24 neighbours in the barrel, which is sufficient.

The off-detector electronics should, ideally, measure the timing of the returned clock relative to a local clock with a resolution of about 100ps (ref. BOC99). The jitter may be larger than this, which would require averaging over many measurements, ideally done by the ROD.

3. PROCEDURE FOR INTERNAL SYNCHRONIZATION

The procedure for internal synchronization of the clock and control system is updated from that outlined in ref. SYN98. It is automated and under the control of the local computer in each SCT readout crate. It does not require the TTC system. This procedure is performed infrequently, at the

instigation of an expert operator who has determined a need to do so. The estimated time for the procedure is a minute or two.

The first stage is to align the timing within each group of modules using the pair-wise synchronization method.

1. Starting values of the delay for each channel are loaded into the BOCs (e.g. the reference data to be monitored). These values should exclude the effects of time of flight and delay between and within readout crates.
2. The front-end chips are switched into clock through mode (all at once).
3. The BOCs measure the phase of the clocks returned via the data links relative to the local copy of the system clock. The data is reported to the local computer. Jitter may require averaging over many measurements.
4. The local computer has to account for the measurements being modulo 25ns or 50ns (is the phase of the returned clock determined?). The simple solution is to adjust BOC delays such that the measurements are mid-range, and repeat the previous step.
5. The front-end chips are then instructed to use the neighbour clock (all at once).
6. Repeat the above BOC measurement step for the neighbour clock.
7. The local computer evaluates a timing correction for each out-going channel based on the measured relative phases of the returned clock and neighbour clock. A 'bad channel' database may be used. The corrected channel delays are loaded into the BOCs.
8. The procedure is repeated until it converges (the delay step size is not necessarily well controlled, so iteration may be required).

The second stage of the procedure is to align the timing between groups of modules. This consists of calculation by the local computer.

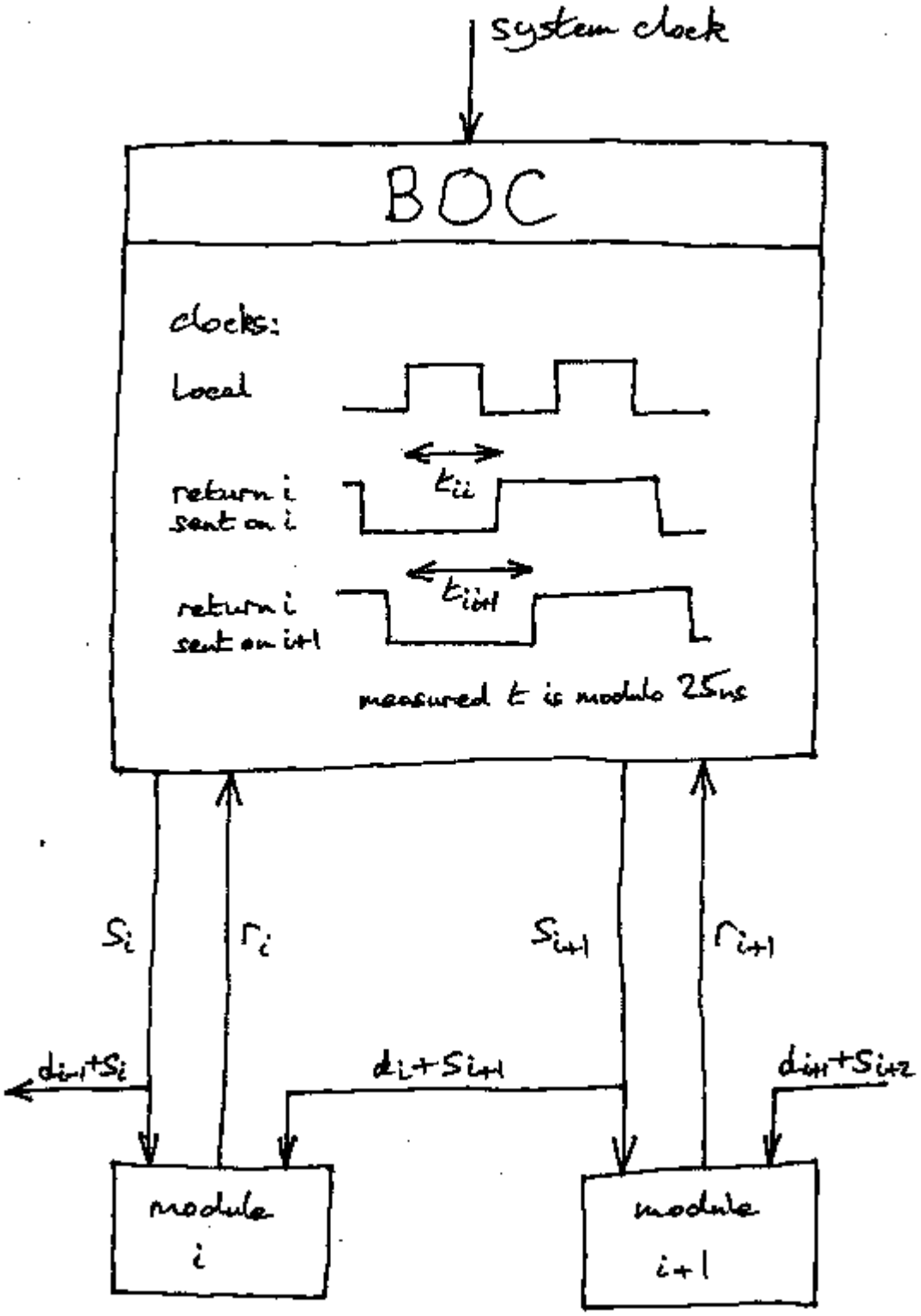
1. An average overall shift in delay for each group of modules is calculated from the channel-by-channel corrections. The average shift may have been constrained to zero for a group of modules forming a ring (the pair-wise synchronization cannot distinguish between delay in the out-going and in-coming links).
2. Using the database information on propagation delays for each link, the mean propagation delay for each group of modules is calculated. This is an absolute delay for each group and gives the relative delays between groups.
3. The channel-by-channel delays within a group are combined with the relative delays between groups, to give a delay correction for each module. This results in all front-end clocks being synchronized relative to the local copy of the system clock in a BOC.

The out-going channel delays calculated above consist of a fine clock delay of modulo 25ns, and a coarse command delay of an integral number of 25ns clock cycle periods. The latter delay is required to ensure that all modules across the detector read out the same bunch crossing.

For data taking, in addition to the above procedure, the internal synchronization needs to account for variation in time of flight across the detector and in delay between and within readout crates.

4. MATHEMATICAL SUMMARY

This section is a brief summary in mathematical terms of the procedure for internal synchronization. The diagram below shows the layout of the scheme.



The propagation delays r and s are for the 'return' data links and the 'send' control links. The BOC measures a time $t \pm \sigma_t$, which is later than the required time at the module by a delay r. The measurement is modulo a clock period, which is accounted for below. For module i, we have measurements with its clock and neighbour clock

$$t_{ii} = r_i + s_i$$
$$t_{ii+1} = r_i + d_i + s_{i+1}$$

where the dogleg contribution is $d \pm \sigma_d$. We cannot solve for s, only for differences. Let us define a difference between neighbours in a group

$$\Delta t_i = t_{ii+1} - t_{ii} - c_i$$

where c is a number of clock periods. We can ensure c = 0, assuming that the propagation delays of the fibres are about the same (25ns is 5m). Let us eliminate r and define a difference equation for s

$$\Delta s_i = s_{i+1} - s_i = \Delta t_i - d_i$$

The Δs are strongly correlated but the Δt are uncorrelated. For a ring of n modules we have the constraint

$$\sum^{n} \Delta s_i = 0$$

which gives a measurement of the dogleg contribution

$$\sum^{n} d_i = \sum^{n} \Delta t_i$$

Within a non-ring group of n modules, an estimator for the difference in delay between two control links, k modules apart, is

$$\hat{\Delta}_k s_i = s_{i+k} - s_i = \sum^{k} (\Delta t_i - d_i)$$
$$\sigma^2 = k(\sigma_{\Delta t}^2 + \sigma_d^2)$$

The maximum variance between distant control links within a group is given by k = n – 1.

Within a group of n modules forming a ring, we can apply the above constraint and get an improved result (k is now modulo n)

$$\hat{\Delta}_k s_i = \sum^{k} (\Delta t_i - d_i) - \tfrac{k}{n} \sum^{n} (\Delta t_i - d_i)$$
$$\sigma^2 = k(1 - \tfrac{k}{n})(\sigma_{\Delta t}^2 + \sigma_d^2)$$

The maximum variance between distant control links is half way around the ring, given by k = n / 2.

We now move on from relative differences to the absolute corrections, including the inter-group contribution. During assembly, the fibre propagation delays were measured, $F_i \pm \sigma_F$. We want a correction for each control fibre delay $\Delta f_i \pm \sigma_f$. We use f instead of s to avoid confusion with the previously defined Δs.

$$\Delta f_i = f_i - \overline{F_i} = s_i - \overline{F_i}$$

The mean F is averaged over the group containing module i. Let us now redefine the earlier difference equation for s into a recursion relation for a group

$$\Delta f_{i+1} = \Delta f_i + \Delta s_i$$
$$\Delta f_1 = 0$$

Within a group of n modules, an estimator for the correction of control link k, is

$$\hat{\Delta} f_k = \sum^{k-1} (\Delta t_i - d_i)$$

$$\sigma_f^2 = \tfrac{n}{4}(\sigma_{\Delta t}^2 + \sigma_d^2)$$

where we have taken the above maximum variance for a ring. This gives a final result

$$\hat{f}_i = \overline{F_i} + \hat{\Delta} f_i - \overline{\Delta f_i}$$
$$\sigma_f^2 = \tfrac{1}{n}\sigma_F^2 + \tfrac{n}{2}\sigma_t^2 + \tfrac{n}{4}\sigma_d^2$$

Smaller rings rely more heavily on the dead reckoning using the measurements F. Possible values for the calibration errors are

$$\sigma_t = 100\,ps$$
$$\sigma_d = 250\,ps$$
$$\sigma_F = 250\,ps \quad (c.f. \quad 5cm)$$

The timing delay offsets downloaded for a data-taking run would also include a time of flight correction, which has a different configuration for beam or cosmics

$$\hat{f}_i + \Delta ToF_i$$

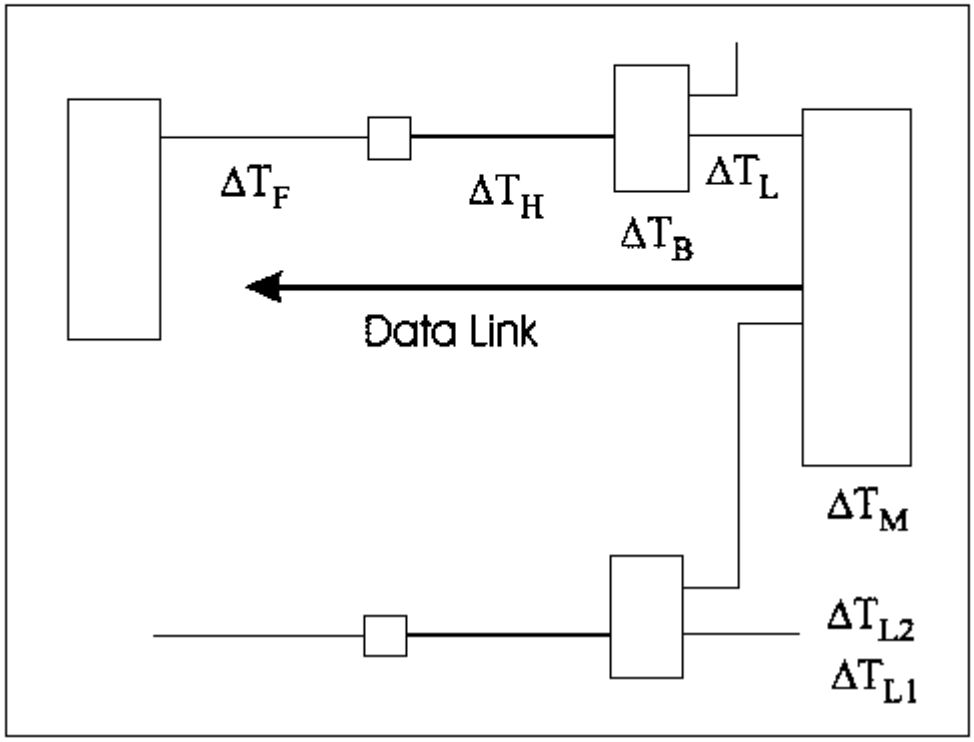
Each of the final delays is separated into a modulo 25ns part for clock delay, and an integral number of 25ns periods for command delay.

The measurements contain additional information not discussed here.

5. CALIBRATION UNCERTAINTIES

This section is a copy of the slides on uncertainties in the calibration of the internal synchronization shown by Nickerson at the July 1999 workshop. I haven't written it up yet.

Synchronisation



Goal for synchronisation is $\Delta T_T = 0.5$ns
where ΔT_T = misalignment wrt LHC clock

A) ΔT flight path is around 3ns within barrel alone

- It is only uncertainties in times that are of interest
- Actual clock times must be corrected for flight times
- Goal is that all clocks arrive at the FE within 0.5ns of each other [modulo flight paths] leaving one overall correction.

B) Uncertainties

Uncertainty = $\Delta T_R + \Delta T_F + \Delta T_H + \Delta T_B + \Delta T_L$
(or sums of squares since number large)

i) ΔT_R

Assume careful design yields 250ps
Calibrate to 150ps
Only differences in timing are important.

ii) ΔT_F

- Assume overall uncertainty in fibre ≤5cm
- 5cm with n=1.5 gives ≈0.5ns uncertainty
- assumed to be random
- Calibrate to 150ps
- Note that CTE ≈ 10^{-5} so 1mm in 100m
- Gives ≈ 100ps over 10°C range

iii) ΔT_H

- Assume uncertainty ≤ 0.5cm
- Gives ≈ 50ps + 15ps over 50°C

iv) ΔT_B

- Small number requested for variation
- Assume calibrate to 150ps
- Plus (?) 100ps for variation in supply voltage

v) ΔT_L
Propagation delay down dog leg & along module
Estimate at 10cm $\varepsilon_r = 6$ (?)
Then T ≈2ns, assume uniform, or calibrated to 5%
Gives 100ps + (?)100ps for supply voltage.

Therefore

$$\Delta T = 150 + 150 + 100 + 50 + 15 + 150 + 100 + 200\ (?)\ \text{from voltage} \approx 1\text{ns}$$

C) Above is 'dead reckoning' and in particular depends on the electronics being very stable.
→ pair-wise synchronisation using clock feed-through.

D) 24 Modules are connected in a ring, with neighbours sharing a return data link in feed-through mode. Error on neighbour synchronisation is then

$$\Delta T = \Delta T_B + \Delta T_L + \Delta T_M + \Delta T_{measure}$$

ΔT_M is taken to be small (?)

Error between neighbours is then

$$\approx 250\text{ps} + \Delta T_{measure}$$

For all modules within one closed loop of 24 to be within 0.5ns, require that

$$\approx\sqrt{6} \times (250+\Delta T_{measure}) \leq 0.5ns$$

$$\text{ie } \Delta T_{measure} \leq -50ps$$

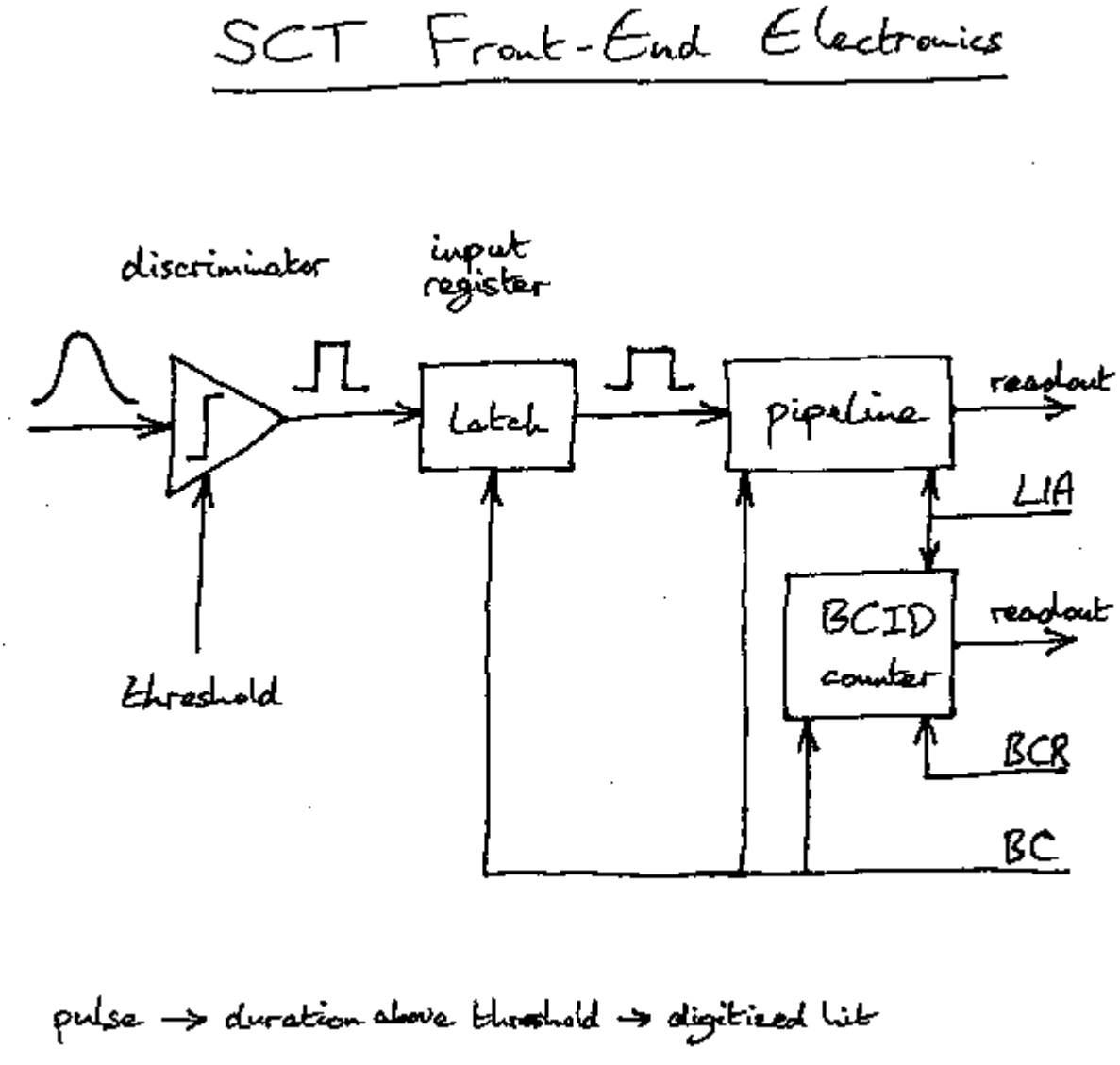
ie

Need as good a measurement as possible, and a good understanding of the opto-board and dog legs.

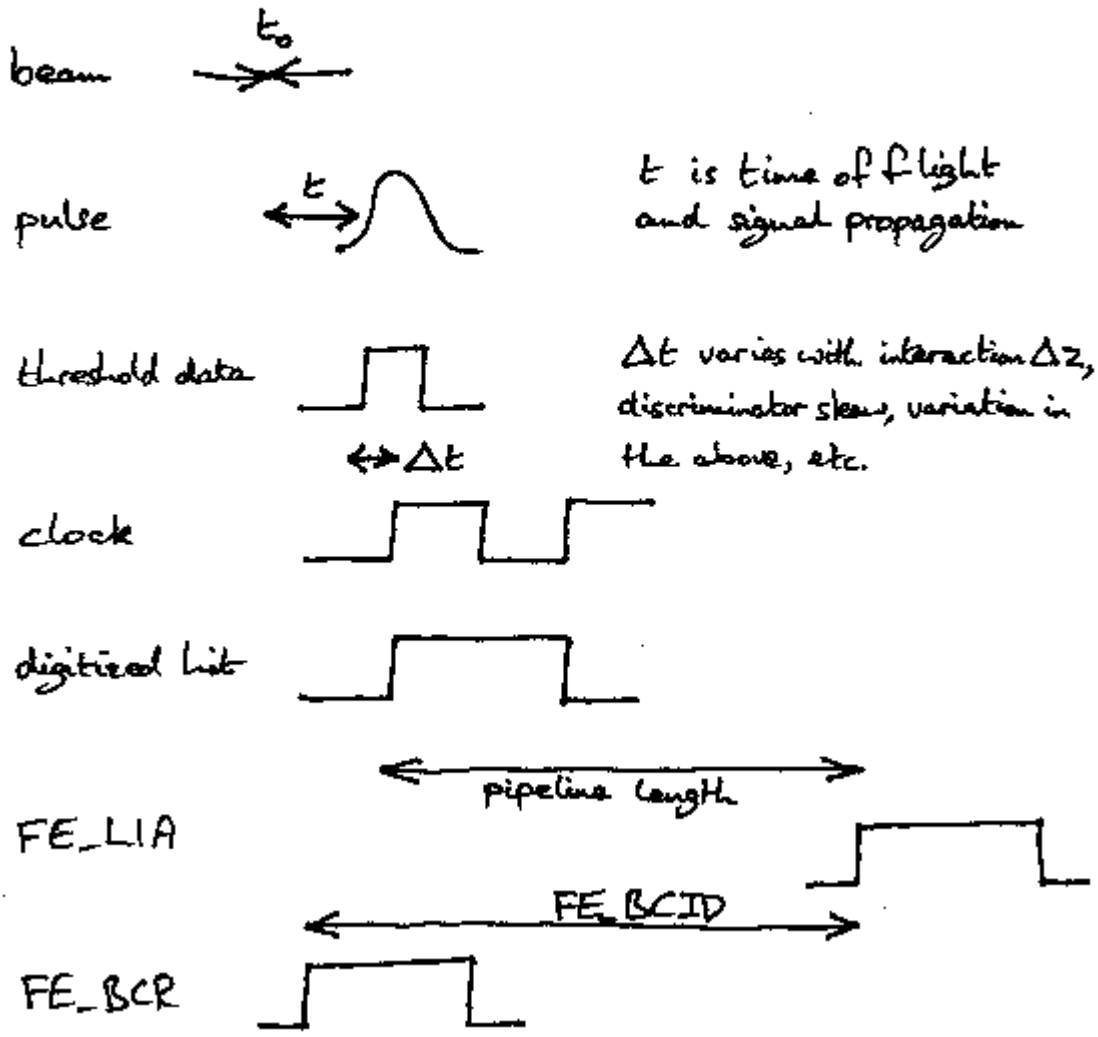
Note that by assuming that the sum of ΔT round the ring is zero, there may be an improvement in the overall error. Analysis not done.

6. SCT TIMING MEETS THE FRONT END

The timing of the SCT in terms of digital clock signals meets the timing in terms of analogue detector pulses at the front-end electronics. This section shows a few diagrams. Are these diagrams appropriate for this document?



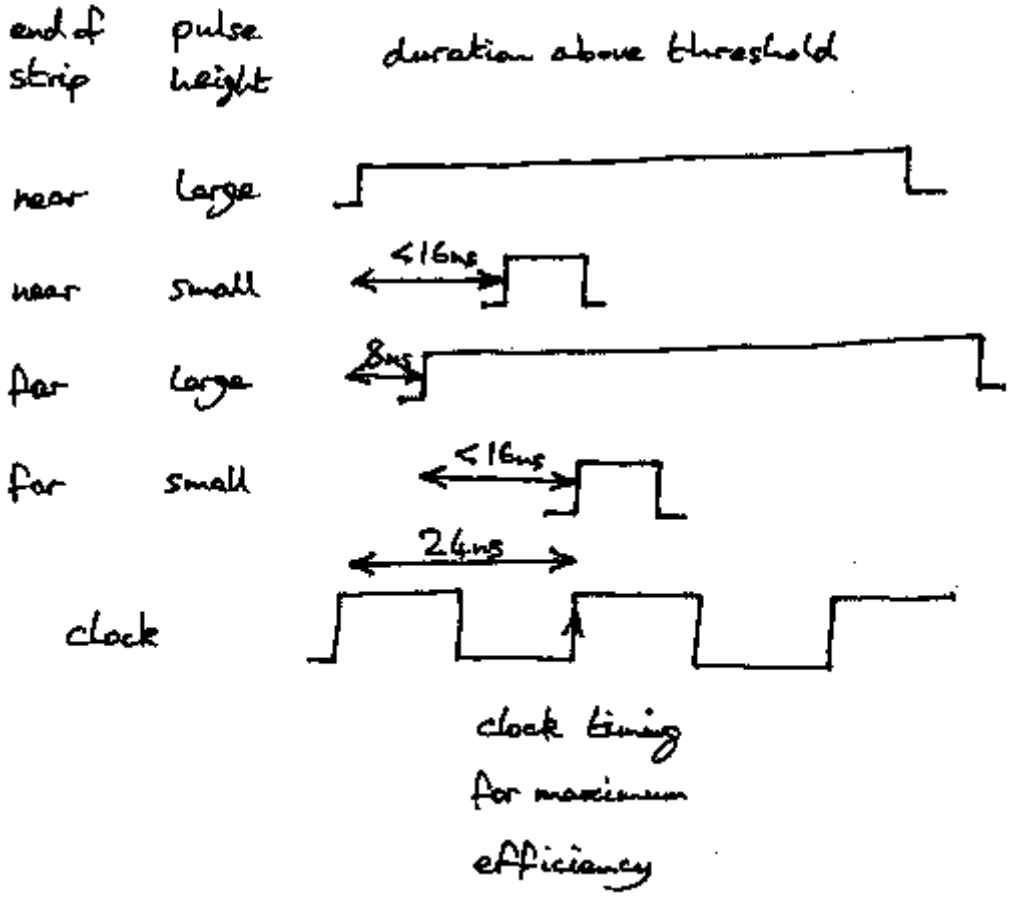
Front-End Timing



Interplay with system clock timing

propagation delay for 12 cm strip 8ns

timewalk from "large" to "small" pulse <16 ns spec



clock timing for maximum efficiency

7. REFERENCES

On the Web via SCT timing Web page at http://www.hep.ucl.ac.uk/~jbl/SCT/SCT-timing.html:

L1TDR: ATLAS TDR 12, Level-1 Trigger Technical Design Report, CERN/LHCC/98-14 (1998)

SYN94: R. B. Nickerson A. R. Weidberg, ATL-INDET-94-048, Clock and Control Transmission (1994)

SYN96: R. B. Nickerson A. R. Weidberg, ATL-INDET-96-141, Redundancy and Synchronisation in the SCT (1996)

SYN98: R. B. Nickerson A. R. Weidberg, ATLAS SCT Clock and Control (15 May 1998)

BOC99: M. J. Goodrick, BOC Timing Functions (1999+)