

TIM Status

Overview

Availability

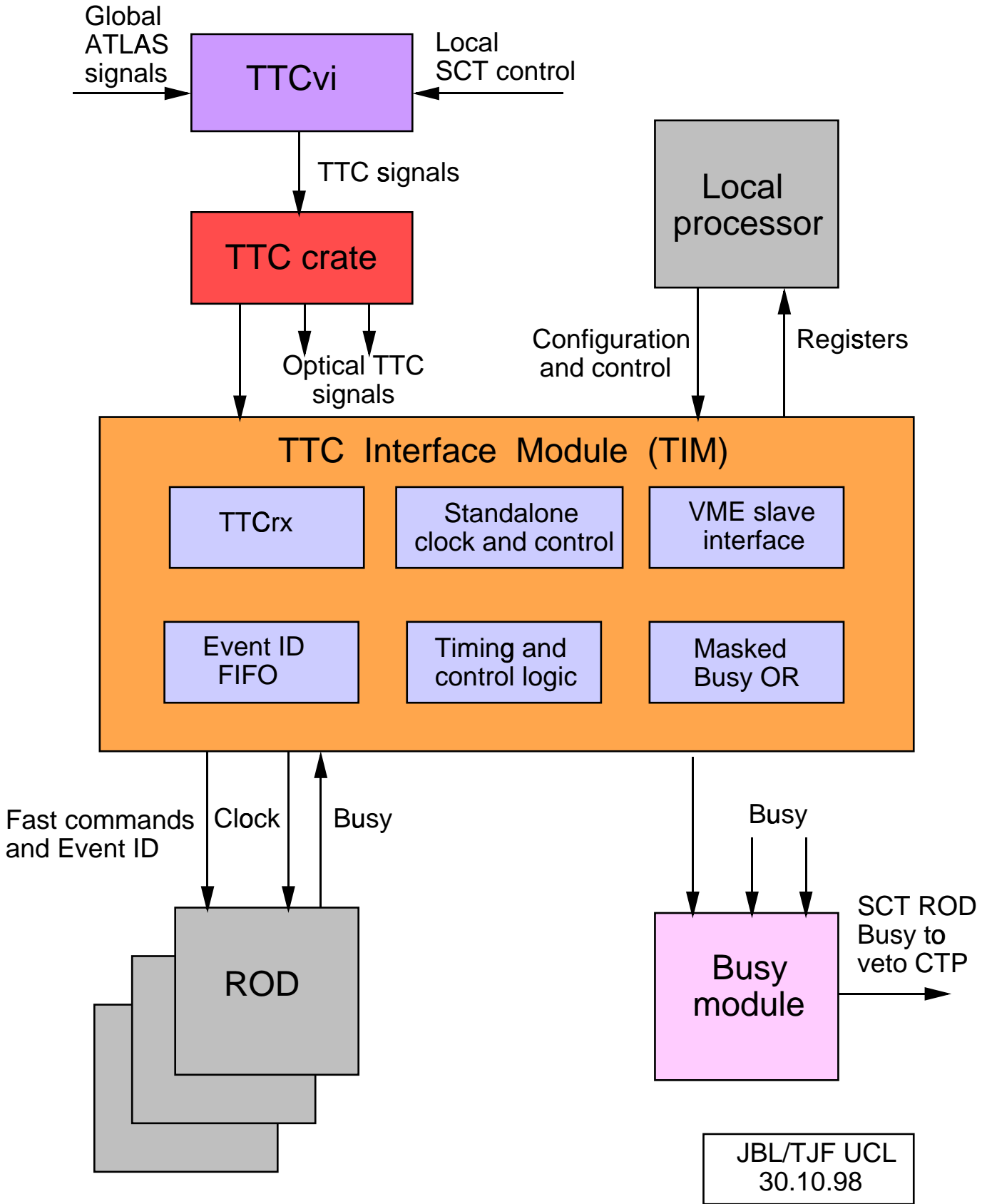
TimModule Class Library

TTC Interface Module

TIM overview:

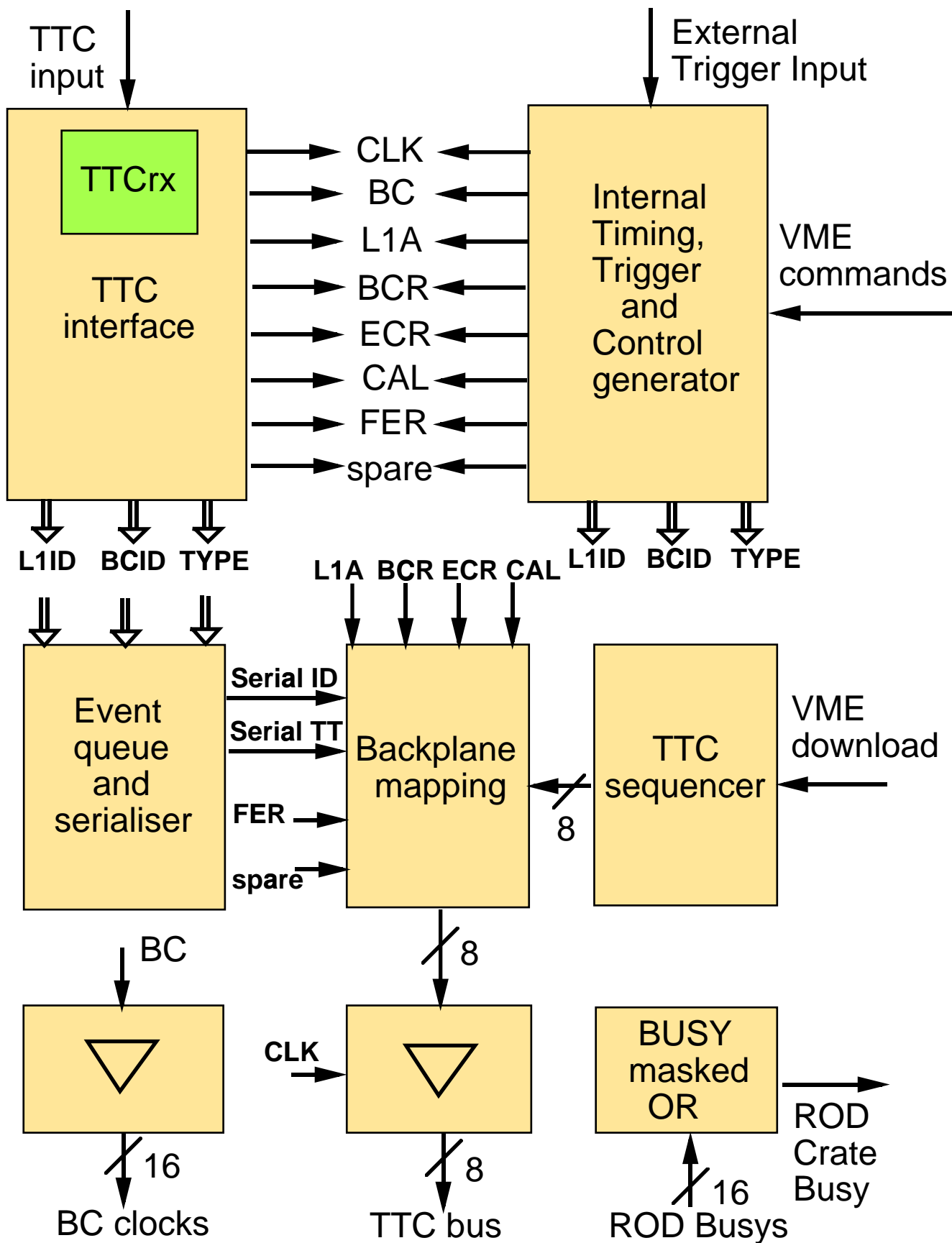
- Operates in TTC or stand-alone mode
- Receives clock and signals from TTC
- Transmits clock and signals to RODs
- Receives busy signals from RODs
- Transmits masked busy signal to Busy module

SCT TIM Context and Essential Model



TIM Functional Model

JBL/TJF 7/8/99
UCL 7/9/99



TIM Availability

- TIM is operational but expect a few bugs to be found!
- TIM is already at Cambridge, CERN, Iowa/LBL, NIKHEF, Oxford, UCL.
- 4 more TIMs are available immediately.

TimModule Class Library

- Status: following RodModule code and learning C++.
- Methods inherited from VmeModule class, e.g. initialize, reset, status.
- Constructor creates a VmePort object and registers it with its VmeInterface object.
- Schedule: first version on 1 Nov.
- I am committed to all TIM software.