

# SCT and Pixel TTC

Introduction

Partitions

TTC Interface Module (TIM)

Requirements

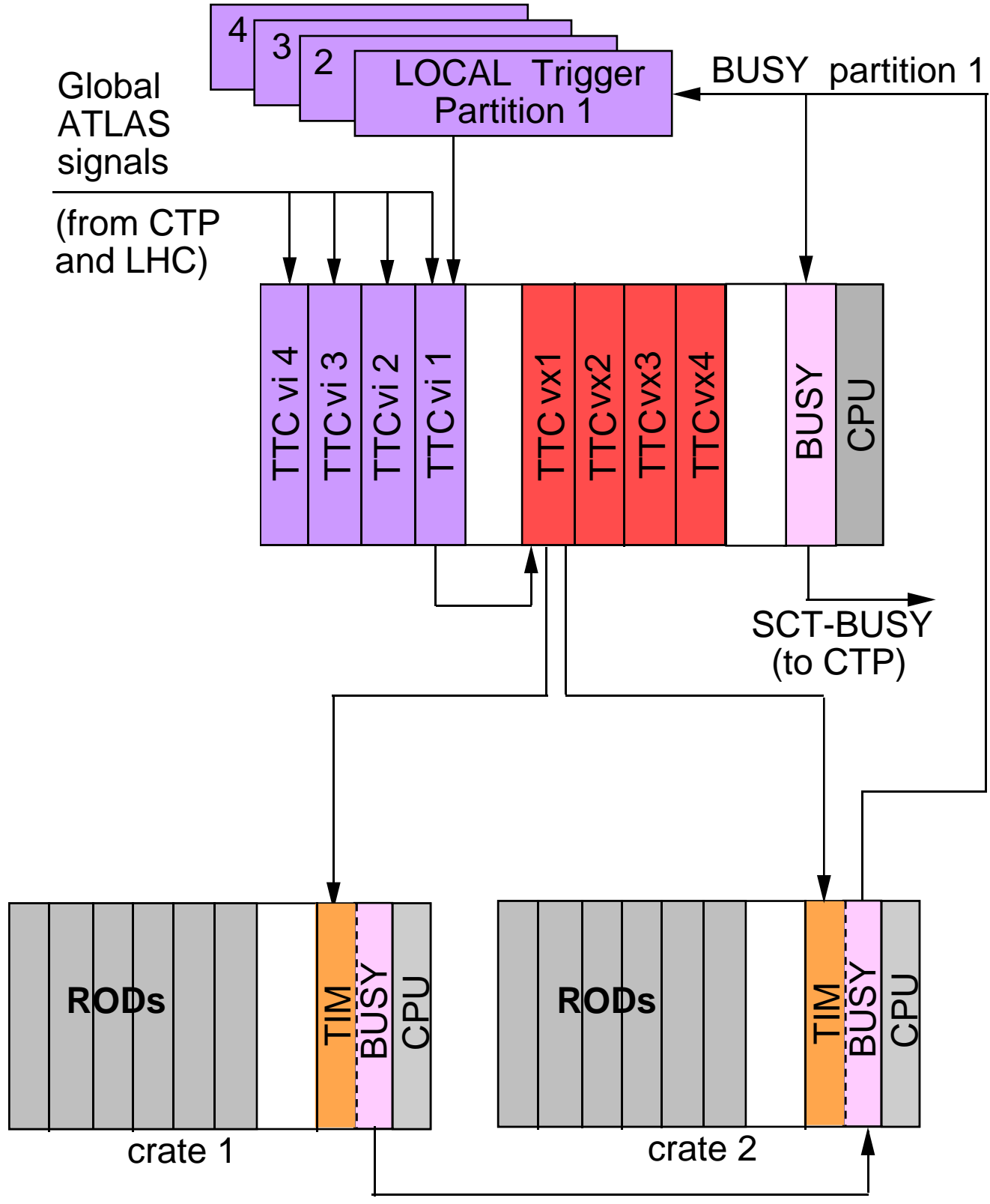
In conclusion

# Introduction

- ATLAS TTC system is used only to the ROD crate level:
  - RODs make a change of protocol for the Front-End
- 4 TTC partitions in SCT:
  - Left and Right Barrel
  - Left and Right End-Cap
- 3 TTC partitions in Pixel:
  - See Kevin's slide
- Up to 16 RODs can be connected to a TTC destination:
  - Each ROD crate has a TTC Interface Module (TIM)

# SCT Partitions of TTC and BUSY

JBL/TJF  
UCL  
26/05/99



## Pixel ROD Configuration

### **Module mapping already defined (for full 3-hit system):**

- B-layer has half-stave per ROD, for a total of 44 RODs
- Layer 1 has one stave per ROD, for a total of 38 RODs
- Layer 2 has two staves per ROD, for a total of 26 RODs
- Disks have four sectors per ROD, for a total of 12 RODs

### **Rod Rack layout (4 racks allocated in USA15):**

- Assume only two ROD crates per rack because of complex service issues involved in bringing large numbers of opto-links in and out of BOC.
- Assume there is an additional 6U VME crate placed in the middle of the rack. This would contain the TTC electronics and any additional test/diagnostic electronics.

### **TTC Partition proposal:**

- Propose that B-layer is one partition of 3 ROD crates.
- Propose disks are a second partition of 1 ROD crate.
- Propose that Layer 1 and 2 are third partition of 4 ROD crates.
- Separating Layer 1 and Layer 2 into different TTC partitions would require two extra ROD crates, because there are only 16 slots per crate available for RODs.

# Partitions

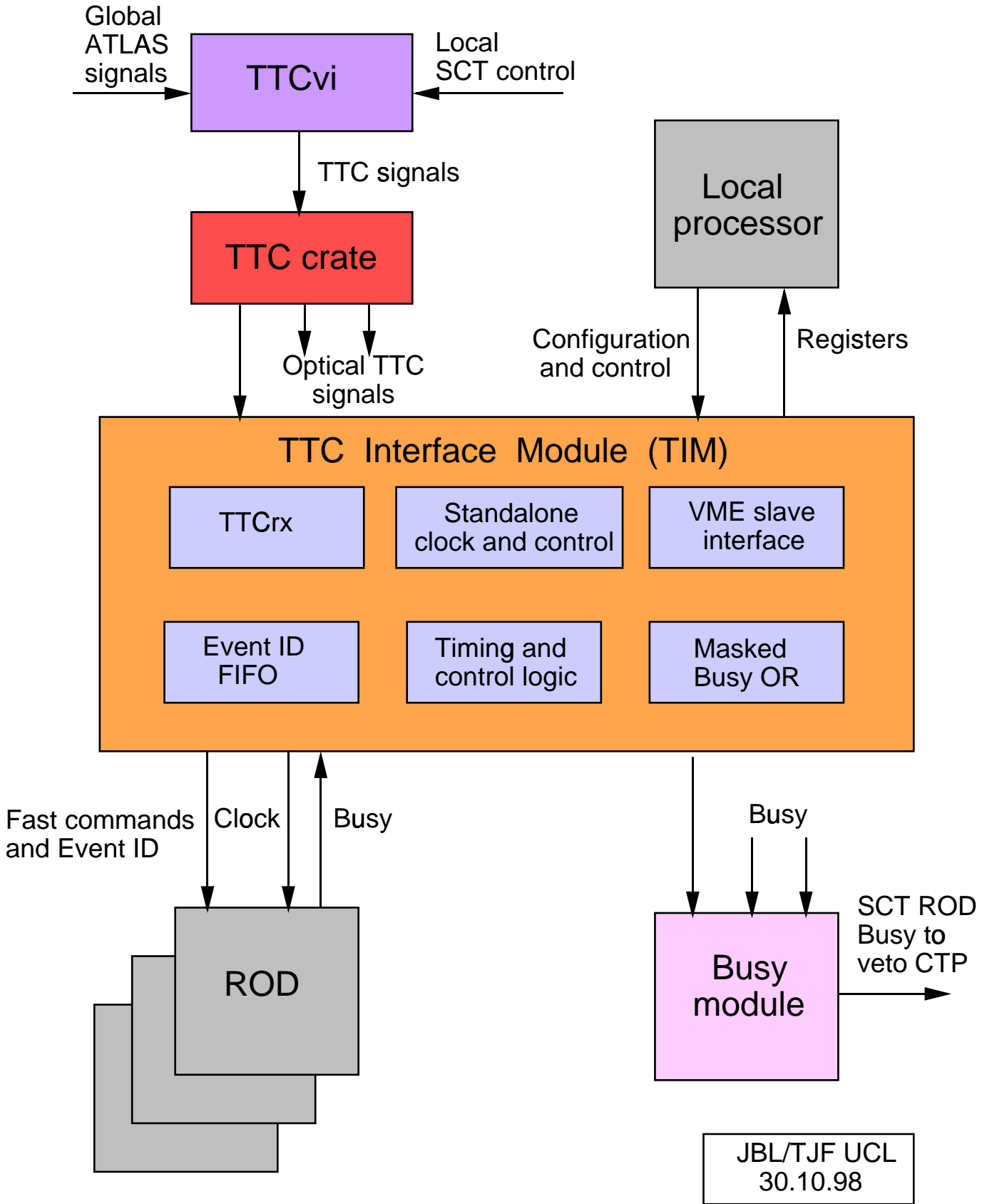
- 4 (3) partitions for SCT (Pixel):
  - Sources are in a 6U VME crate in the ROD racks
- 2 to 5 destinations per partition:
  - 2 (1, 3, 4) ROD crates
  - Level-2 Trigger or TDAQ?
  - no destinations on detector
- In the ROD racks of SCT (Pixel):
  - 1 (1) Busy module
  - 1 (1) cable set from the CTP
  - 4 (3) Detector CTP Interface
  - 4 (3) TTCvi
  - 4 (3) TTCvx or 2 TTCex
  - 8 (8) short fibres
  - 8 (8) TTCrx mezzanines
  - no optical splitters

# TTC Interface Module

TIM overview:

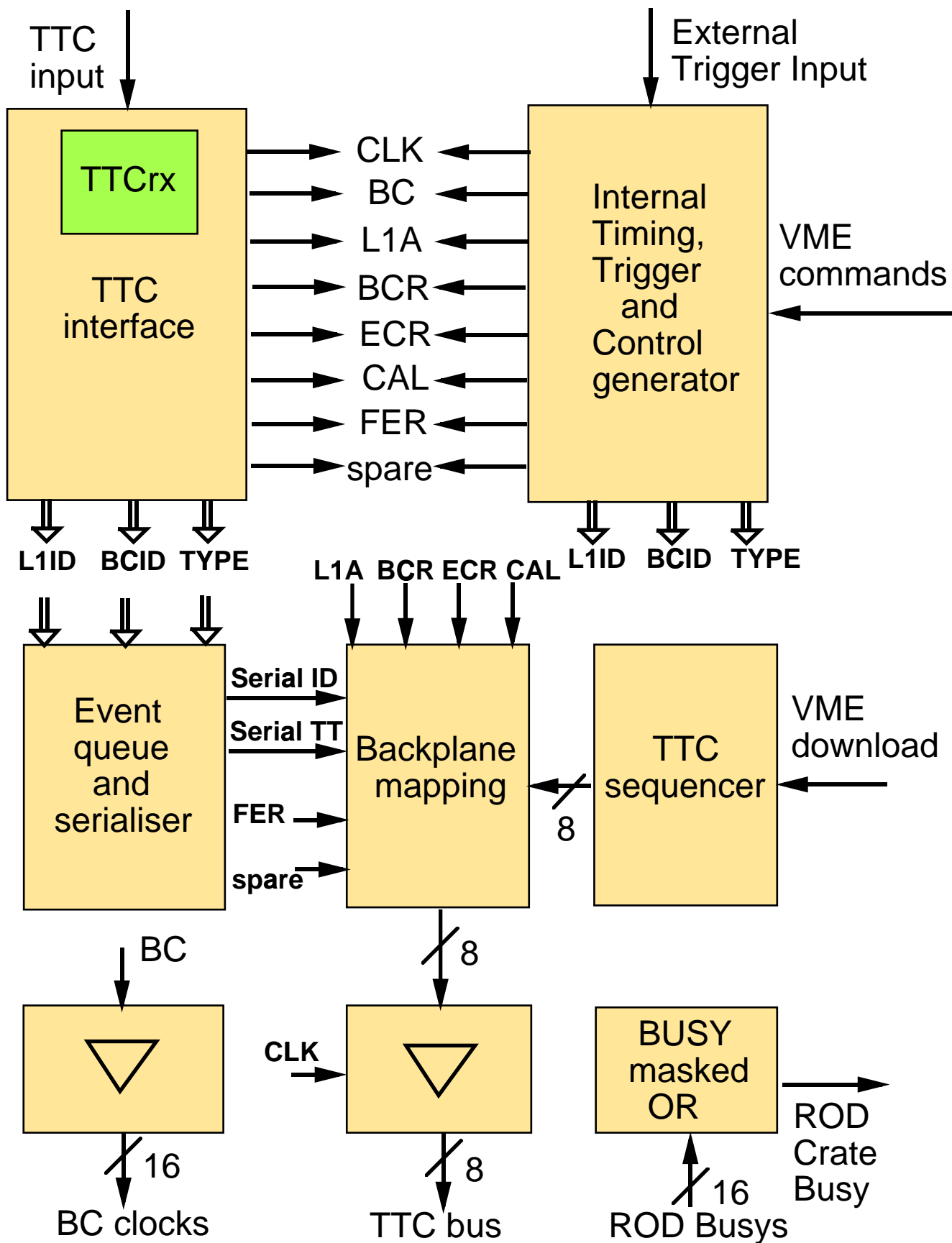
- Operates in TTC or stand-alone mode
- Receives clock and signals from TTC
- Transmits clock and signals to RODs
- Receives busy signals from RODs
- Transmits masked busy signal to Busy module

# SCT TIM Context and Essential Model



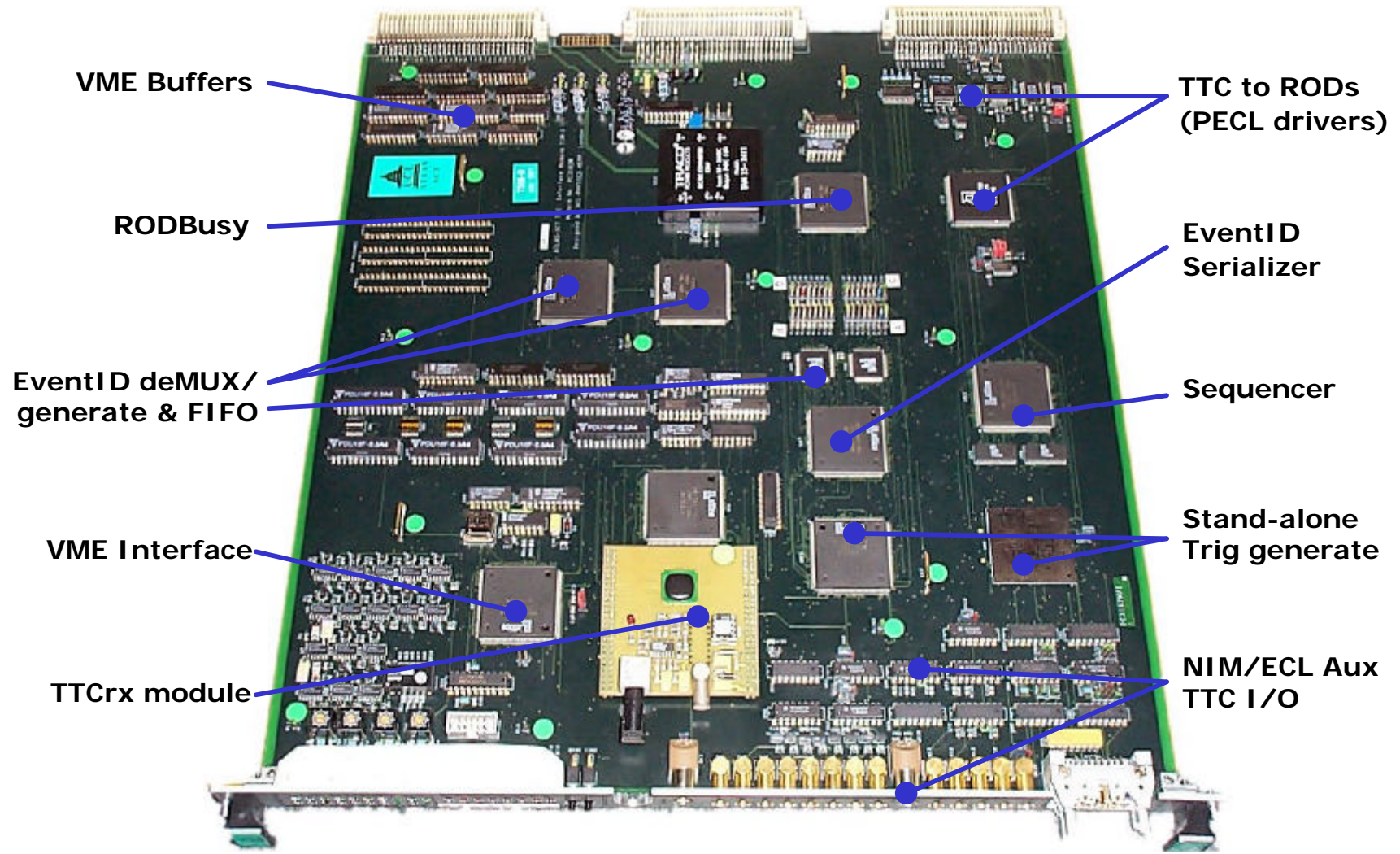
# TIM Functional Model

JBL/TJF 7/8/99  
UCL 7/9/99





# Timing Interface Module (TIM)



# Requirements

- Standard TTC system
- No special calibration requirements
- Latency:
  - The sum of the 3 worst-case lengths
    - CTP rack to TTC rack
    - TTC rack to ROD rack
    - ROD rack to detector
  - should not exceed 140 metres in total

## Survey of SCT latency budget

The overall latency is the time from the interaction until the L1Accept trigger signal is received by the front-end pipeline. The table is a summary of the latency in **Bunch Crossings** and nanoseconds, including which group has the final say in some sense on the latency value.

BC	ns	Latency Item	Latency Responsibility
77.9	1947	Central Trigger Processor output	ATLAS Level-1 Trigger
0.4	10	Fanout module	ATLAS Timing, Trigger & Control
1.6	40	8m cable . . . . . CTP -> TTCvi	ATLAS Technical Coordination
0.1	3	TTC vme interface module	ATLAS Timing, Trigger & Control
0.1	3	0.6m cable . . TTCvi -> TTCvx	ATLAS Timing, Trigger & Control
0.9	22	TTC vme transmitter module	ATLAS Timing, Trigger & Control
6.4	160	32m fibre . . . TTCvx -> TTCrx	ATLAS Technical Coordination
3.0	75	TTC receiver chip	ATLAS Timing, Trigger & Control
2.0	50	Timing Interface Module	SCT Off-Detector Electronics
0.2	5	Backplane of ROD crate	SCT Off-Detector Electronics
3.0	75	Read-Out Driver module	SCT Off-Detector Electronics
0.5	13	Back Of Crate card	SCT Off-Detector Electronics
2.0	50	Bi-Phase Mark chip	SCT Links
19.4	485	97m fibre . . . ROD -> Detector	ATLAS Technical Coordination
1.0	25	DORIC decoder chip	SCT Links
7.0	175	ABC(D) readout chip	SCT Front-End Electronics
6.5	162	SCT Contingency	SCT Electronics Coordinator
<b>132.0</b>	<b>3300</b>	<b>Total ( = Pipeline Length )</b>	

- SCT L1 Trigger Latency Budget Specification ( [pdf](#) or [ps](#) )
- Alex Grillo's overview of SCT L1 Trigger latency and comparison with TRT ( [pdf](#) or [ps](#) )
- The 97m fibre length and routing is under review: [Jan Troska's SCT fibre routing document](#) (superseded drawings: [pdf](#) or [ps](#) or [old](#) )
- The biggest uncertainty is the position of the ROD [racks in USA15](#)
- The 40m (=8+32) is the worst case cable/fibre length from CTP fanout to ROD crate.
- The TTCvi and TTCvx may be nearer to the ROD crates than in the table.
- [More details \(SCT\\_latency.txt\)](#) ; also [email archive](#) and [latency talk](#)
- L1 Trigger latency ( [pdf](#) or [ps](#) ) ; [TTC latency](#)
- [SCT Link fibre installation \(old draft\)](#)

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*Last update: 28 October 1999 (last budget change: 6 June 1999)*

*John Lane (UCL) email: [jbl@hep.ucl.ac.uk](mailto:jbl@hep.ucl.ac.uk) (Please let me know if anything should be changed)*

*[http://www.hep.ucl.ac.uk/~jbl/SCT/SCT\\_latency.html](http://www.hep.ucl.ac.uk/~jbl/SCT/SCT_latency.html)*

## In conclusion

- No special requirements
- Small number of modules and fibres:
  - Delivery schedule is negotiable
  - Detector assembly does not use TTC
- Topics for discussion:
  - TTC input to Level-2 Trigger for stand-alone partitions?
  - Spares?