T/DAQ Interface to Front-end: Requirements and Rules.

Ph. Farthouat, 18–11–98.

- History.
- Main parameters.
- ROD definition.
- Requirements.
- Next steps.

History:

Document written second half of 95

Approval procedure

- Discussed in the community
- EB approval January 96

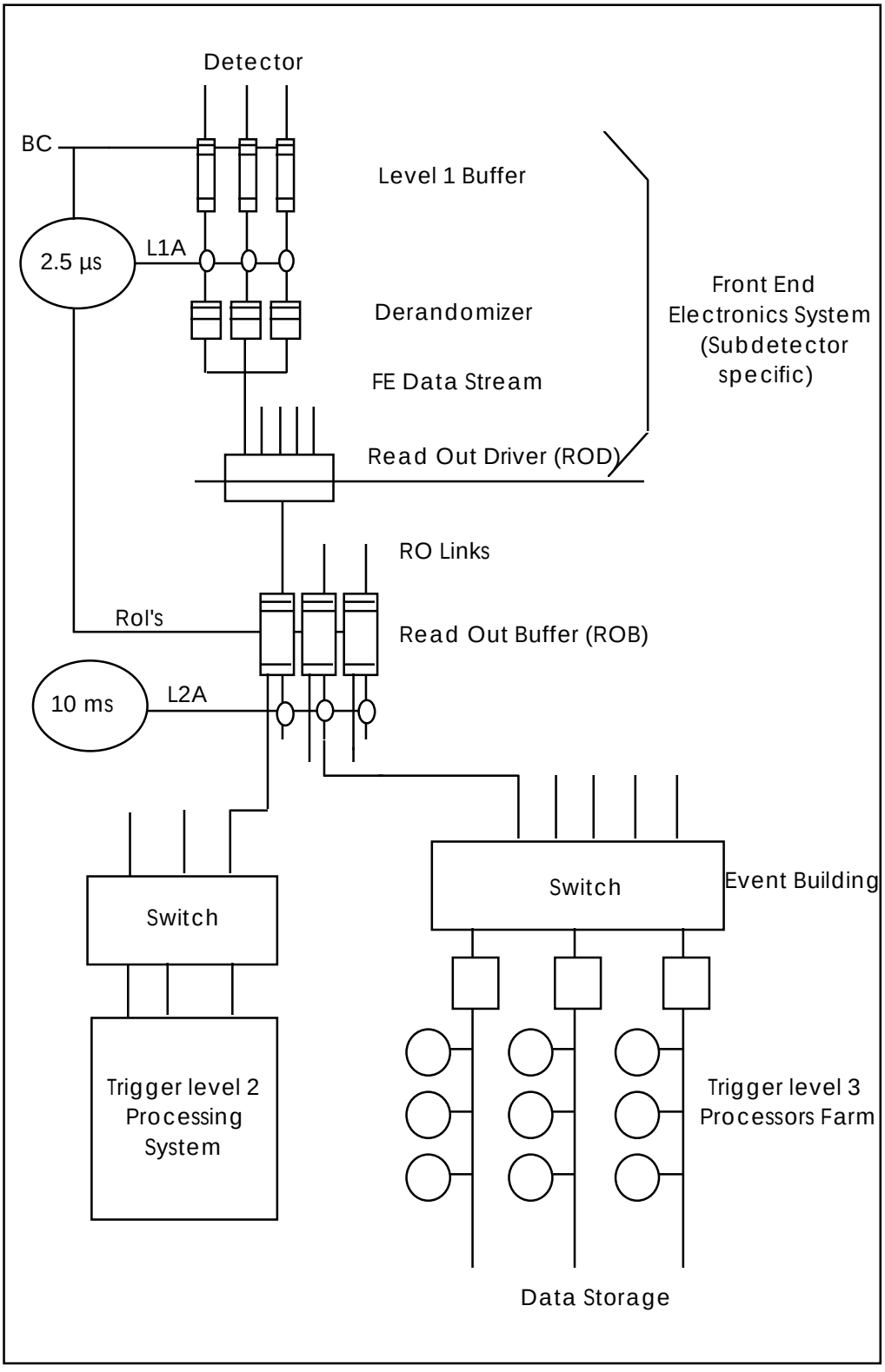
Modified in March 98

- Deadtime requirement update

Main Parameters:

Element	
Clock Frequency	40.08 MHz
Maximum L1A rate	75 kHz upgradable to 100 kHz
Level-1 pipeline length	> 2.5 μs
Minimum interval between 2 L1A	125 ns (4 empty BC)
Raw data read-out time & derandomiser size	To introduce deadtime (or data loss) < 1% @ 75 kHz L1A rate < 6% @ 100 kHz L1A rate

ROD definition:



ROD definition:

Module in between the front-end (detector dependant) electronics and the ROB (DAQ & High Level Triggers)

Contains sub-detector specific parts and ATLAS common parts

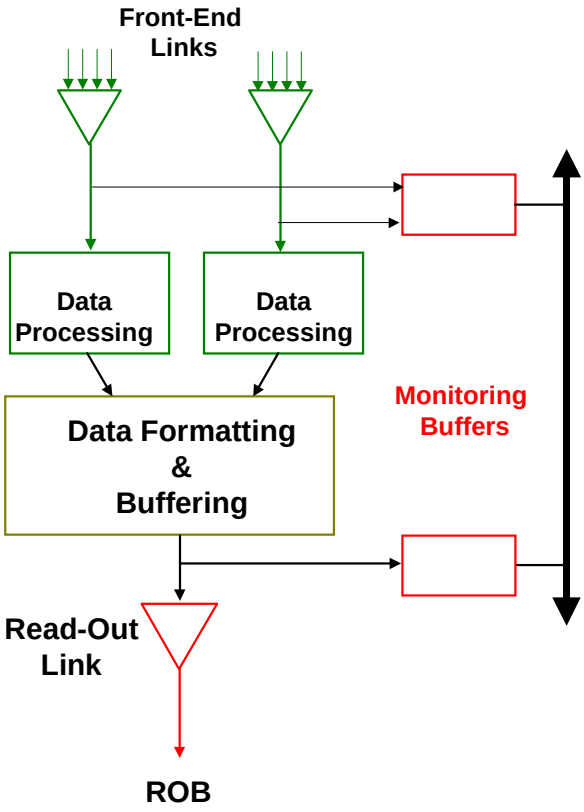
Separated from the ROB in order to:

- have a clear boundary between elements (without mezzanine)
- allow different teams to work independently, in parallel and with different schedules
- much easier debug and integrate the system

Draw-back:

- high speed link to ROB
- total buffer size increase

ROD functionality:



Collect (several) front-end elements

Data processing (Zero-sup., energy extraction,...)

Error detection (data, synchronisation,...)

Receives the TTC

Format the event and interface to the ROL

Monitoring (before and/or after processing) & Calibration

Requirements on the ROD:

Level-1 Trigger:

- Must run at L1A event rate
- Must receive BCID (16-bit) and L1ID (24-bit) from the TTC
- Must check FE_BCID and FE_L1ID
- Must provide a BUSY signal if buffers almost full
- Must follow ROIs segmentation (see P. Ledu's talk)

ROB:

- Format the data according to the ATLAS definition (see D. Francis's talk)
- Interface to the ROB at L1A event rate using the standard Read-Out Link (defined for the prototyping phase. See R. McLaren's talk)
- Detect errors and provide and empty event flagged when it occurs
- Latency: data should reach the ROB 100 μs after L1A (?)

Test & monitoring:

- Monitoring must not introduce dead-time
- Testing facilities must be foreseen

Next steps:

1000 - 2000 RODs in ATLAS

Major element in the read-out chain

- one SCT ROD handles several 10000’ ch.

To be ready in 2001 - 2002 because used during the sub-detectors assembly & commissioning

It’s time to clarify some points

- deadtime handling
- partitioning
- synchronisation
- timing set-up
- initialisation

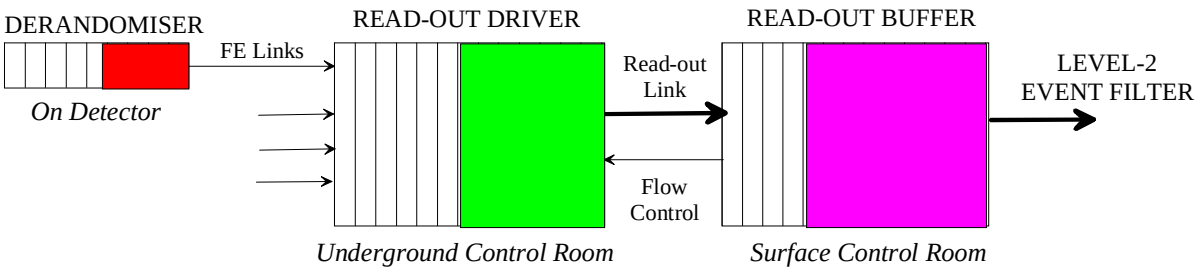
It’s time to prepare decision on some parts

- backplanes, crates
- final Read-Out Link

It’s worth to explore possible commonalities

- hardware (interfaces, components,...)
- software

Deadtime Handling:



Buffers are filling in different places

Deadtime to be introduced as necessary

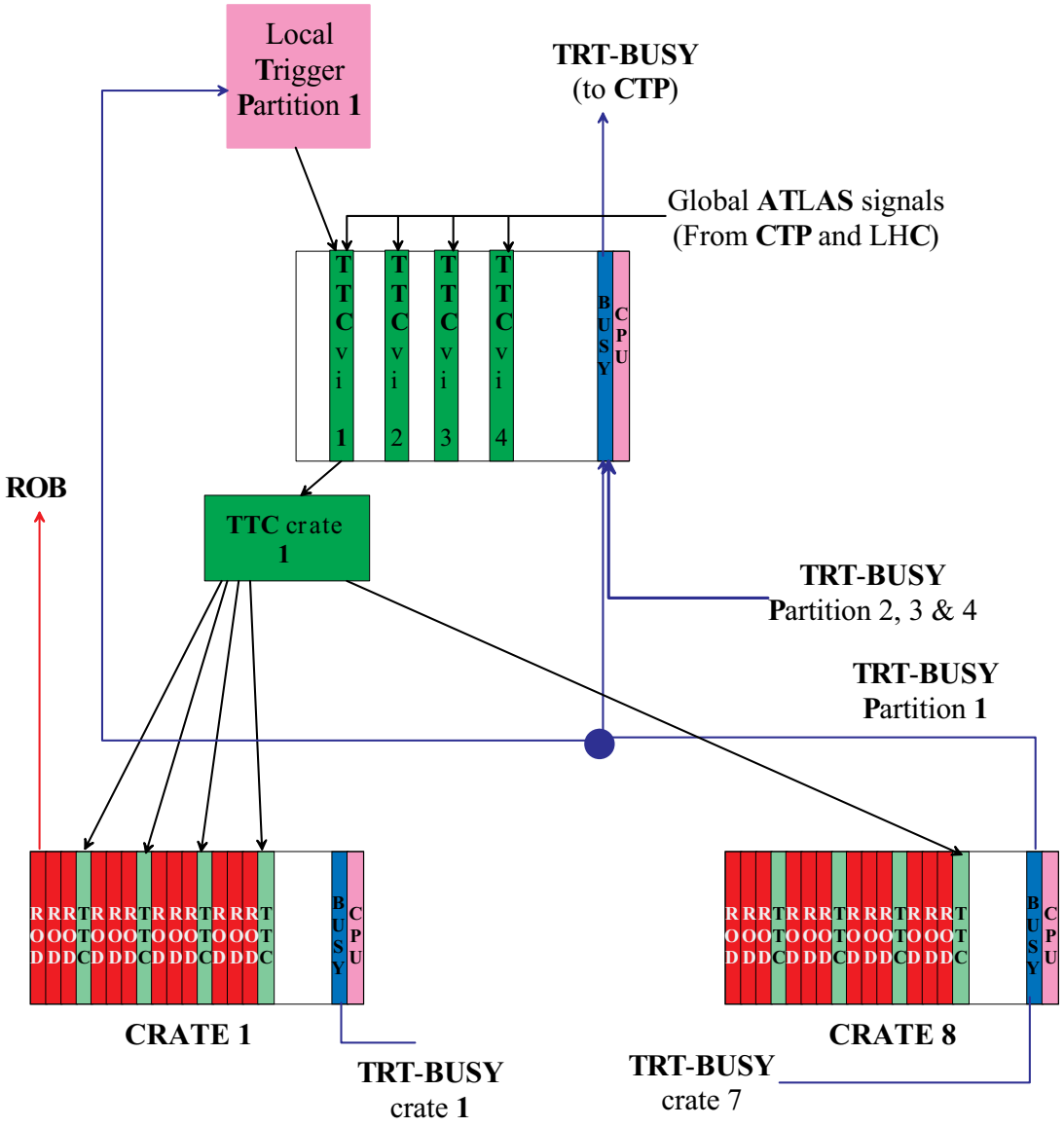
Handling in three different manners

- Derandomiser: in the CTP
- ROD: BUSY signal
- ROB: back pressure on the ROD

Presentation on Friday morning

Partition:

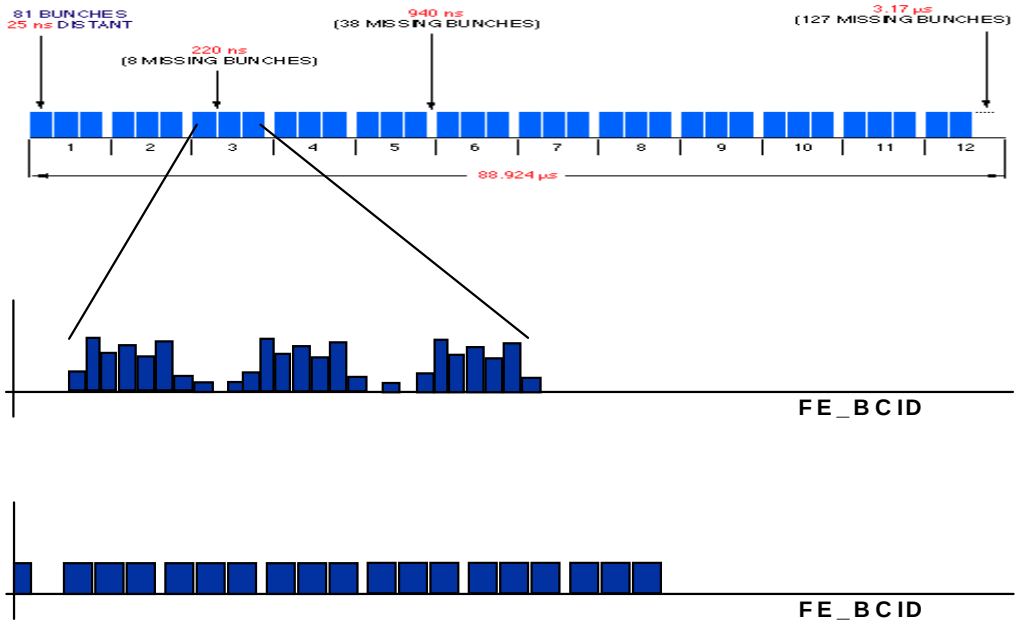
TTC, Deadtime handling



Sub-detector requirements

Proposed solutions: TTCvi, BUSY module

Timing set-up:



Proposed scheme

May require functionality in the ROD crate

Synchronisation:

BCID and L1ID

Some sub-detectors have no FE-BCID

Need for periodic RESETs

L1ID reset

To be defined

Initialisation:

Before a run start some initialisation sequences have to be performed

Is the proposal of using the BUSY signal agreed?

Crates:

Most of (all?) prototyping in VME 9U

Questions:

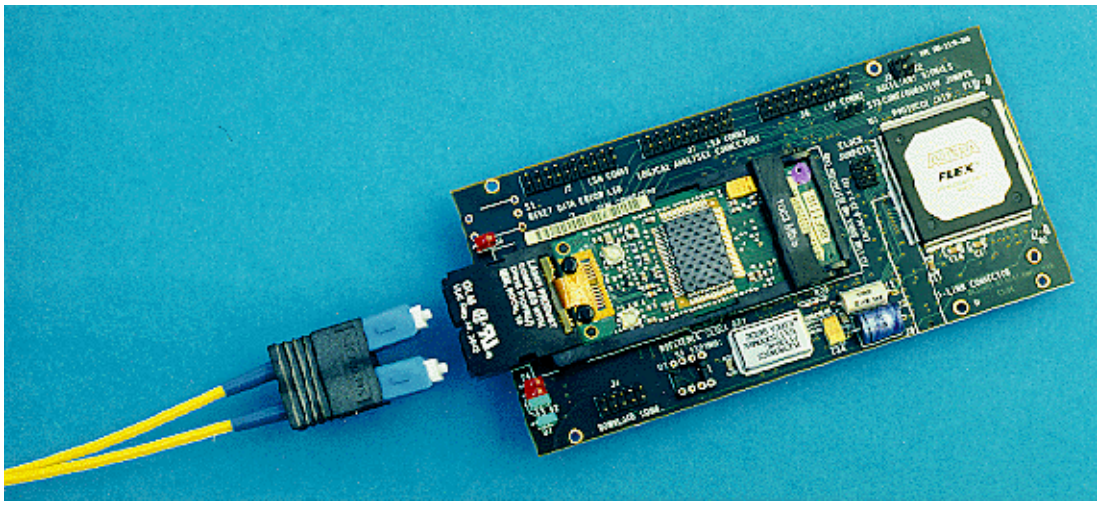
- Standard VME or “VME for Physics” extensions?
- VME64ext, VME320?

What do we know:

- Study requirements
    - From this workshop
- Low cost is a common requirement
    - Limit number of types and hence increase the production quantity
    - Use as much as possible standard components
- Long term maintainability
    - including upgradability (CPU)

Status of the standard on Friday afternoon

Read-Out Link:

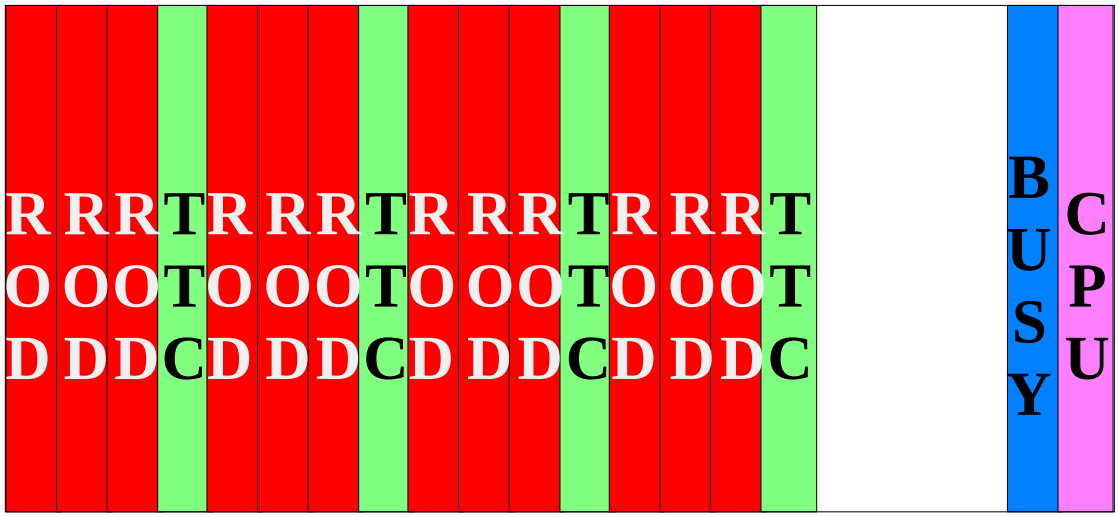


S-Link has been defined to allow easy prototyping

Should consider what is needed for production:

- keep S-Link or similar concept?
- keep mezzanine concept?
- implement the link on ROD?
- select the physical layer?

Possible commonalities:



Interface to backplane(s)

- So that it looks the same from the crate processor point of view
- TTC distribution?

Common elements in the ROD crates

- Processor

Common software

- Common framework?

Summary:

Use this workshop to study the requirements and have a first in depth discussion

A complete session with the Detector Interface Group (DIG) should allow to clarify the software needs

May lead to the creation of a ROD working group to organise the follow-up