Appendix A

Feedback Circuit Trimming Procedure

This appendix details the trimming procedure used to correctly set the voltages for the FONT feedback circuit board, as mentioned in Section 5.3.2. A 10 MHz 100 mV CW source was used as the reference signal: using a sine wave input, rather than a DC pulse, ensured that the offset at each pair of pins was correctly nulled, since a combination of the three voltage offsets (X, Y and Z+W) could produce zero output without any of them being correctly zeroed. A scope probe was connected to the output pin of each chip being monitored to measure their outputs. Refer to Figs. 5.24 (page 181) and 5.26 (page 185) and Sections 5.3.1 and 5.3.2 for the chip ID and pin numbers used in the following description.

The input to chip 2 was driven with the sine wave, with all other connections terminated. The voltage on pin 7 of chip 4 (the Y2 input) was adjusted with the variable resistor until the output of chip 4 became flat (indicating that the combination of all voltages at pins 7 and 8 is zero). The voltage on pin 4 (the Z input) was then adjusted until the output of chip 4 was zero. The process was then repeated with chips 1 and 3, driving the input of chip 1 with the sine wave and adjusting the voltages on pins 2 (the X2 input) and 4 of chip 3 until the output of chip 3 becomes zero. The BPM sum and difference inputs were then grounded and the AWG input driven with the sine wave input set at 1 V. The voltages on pin 2 of chip 4 and pin 7 of chip 3 were then adjusted until the output of chips 3 and 4 was zeroed. The voltage at the Z input of both chips was then readjusted to ensure that it matched with the first voltage setting.

Having trimmed the voltage offsets for the sum and difference multipliers, the next stage was to correctly trim the voltages on chip 5. The variable resistor on pin 1 of chip 5 was set to 0 V and the BPM difference input to chip 1 grounded. A 14 dB attenuator was connected to the BPM sum input and the AWG and BPM sum inputs were driven with the 1 V sine wave[1]. The output of chip 5 then shows a $\sin^2$ output as a result of the multiplication of the chip. The voltage on pin 7 of chip 5 was then adjusted until the output of chip 5 became flat. The voltage on pin 4 was then adjusted until the output was zero. The sine wave generator was then disconnected from the sum input and reconnected to the difference input, with the sum input grounded (producing the same $\sin^2$ output as before). The voltage on pin 1 of

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[1]A 14 dB attenuator provides a factor of 25 reduction in power and therefore a factor 5 reduction in voltage, dropping the peak-to-peak voltage to the BPM sum input to 200 mV.

chip 5 was then adjusted until the output of chip 5 became flat: this voltage was measured at 10 mV. The voltage on pin 1 was then reset to 1010 mV to provide the correction given in Eq. (5.14), page 183: this completed the voltage trimming procedure for the normaliser part of the circuit.

Using the same sine wave generator setup to provide a 1 V sine wave input to pin 8 of chip 8, the gain adjust for chip 8 (pin 1) was grounded. The voltage on pin 2 of chip 8 was adjusted until the output of chip 8 became flat. Next, the AWG and BPM sum and difference inputs were grounded and the sine wave generator connected to the gain adjust input to chip 8. The voltage on pin 7 of chip 8 was then adjusted until the output of chip 8 was zeroed. Finally, the feedback loop monitor output was terminated with a 50 Ω terminator and the pulsed gain adjust input to pin 1 of chip 9 was grounded. Chip 8 was removed from the board and the sine wave generator was connected to the feedback amplifier output, thus driving pin 8 of chip 9 with a 1 V sine wave. The voltage at pin 2 of chip 9 was adjusted to flatten the output of chip 9. The feedback amplifier and loop monitor outputs were then grounded and the sine wave generator connected to the pulsed gain input of chip 9. The voltage on pin 7 of chip 9 was adjusted until the output of chip 9 became flat. The final step was then to adjust the voltage on pin 4 of chip 9 to zero the output of chip 9, completing the full trimming procedure for both circuits.