Questions and Answers from 23-Jun-2010 meeting

24.6.2010 v1 CY

1 Attendance and why are we sitting here?

WP76: D.Wilson and C.Youngman
Petra3 J.Viefhaus, J.Klute and H-T.Duhme
UCL: E.Motuk, M.Wing, M.Postranecky and M.Warren

Jens Viefhaus: scientific officer for a beam line at Petra3. XFEL bunch period (220ns) and 40 bunch operation at Petra3 (192ns) are comparable. XFEL/Petra3 bunch duration 100-200fs/10-20ps with experiments sometimes wanting to probe the sample with lasers – these users exists at FLASH, FLASH2, PETRA3 and Eu.XFEL hence the idea of combining a DAQ with fast ADCs and hence his interest. Currently responsible from the user point of view for organize timing and because of this the connection to Jens and Hans-Thomas. In this respect looking for a solution that will work everywhere cost effectively.

Hans-Thomas Duhme: working on providing the bunch clock system at Petra3 among other things.

Jens Klute: workpackage leader for timing and feedback systems at Petra3.

UCL is contracted by Eu.XFEL to develop and produce the synchronizing clock and control system for the 2D cameras being developed for use at Eu.XFEL. Part of the project definition is that these systems can be used at other light sources (LCLS, Petra3…). WP76 coordinates the 2D control and readout development, but is also developing DAQ and control systems as challenges before Eu.XFEL operateration begins and hence WP76 involvement with Ch.Bressler's experiment being setup at Petra3 (and later Eu.XFEL). Both 2D and Bressler developments have considerable overlap w.r.t. timing which is why we are all sitting here – the aim is to find a solution that works everywhere cost effectively.

2 Discussion

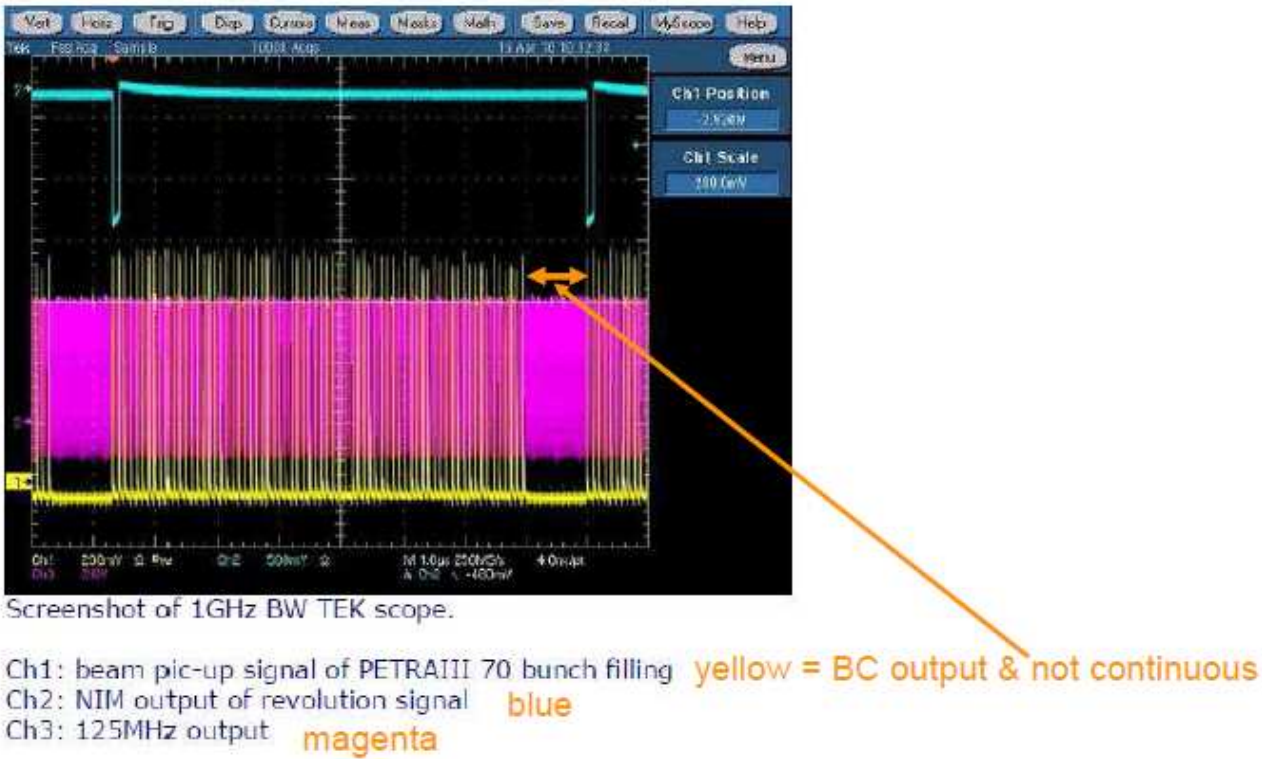
As an introduction Jens showed three slides showing the Petra Bunch Uhr (clock) 1U rack unit (J_Klute_PBU_23Jun2010.pdf). Herman Franz specified for Petra3 that a module be made available for each user based on the design used at Doris – this is conceptually a simple design and provides NIM/TTL signals and clocks to the user.

Picking out the PBU features of interest within the context of this week's meetings:

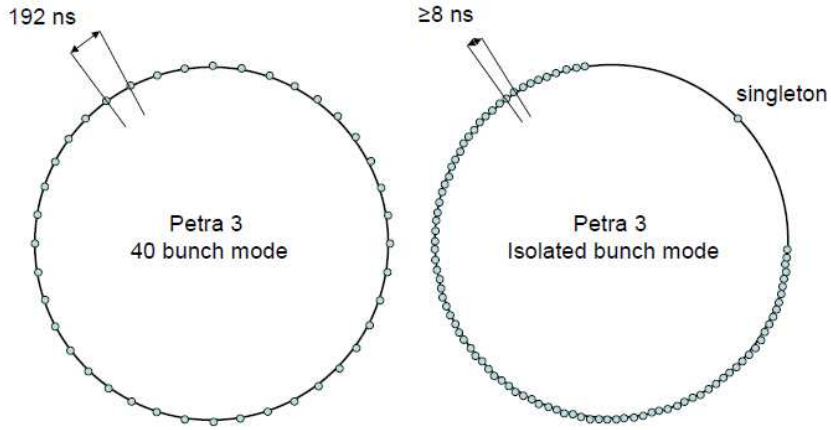
- 40 MHz clock with data encoded onto drives the PBU [similar concept to XFEL TR xTCA board 1.3 GHz input]
- an output (NIM/TTL) unit consists of:
  - BT – bunch trigger (= 130 kHz = revolution rate) [XFEL start telegram viewed as clock]

    - BC – bunch pattern clock (8…192… ns) [equivalent of XFEL bunch clock, e.g 4.51MHz… modulate with the XFEL bunch pattern]
    - Thumb wheels to shift the BT output in 1 ns steps (timing in) [hand timing in version programmable delay features in the XFEL TR associated with telegram events}
- 3 bit octal Petra3 operating mode (filling, topping up…)
- There are 3 independent units per PBU
- 83.33, 125 and 500 MHz clock outputs synchronized to BC with jitters of ~50 ps
- RS232 serial link allows internal configuration (set from encoded 40 MHz and thumb wheels(?) to be readout.

BC can be continuous or non continuous. A scope shot showing BC (channel 1), BT (2) and 125 MHz (3) clocks, see below, for a 70 bunch fill with 96 ns between bunches illustrates a non continuous BC signal.



The Petra3 revolution period is 7680 ns, so a filling can contain 80 bunches x 96 ns spacing, or 40 x 192, or 960 x 8 … or even more exotic fills as shown below.



Notes relating to Petra3 operation:

- BC is not continuous as it is modulated by the filled bunch pattern.
- The bunch pattern changes infrequently, typically once per shift and at most once per hour, unlike XFEL where the bunch pattern can change between consecutive trains (hence the need for a bunch pattern index telegram in the TR). The pattern used may or may not (could not work this out) be set using telegram information encoded in the 40 MHz input. Seems to be a manual setup.
- There are 7 storable filling patterns in the PBU.
- Ch.Bressler's experiment in 2011 wants to use the singleton pulse (rate = BT = 130 kHz) for measurements. In 2012 the 40 bunch mode will be used.
- The PBU will be modified using feedback

Notes relating to XFEL 2D pixel detectors:

- The 50 ps clock jitter is compatible with 2D detector operation requiremenst.
- The BT signal should be used as the (XFEL like) START for measuring the singleton bunch only.
- The bunch clock used would have to be generated by dividing down the 125 MHz clock to a settable value (125 / 24)
- The DAQ readout operation mode has to be defined – we have to emulate a train mode including the period of time when data is not taken which allows the pipelined data to be passed on to the backend. We have to define the mode which each camera wants to acquire data – this depends, amongst other things, on how much time is charge allowed to sit in the pipeline as it leaks away. AGIPD thought about acquiring a complete storage pipeline of ~400 bunches = 76 µs at 192 ns bunch spacing followed by a readout period of 100ms. Acquiring 400 singletons would require 3 ms which possibly becomes critical for storage cell leakage.

Notes relating to Ch. Bressler's single crate DAQ system:

- The XFEL 2D notes apply here, except the DAQ readout mode which can be continuous at 192 ns bunch spacing – there are no bandwidth issues due to data size. Data is also digitized immediately – there are no storage cell lifetime issues.

3 Conclusions

The XFEL TR can probably be used to interface 2D and single crate DAQ systems, this requires:

- Copper inputs to TR:
  - Start = BT
  - Bunch clock = 125 MHz divided down to the appropriate rate (125/24 = e.g. 5.208333 MHz)
  - Additional input for Laser tagging.
- The input Start needs to be injected into the EncClock (currently 108MHz) TR bussed line (RX17 – TX20).
- The Bunch clock needs to be distributed as the p2p TCLKA TR line.
- The additional input needs to be injected into the EncClock, or inserted onto a spare bussed line (RX17 – TX20).
- Signal conversion NIM/TTL to LVDS…

We need to find out whether Uwe Hurdelbrink is already working on interfacing Petra3 timing to the XFEL TR because may be he's already written the firmware required.

- Phone him and find out.
- If there is such a development – which users requested it?

Possible requests to the PBU designers:

- Allow access to LVDS output signals from PBU's FPGA.

We will document the functionality that we want to use from the PBU and send it to you within the next few weeks (i.e. when we have fully worked out what we are doing).

4 Misc. open questions

What is on the TR RTM?