Modified Tracker Readout for Demonstrator

M. Carter, S. Kolya, R. Saakyan, J. Sedgbeer, S. Soldner-Rembold, J. Thomas, R. Thompson, D. Waters

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Objectives for SuperNEMO Tracking Readout

This note describes the proposals for modifying the objectives for the tracking readout work package in the SuperNEMO Demonstrator phase, the reasoning behind these plans, and the cost implications.

Our initial bid for the Demonstrator phase was submitted in February 2009 and so reflects the situation at that point. The subsequent descoping exercise and significant delays in funding the Demonstrator project have led to changes in the original programme. The tracking readout work package has had to also be revisited.

The motivation behind modifying the readout programme is summarised below:

- The R&D for the readout starts now. The basic R&D for the tracking detector has been taking place over the last few years in the previous phase and the detector work is now moving into the production phase. By contrast, we are only starting the readout R&D now - this was explicitly excluded from the previous phase following the PPRP recommendation. While both the R&D and production can be accommodated within this phase, the TDR can only be finalised after the R&D is complete. It is entirely proper and desirable that the readout design should lag the detector design.

- The full detector specification is an essential input to readout design. Some key elements of the specification are missing, for example, work is ongoing on how the detector will be cabled. SuperNEMO cannot place amplifiers on the detector and the cable connections, feedthroughs etc. are very important components of the final signal characteristics. It would be dangerous to specify an ASIC before having this specification – ideally having a prototype to study.

- The 90-Cell prototype is not necessarily the best way to specify the readout for our final Demonstrator design. Not only because of the external issues (cabling etc. above), but also because the wire used was not the final (cleaned, treated) wire as will be used in the Demonstrator. A number of questions about the tracker performance and pulse characteristics will inevitably have to be studied in the Demonstrator phase.

- Ultimately we would like to implement a readout that is only cabled at the top of the detector, but as this is not proven it has been decided to cable the Demonstrator top and bottom anyway. So some changes to the readout are already foreseen between Demonstrator and full production. The current plan is to have additional amplifiers/ discriminators on the ASIC which we would not expect to use in full production – this is wasteful.

- The final de-scope allowed us to build only ~1/3 of the required channels at most. This is only a sensible choice if we are confident that substantial follow on funding will be available immediately after this phase completes. In the current economic climate this seems questionable, and a better choice would be to use the available funding to instrument fully the Demonstrator to deliver the physics programme, while at the same time being mindful of the longer term goals of the project.

Summary of existing proposal

The baseline design for the readout as presented in our bid is summarised here. The basic repeatable unit of the readout is the readout crate that accommodates all the required bespoke electronics, taking signals directly from the cells at the input and outputting data to a COTS networking and computing structure. The crates will also link to the central clock & fast control system (being developed by the French groups).

The system is directly scalable. Any size of detector can be accommodated with the appropriate number of crates. Crates do not need any intercommunication.

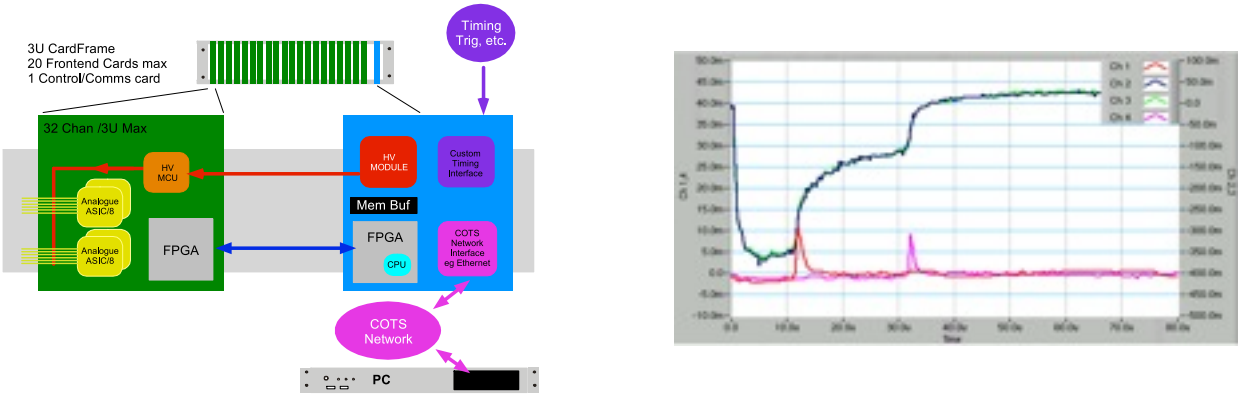

Fig 1. Basic building blocks of SuperNEMO readout in the original proposal (left) and a typical pulse from the Geiger cell.

The baseline plan includes an ASIC to perform the initial amplification and capture of the signals from the detector. A major issue is cost; over a full detector of some 40K channels an ASIC solution offers very substantial savings despite the high initial development costs. Another major concern for us is optimisation of the readout. In NEMO-3 pulses on the anodes and cathodes are discriminated against a simple threshold to give a time. The Geiger propagation is not uniform enough or reliable enough to allow you to infer the 'z' coordinate from a single cathode signal, both rings need to be instrumented. Our detector design presents some major logistical issues in cabling the lower rings, and a solution where connections are only needed to the top of the detector would be very advantageous. This would also reduce the overall amount of cabling (potentially a source of radiation background).

The anode pulse shape extends over the full discharge, and shows features from which the cathode times can be recovered. While technically possible to implement this in a generic way using a FADC and FPGA solution, this would be prohibitively expensive. Previous studies have shown that the rate of change of the anode signal gives useful information on cathode times, and

a simple analog circuit can be developed to exploit this. Early studies on the smaller prototype chambers have shown that simple thresholds on the rate of change gives comparable accuracy to the cathode rings themselves, but this will require a further study.

Revised proposal – Full modular readout

We want to develop an interim readout system that is 100% compatible with the final plans for SuperNEMO, but which does not require a detailed specification of the signals before design, and where we can afford to implement full readout of all channels in this Demonstrator phase. The main revision in the design is that the front end cards are now modular design with 'signal capture' daughtercards. Ultimately these daughtercards will carry the SuperNEMO specific ASICs to provide a low cost, and ideally, single ended readout. In this phase, it has already been decided to cable top and bottom, so simple discriminator readout is adequate. The plan would be to implement FPGA based discriminator readout on daughtercards that could be replaced with ASIC based daughtercard when the ASIC is available. We would use the experience of operation of the Demonstrator itself as the basis for the design of the ASIC, which would be delayed until the next phase.

This very greatly reduces the financial risk associated with a failed ASIC design. The funds allocated to ASIC design and production in this phase would be redirected to cover the increased costs of the modular design, to produce enough readout to fully instrument the Demonstrator. The costings (shown below) are based on the most expensive partitioning of channels into daughtercards and boards. If savings can be made this would allow us to move money back into external engineering effort. We would use this effort to accelerate firmware development – for the reasons detailed above we do not think we will be ready to start ASIC development until we have results from first operation of the Demonstrator.

The analysis of the signals from the Demonstrator will require full digitisation of the analogue signal. Oscilloscope type measurements will be possible at the daughtercard, but to study wider issues (crosstalk etc.) we might need to use commercial FADC systems, such as the CAEN DT5740.

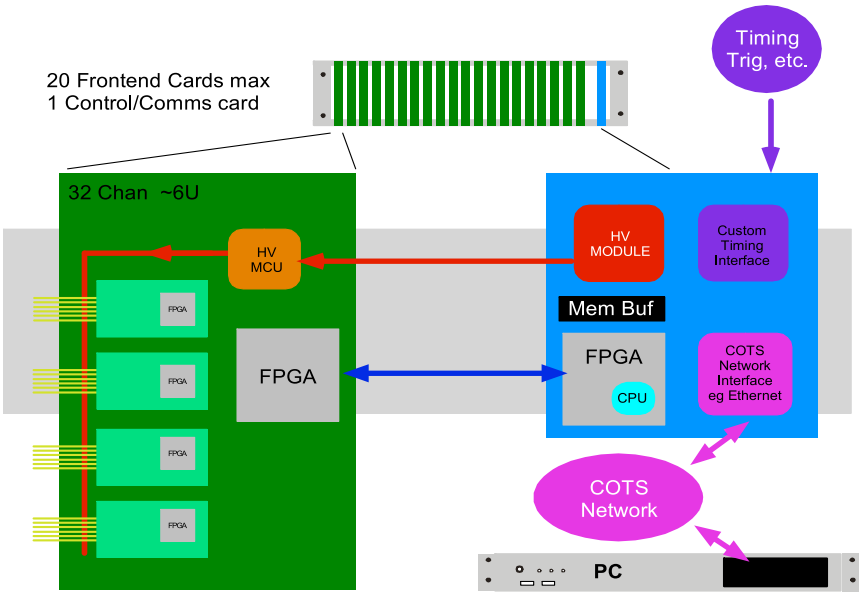

Fig 2. Basic building blocks of SuperNEMO readout in the revised proposal

We propose to defer ASIC design, prototyping and production to the next phase of the project, replacing the ASICs with a discriminator daughtercard. Table 1 below shows the redistribution of funds in this phase, and also has estimates of the funding requirements in the next phase (full production) in both scenarios. As it can be seen from the table the difference in the cost of the full detector readout between the two options is only ~6%.
It is important to note that the cost estimates for the next phase are only rough estimates at this time! Note that the de-scope already forces us to repeat tape-out and mask steps because our pre-series run would be a reduced cost MLM run.

The costing is based on worst case partitioning of the system into daughtercards and boards (more daughtercards, more boards). If better density was achievable the costs would be lower, though this might increase the complexity of the FPGAs. In the event of savings we would return funds to the external engineering effort line, for FPGA firmware work rather than ASIC work, to accelerate the delivery of the readout.

The production schedule of the revised readout for the Demonstrator will not meet the requirements for cell and chamber testing/commissioning at MSSL with cosmic rays. We address this by using the existing Geiger readout system from NEMO-3. We have agreed with the Collaboration that UK can recover all 6000+ channels of the NEMO-3 readout electronics (this is 3 times the number of Demonstrator channels). Although incompatible with the full SuperNEMO readout (which is trigger-less and without deadtime), such a system would be more than adequate for initial tracker commissioning.

Conclusion

The original plan calling for an immediate start to an ASIC design will see only 1/3 of the Demonstrator equipped with the readout which will not allow us to pursue the Demonstrator physics programme on a competitive time scale. In addition it will bear the risk of a failed ASIC design since the final specification of the cell for readout purposes will be available only with the Demonstrator data.
The revised scheme allows us to start work safely, and will allow for full readout of the Demonstrator within our current budget. The financial consequences for the next phase (full production) are only ~6% of the overall budget estimate.

Table 1. Readout equipment costing (in £k)

Item	Original Bid	De-scope	Revised		Next Phase (De-scope)	Next Phase (New)
ASICs	130	70			140	170
MPW/MLM	20	20			-	20
Run	70	30			90(a)	90
(15 + 5 packaing)	20	-			-	-
Custom Fab run	20	20			50	60
Upgrade to buy all chips						
Packaging						
Readout boards	115	58	115		1625	1635
FPGA development (4+)	5	5	5		-	-
Custom connector development	10	10	10		-	-
Prototype run (2 boards)	10	10	10		-	10 (b)
Production run (150)	85	28(c)	85(d)		1600	1600
Test stand and fixtures	5	5	5		25	25
Readout Daughtercards			135			15(b)
FPGA development			5			-
Prototype run (4 boards)			5			10
Production run (600)			120			-
Test stand and fixtures			5			5
Custom Crate	28	28	30		275	275
Metal work for crates	8	8	10(d)		75	75
Power supplies	8	8	8		100	100
Prototype backplane (2)	4	4	4		-	-
Production backplane (10)	8	8	8		100	100
Interface Boards (with HV)	40	40	42		400	400
FPGA Development board	2	2	2		-	-
IP Cores/Licenses	2	2	2		-	-
Prototype run (2 boards)	8	8	8		-	-
Production run (10 boards)	18	18	20(d)		200	200
HV supply (modules & prototyping)	10	10	10		200	200
DAQ Infrastructure (commercial switches, cabling, servers)	15		15		150	150
Timing System (FPGA development board, timing board, real time clock, cabling, testmodules)	10	(French)	(French)			
ASIC Engineering	140	140			30 (a)	140
FPGA Engineering						
Totals	**478**	**336**	**337**		**2620**	**2785**