Data Acquisition Systems for Future Calorimetry at the International Linear Collider

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***Abstract*–A data acquisition system is described which will be used for the next generation of prototype calorimeters for the International Linear Collider and could also be used for the final system. The design is sufficiently generic such that it should have applications elsewhere, be they other ILC detectors or within High Energy Physics in general: e.g. this could be applied to LHC upgrade apparatus. The concept of moving towards a "backplaneless" readout is pursued. A strong under-pinning thread here is to attempt to make use of commercial components and identify any problems with this approach. Therefore the system should be easily upgradeable, both in terms of ease of acquiring new components and competitive prices. The conceptual design, both hardware and software, of the data acquisition system for the ILC calorimeter will be discussed. Results and tests already done will then be shown indicating both the potential and limitations of the approach.**

I. Introduction

The International Linear Collider (ILC) provides new challenges for detector designers. In particular the calorimeter needs to be enhanced to a much higher granularity. Prototypes have been under test for many years, and are reaching the stage where the ILC scale designs are in development.

The CALICE collaboration [1] studies sandwich calorimeters. Tungsten is used as the absorber for the electromagnetic calorimeter (ECAL) and stainless steel for the hadronic calorimeter (HCAL). There are a number of prototype designs, both ECAL and HCAL. Much of this development is shared with an EU funded ILC detector development project (EUDET [2]), which has a goal of a testbeam in 2009.

These detector prototypes are now an order of magnitude larger than previous designs as well as being technically very different to facilitate ILC like operation (this is detailed in the next section). A common DAQ [3] is being developed to readout all CALICE prototypes. As such it is modular – with most of the hardware shared by all detectors. To further take advantage of economies-of-scale the system aims to make use of commercially available components and connections with standard protocols where possible. Any detector specific customisations will be via the firmware loaded into the modules.

The generic functions of these modules does not preclude other ILC detectors (e.g. vertex) or indeed other experiments using this system, so care is being taken to include their requirements (e.g. clock-jitter) where feasible.

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A further goal of the CALICE DAQ project is to use PCs as the off-detector readout system – as opposed to traditional crate based systems. Here the use of serial protocols and bus standards will allow transfer of much of the work done here to a crate based architecture in future projects if desired.

II. ILC Calorimetry

The ILC design specifies both a large tracker and the calorimeter to be inside the magnetic coil to minimize dead material [4]. As the coil is extremely expensive, the calorimeter is forced to be as thin (and as dense) as possible. Fig. 1 shows this geometry.

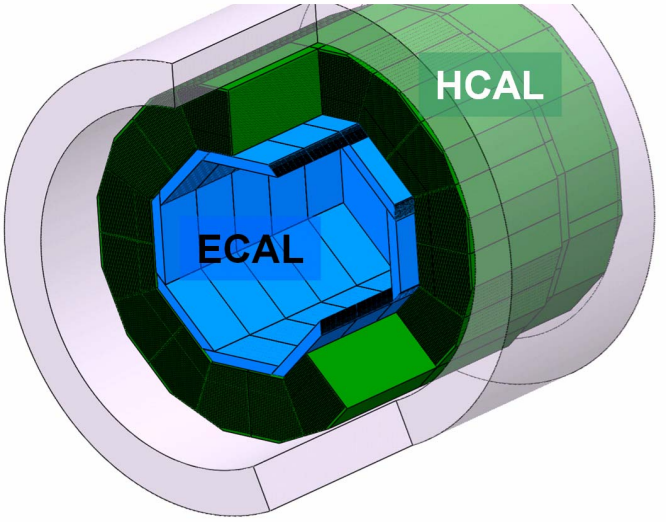

Fig. 1. The geometry of a calorimeter inside an ILC detector

To facilitate this density, high granularity is required (exceeding 100 million channels). The density is achieved by compressing the active sensors into as small a gap as possible. Electronics needs to be close to the sensors to allow high granularity without the huge volume required for signal routing out of the detector. Consequently the electronics is mounted inside the gaps with the sensors.

These calorimeter constraints lead to the following electronics structure: Sensors must be readout by ASICs inside the detector for best function/volume ratio. Control and signal lines are multiplexed to avoid huge routing of wires. Larger components have to be located at the end plates or into cracks.

The ECAL EUDET prototype, known as module-0 demonstrates the ILC concept (shown in fig. 2). A 1.5m long slab with over 100 ASICs has an edge just 180mm wide exposed for power and readout connections.

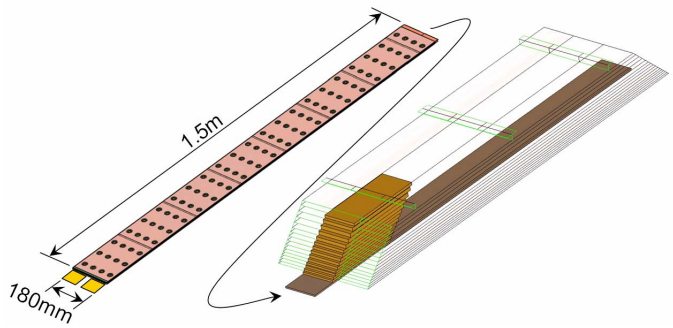

Fig. 2. ECAL slab shown in the context of the EUDET module-0 design.

Having so little room for cooling and so many ASICs inside the detector should prescribe unfeasibly low ASIC power dissipation, but the ILC bunch structure improves the situation. The beam is structured in trains of approximately 1ms filled with bunches every 300ns. This is followed by a gap of 200 ms, during which electronics can be powered-down (so called power-pulsing). This provides a 100 fold reduction in power consumption.

Another ILC feature is the trigger-less readout concept: data is sampled from every bunch-crossing. As the bunch rate is too high for instantaneous data transfer, and on-detector resources too constrained to store all events, an auto-trigger is implemented on the ASICs. Only data over-threshold is stored, tagged with a pad and bunch identifiers. This reduces data output to less-than 5kB per ASIC per bunch-train, which extrapolates to the order of 20MB/s per slab.

III. Data Acquisition System

The DAQ is split between on-detector and counting room (off-detector) components. These are connected using gigabit optical data-links that can span a few hundred metres and provide electrical isolation. It is planned to transfer configuration, clock and control signals onto the detector over these optical links too, but this requires specialised protocols and development, so in addition copper connection is provided in the interim.

On-detector components are located as close to the detector ASICs as possible within the constraints of geometry and cooling.

The system comprises four main components (shown in fig. 3) which ultimately connect to a *detector unit* which hosts the ASICs and sensors. These components are: the detector interface (DIF) that connects the generic DAQ and services to the detector unit; the link/data aggregator (LDA) that connects multiple DIFs to the off-detector data-link; the off-detector receiver (ODR) - a PCI express card hosting the optical interface to LDA. The clock and control system is dealt with in a later section.

For ease of development USB interfaces are provided on the LDA and DIF modules. This allows stand-alone testing of individual components and subsets of the DAQ chain to be used without the full system.

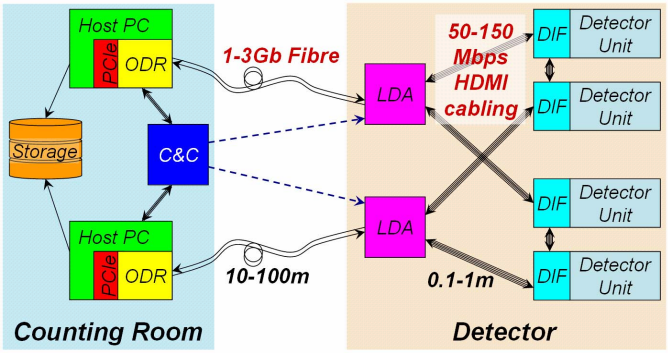

Fig. 3. CALICE DAQ structure, showing the various modules of the system.

Hardware is also provided for low latency signals to be propagated asynchronously to the detector. Although this is certainly not required for the ILC, testbeam and other applications (e.g. cosmic tests) might need this.

A. Detector Interface (DIF)

The DIF straddles the boundary between a specific detector and a generic DAQ. It is physically connected to the detector unit and must match its geometry and connections, provide power and cooling and interface both physically and logically to the ASICs. The logic will be handled by an FPGA.

By defining a common interface, firmware can be written by each detector group to format its' data and controls such that they can integrate with the generic DAQ.

Provision is made on the DIF to connect to a neighbour. This will provide a link to the off-detector for a DIF even if its own connection has failed.

B. DIF-LDA Link

The DIF-LDA link connects the DIF to the rest of the DAQ. It must be small, of sufficient bandwidth and due to the number of links, low cost. The link provides clock, data up and down, fast-controls and a low-latency trigger using HDMI cabling.

HDMI [5] is a home entertainment system standard that defines cables and connectors with 4 shielded twisted pairs and 2 spare conductors in a small (13.9mm by 4.45mm) connector. These cables are commercially available, at low cost and can be sourced halogen-free. They are rated at more than 300Mb/s for data.

The data-link will run at a multiple of the machine clock (expected to be near 50Mbps) with the data encoded in a balanced protocol e.g. 8B/10B.

C. Link/Data Aggregator (LDA)

The LDA is a small FPGA based board tasked with connecting multiple DIFs to the off-detector. It has hardware to fanout clocks, signals and data to the DIFs from the optical (and copper) up-link and aggregates data and monitoring from multiple DIFs, driving the off-detector optical link.

The LDA is positioned on the detector as close to the DIFs as possible for the shortest cable runs where convenient from a and geometry point of view. It is expected that links will be between 30 and 100 centimetres.

The optimal number of DIFs/LDA must take into account the number of available pins on a low-cost FPGA, the bandwidth per DIF and the cost effective maximum bandwidth of the optical link. With the DIF link rated at 50Mbit, 3Gbit optical links becoming standard and the number of usable pins on a small Xilinx Spartan 3 FPGA at around 200, 50 DIFs per LDA is the goal.

Physically the LDA has banks of HDMI connectors for connection to DIFs and a small form-factor pluggable (SFP) connector for the optical link off-detector.

The prototype version of the LDA is built on a commercial development board (*Enterpoint Broaddown2*[i], *Xilinx Spartan3-2000* FPGA), with two purpose specific add-on boards: One providing the SFP and serialiser chipset for the optical link, and the second hosting 10 HDMI connectors with clock fan-out hardware.

D. Off Detector Receiver (ODR)

The ODR is a PCI-Express card hosted in a PC. It collects data from an LDA where it is passed to (or fetched by) the PC and written to disk. The ODR is also responsible for sending data to LDAs and DIFs (and ultimately the ASICs) as well as clock and fast commands. Provision is also made for interfacing with fast-control (clock and synchronous command) sources.

We selected a commercially available development board for this function: the *PLDA XpressFX100*[ii] which is supplied with PCI-Express firmware. The board uses a *Xilinx Virtex4 FX100* FPGA and has 2 SFP gigabit interfaces already fitted, with the capability to add four more via plug-in modules.

The ODR FPGA firmware is responsible for receiving the data, and storing it in the card buffer memory. At present, the data stream is either data generated by the internal data generator (IDG) in firmware, or data received via on-board gigabit Ethernet interface.

The user interface to the ODR card contains two parts: a custom driver - mainly tasked with mapping card memory to the user space and providing direct memory access (DMA) support, and a "requester" program. The requester retrieves data from the ODR card memory and stores it on the local disk. The requester is a fully programmable, multi-threaded application with separate threads for data transfer (DMA) from the ODR to the host memory, and IO threads for storing retrieved events to the local disk. The requester maximises data throughput. The current transfer rate as a function of the ODR data size is shown in fig. 4 for the network, and internal data generator (ING) streams. A Maximum rate of 230 MB/s is achieved with no disk writes (i.e. ODR to memory transfer) and 123 MB/s when data is written to disk. In the case of ING, the upper curve shows transfer rate without data transfer to disk.

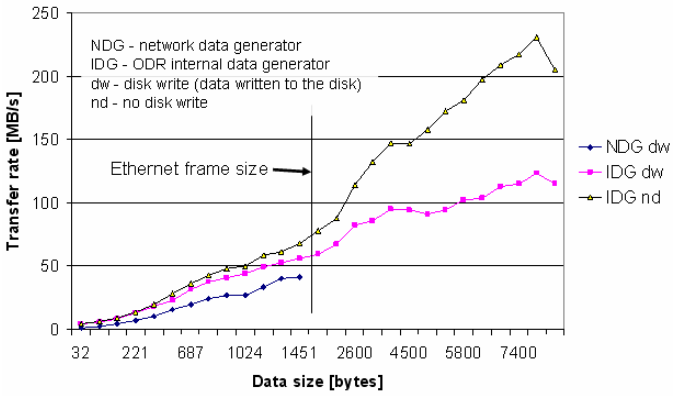

Fig. 4. ODR through-put performance. All measurements with a single requester thread, single IO thread (disk write). Data is written to a disc-array, with Events stored in groups of 10000 events written to the same file.

E. Operation and Software

The DAQ software will be based on an existing system where possible. As the system it triggerless our requirements are closer to those of a slow-control system: after configuration only train-start signals need to be sent to the detector. The ASICs do event selection and the DIF automatically co-ordinates sending of the data.

We are still in the selection phase, having examined EPICS[iii], ACE[iv] and DOOCS[v]. The later is the most likely candidate as is open source, in active development, provides slow and fast controls tools and is already used by ILC community.

IV. Clock and Control

The goal of the project is to deliver clock and control signals using the data distribution system with commercial hardware and protocols. Commercial networking hardware is not suited to this task as it most efficient when it can buffer data and provides no guarantees on delivery times (by design). Similarly networking hardware built into modern FPGAs suffers from varying latency, as do serialisers in some devices.

In this case a custom protocol has advantages and our development will focus on at least fixing the byte-stream latency. This allows a single fibre between uplink the ODR and LDA. Similarly a single copper connection from LDA to DIF would be the best solution. In both cases an auxiliary means of connecting these signals is provided.

The clock and control (C&C) module must interface with the machine and provide stand-alone signal and clock generation. It then distributes these signals the detector, either via the ODR or LDA. It will also receive a busy signal. The HDMI cables configuration used for DIF-LDA link will be re-used here.

[i] http://www.enterpoint.co.uk/moelbryn/broaddown2.html
[ii] http://www.plda.com/prodetail.php?pid=48

[iii] Experimental Physics and Industrial Control System
http://www.aps.anl.gov/epics/
[iv] Adaptive Communication Environment
http://www.cs.wustl.edu/~schmidt/ACE.html
[v] Distributed Object Oriented Control System
http://tesla.desy.de/doocs/doocs.html

The C&C module will be a commercial FPGA board, with USB for communication with run-control, connected to a custom board providing hardware for a good clock, fail-over clock switching, low skew/latency fan-out and signals I/O connectors. The FPGA firmware will provide command encoders, busy filtering and signals enables.

ACKNOWLEDGEMENT

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