Trigger Board Description

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1. Introduction

The Trigger Board will transfer and translate triggers and related signals from external sources into those acceptable by the UK readout system.
Triggers may also be needed by other independent systems and provision is made to supply these.
The external sources and systems mentioned above are not finalised, so the design has focussed on flexibility.

2. Requirements

Construction

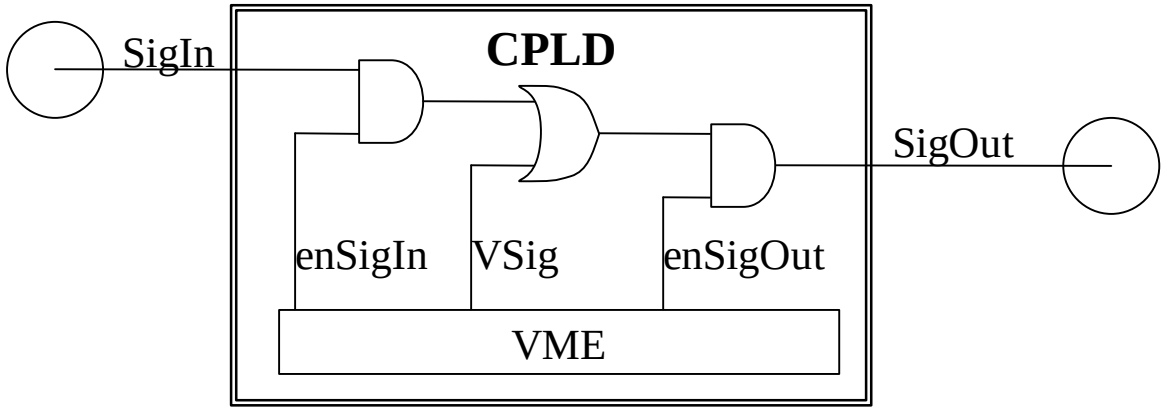
- 6U VME slave
- Generic crate operation
- Interface with the CALICE-UK ReadOut custom back-plane.
- 5V operation, with 3.3V converter-buffers/drivers for the custom back-plane signals.

Operational

- Receives Triggers from external sources.
- Generate a Veto, stopping Trigger acceptance. The Veto is reset by an Abort signal.
- Outputs Trigger to all the ReadOut Boards via J2 backplane bus (low latency).
- Outputs a variably delayed Trigger to external systems.
- Generates stand-alone triggers (via push-button, VME command, internal oscillator).
- Receive Abort signal from VME or external source.
- Receive Clock from an external source.
- Generate stand-alone Clock.
- Provide an Activity input and corrosponding logic/delays to help indicate 'noisy' triggers.
- Accept BeamOn input to allow automatic mode changes if beam is inactive.
- Provide 2 Auxiliary inputs for unforeseen future needs
- Provide VME accessed enables for all input signals
- Provide front-panel outputs of all (PLD modified) signals, with VME enables.
- The unit should be able to operate both as a master or a slave to another Trigger Board.
- Be able to function as a simple front-panel to back-plane interface.

3. Operation

To maintain flexibility, all signals are treated in the same way, with a few extra outputs added. A CPLD will provide both a VME interface, control registers and logic to process triggers. This also provides a means of generating Signals from VME.



Read-out Cycle

- After a trigger is received the Veto signal goes active and no further triggers are accepted.
- The trigger is forwarded to the ReadOut Boards via the backplane.
- The system waits until an Abort is received and the Veto is reset. The Abort will most probably be sent from the DAQ system using VME after read-out is finished.
- In some cases the trigger will be auto-Aborted if the Activity signal is too active around the shaping time of the detector. This time will be configurable.

4. CPLD Information

It is hoped to use a single 5V CPLD on this board (probably a Lattice MACH5-512/256). This will reduce the power supply requirements, and reduce interfacing components.

Signal Group	Pins
Signal Front Panel	33
Signal Backplane	4
VME	101
Debug Connector	8
Delay Units	16
LEDs	5
Total	171