Trigger Board VME Interface

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1. Introduction

With the VME interface we have tried to keep the system as simple, and as generic, as possible for use in the largest variety of crates.
User definable pins on J2 VME connector are used to bus broadcast signals to ReadOut boards on a partially customised backplane.

2. Backplane (non-VME) Signals

LVDS will be used to bus signals from the Trigger Board to the ReadOut Boards

Signal	Spec	No.	Pins	Description
BClkOut	LVDS	1	2	Master clock distribution
BTrigOut	LVDS	1	2	Trigger distribution
BAbortOut	LVDS	1	2	Abort distribution
BAuxOut	LVDS	1	2	Spare
GAIn(4:0)	TTL	5	5	Geographical address input*

3. VME Configuration

A32 and A24 simple VME slave only.
D32 and D16 data transfers supported, but only D(15:0) will contain valid data.
Base-address will be specified by geographical-address pins on the back-plane* or via hex-switches on the PCB for non-customised crates.
A single interrupt will be implemented, but DMA is not needed.
The interface will be located on a PLD, using firmware already written by UCL.

4. Register Map

Offset	Name	Description
0x00	Input Enables	Enables the each front-panel signal
0x02	Output Enables	Enables each front-panel and backplane signal
0x04	Commands	Generates internal equivalents of external signals
0c06	Trigger Modes	Enables special trigger modes (as yet undefined)
0x08	Trigger Delay	Set the delay for the DTrig signal
0x0A	Trigger Window	Configures the enables and window delay-units
0x0C	Status Register	General information
0x0E	Output Test Register	Traps signals on the output path

* See the ReadOut Board VME interface documentation for more information.