TIM (TTC Interface Module) for ATLAS SCT & PIXEL Read Out Electronics

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Abstract

The design, functionality, description of hardware and firmware and preliminary results of the ROD (Read Out Driver) System Tests of the TIM (TTC Interface Module) are described.

The TIM is the standard SCT and PIXEL detector interface module to the ATLAS Level-1 Trigger, using the LHC-standard TTC (Timing, Trigger and Control) system.

TIM was designed and built during 1999 and 2000 and two prototypes have been in use since then (Fig. 1). More modules are being built this year to allow for more tests of the ROD system at different sites around the world.

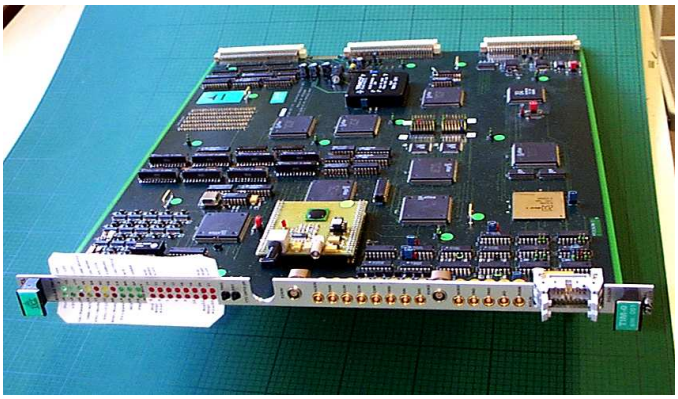

Fig. 1 First TIM-0 module

I. INTRODUCTION

The SCT (or PIXEL) interface with ATLAS Level 1 receives the signals through the Timing, Trigger, and Control (TTC) system [1] and returns the SCT (or PIXEL) Busy signal to the Central Trigger Processor (CTP). It interfaces with the SCT (or PIXEL) off-detector electronics [2], in particular with the Read-Out Driver (ROD), and is known as the SCT (or PIXEL) TTC system .

The SCT (or PIXEL) TTC system consists of the standard TTC system distributing the signals to a custom TTC Interface Module (TIM) in each crate of RODs.

This paper and the accompanying diagrams describe some hardware details of the TIM and their functionality. This paper should be read in conjunction with the original TIM paper presented in 1999 [3] and other specification documents [4], [5] , [6], [7] and [8].

II. TIM

A. Functionality

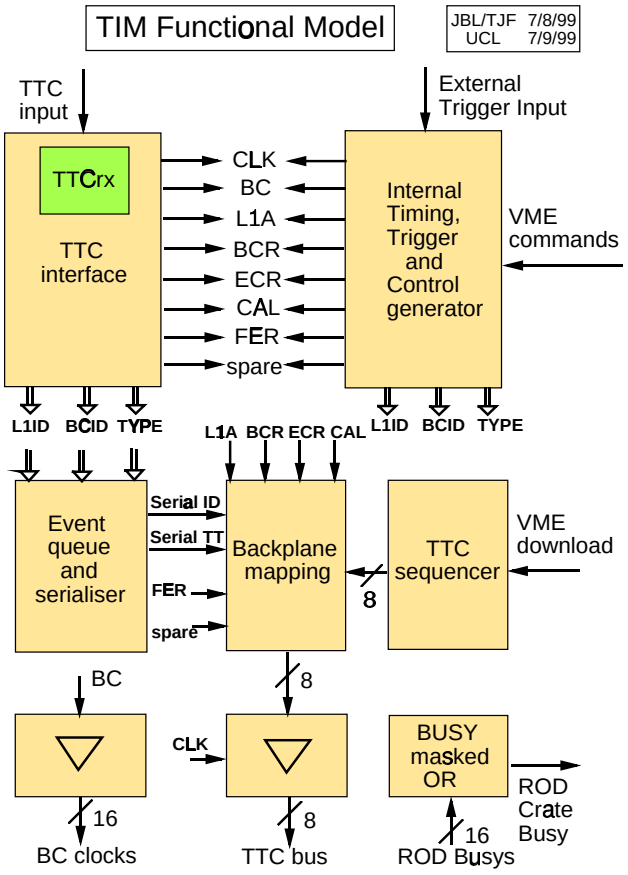

Fig. 2 : TIM Functional Model

The diagram (Fig. 2 above) shows the functional model of the TIM, and illustrates the principal functions of the

current TIM-0 modules :

- To transmit the fast commands and event ID from the TTC system to the RODs with minimum latency. The clock is first transmitted to the Back-Of-Crate optocards (BOC) , from where it is passed to the RODs
- To pass the masked Busy from the RODs to the CTP in order to stop it sending triggers
- To generate and send stand-alone clock, fast commands and event ID to the RODs under control of the local processor

In addition to these main functions, the TIM has also the following capabilities :

- The TIM has programmable timing adjustments and control functions
- The TIM has a VME slave interface to give the local processor read and write access to its registers [9]
- The TIM is configured by the local processor setting up TIM's registers. They can be inspected by the local processor

The TTC information, required by the RODs and by the SCT or PIXEL FE (Front End) electronics, is the following :

Clock :	BC	Bunch Crossing clock
Fast command :	L1A	Level-1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	Calibrate signal
Event ID :	L1ID	24-bit Level-1 trigger number
	BCID	12-bit Bunch Crossing number
	TTID	8-bit Trigger Type (+ 2 spare bits)

The TIM outputs the above information onto the backplane of a ROD crate with the appropriate timing. The event ID is transmitted with a serial protocol and so a FIFO (First In First Out) buffer is required in case of rapid triggers.

An additional FER (Front End Reset) signal, which may be required by the SCT FE electronics, can also be generated, either by the SCT-TTC or by the TIM. At present, it is proposed that FER is carried out by the ECR.

The optical TTC signals are received by a receiver section containing a standard TTCrx receiver chip, which decodes the TTC information into electrical form.

The TIM can also generate all the above information stand-alone at the request of the local processor. It can also be connected to another TIM for stand-alone multi-crate operation for system tests in the absence of TTC signals.

The TIM produces a masked OR of the ROD Busy signals in each crate and outputs the overall crate Busy to a separate BUSY module. A basic ROD BUSYs monitoring is also available on TIM. It may be possible to implement more sophisticated monitoring functionality, on an additional FPGA device on each TIM, if this proves desirable.

B. Hardware Implementation

The TIM has been designed [10] as a 9U, single width, VME64x module, with a standard VME slave interface. A24/D16 or A32/D16 access is selectable, with the base address A16 – A23 (or A16 - A31) being either preset as required, or set by the geographical address of the TIM slot in each ROD crate. Full geographical addressing (GA) and interrupts (eg. for clock failure) are available if required.

On the TIM module, a combination of FastTTL, ECL, PECL and LV BiCMOS devices is used, requiring +5V, +3V3 and -5V2 (or +/- 12V to produce this –5V2) voltage supplies.

The TTC interface is based on the standard TTCrx receiver chip, together with the associated PIN diode and preamplifier developed by the RD12 group at CERN, as described elsewhere [11]. This provides the BC clock and all the signals as listed in section A above. On the TIM modules, the TTCrx mezzanine test board (CERN Ref: ECP 680-1102-630A) [12] is used to allow an easy replacement if required. The latest version utilizes the rad-hard TTCrx3 DMILL BGA144 version of the receiver chip.

The BC clock destined for the BOCs and RODs, with the timing adjusted on the TTCrx, is passed via differential PECL drivers [13] directly onto the point-to-point parallel impedance-matched backplane tracks. These are designed to be of identical length for all the slots in each crate to provide a synchronised timing marker. All the fast commands are also clocked directly, without any local delay, onto the backplane to minimise the TIM latency budget [14].

Most of the logic circuitry required by TIM is contained on a number of CPLDs (Complex Programmable Logic Device), with only the programmable delays and the buffering of the various inputs and outputs being done by separate integrated circuits. This makes TIM very flexible, as it allows for possible changes to the functionality by reconfiguring the firmware of CPLDs, while keeping the inputs and outputs fixed (Fig. 3 below).

This family of devices was chosen during the first design stage of the prototype TIM modules in 1998 because of familiarity with their use and capabilities, thus minimizing the time required for completion of the design. It is proposed to use VHDL to transfer the design to one or more FPGA devices for the final production versions of TIM to reduce costs.

In total, ten of the Lattice (formerly Vantis / AMD) Mach4 and Mach5 devices are used on the TIM-0. A proprietary Vantis / AMD compiler has been used to design the on-chip circuitry and they are all in-circuit programmable and erasable using a Lattice software via a fully-buffered J-TAG interface connected to a PC parallel port. A full, synchronously-clocked simulation of each CPLD circuit can be performed to verify the design, and a limited timing verification is also possible, including a report of all propagation times through the CPLD.

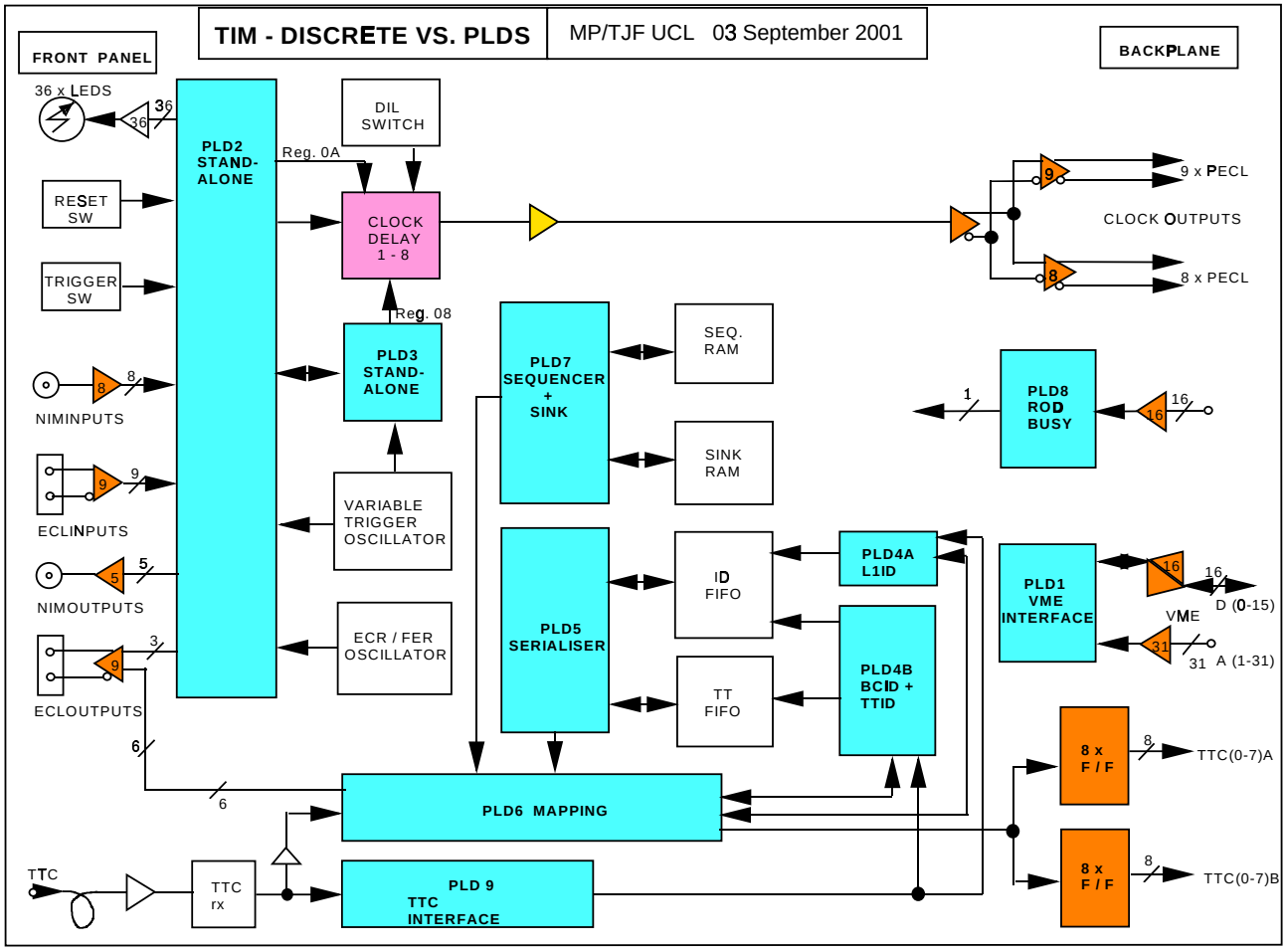

Fig. 3 CPLDs versus Discrete Components

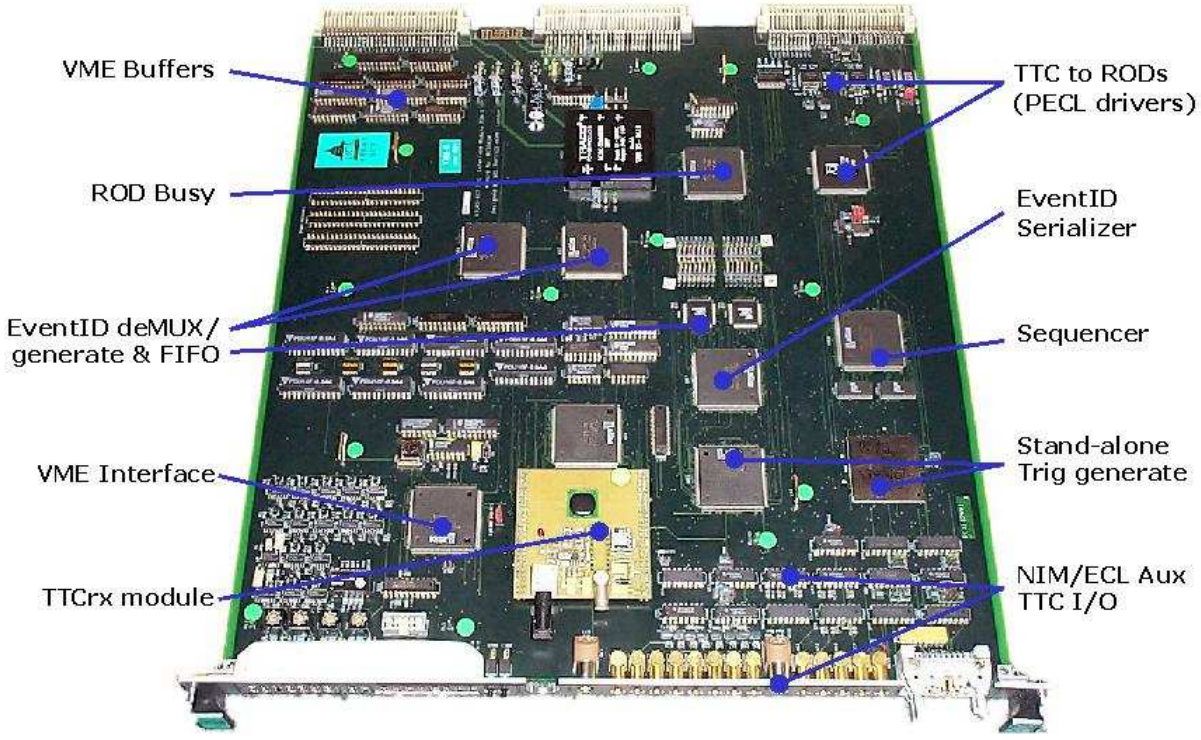

Fig. 4 CPLDs Arrangement on TIM-0

The CPLD devices used on TIM-0 (Fig. 4 above) and their allocation to the individual functional blocks [15] are shown below, together with the percentages of their I/O pins (including 4x8-bit spare buses) and macrocells utilization :

	Main Function	Device	I/O pins	Macrocells
PLD1	VME Interface	M5-384/184-7HC	88	18
PLD2	Stand-alone A	M5-512/256-7AC	59	70
PLD3	Stand-alone B	M5-384/184-7HC	64	38
PLD4a	L1ID	M5-384/184-7HC	61	21
PLD4b	BCID & TTID	M5-384/184-7HC	67	23
PLD5	Serialiser & FiFos	M5-384/184-7HC	79	29
PLD6	Output Mapping	M4-256/128-7YC	88	23
PLD7	Sequencer & Sink	M5-384/184-7HC	85	46
PLD8	ROD Busy	M5-384/184-7HC	57	15
PLD9	TTC Interface	M5-384/184-7HC	84	27

It can be seen that, apart from PLD-2, all devices use less than 50% of their macrocell capacity, and thus are easily reprogrammable. The PLD-2 circuit has been well tested on CLOAC modules [16] and is not likely to require any significant change.

As mentioned before, the TIM uses the TTC information in the "Run" mode, or can operate stand-alone in the "SA" (Stand Alone) mode. Detailed flowcharts [17] show the differences of the sources and of the flow of the fast commands [18] and event ID information between the various CPLDs on TIM, finally producing the same output to the RODs via the backplane.

Another diagram (Fig. 5 below) shows the flow, the distribution and the programmable delays of the clocks in both the "Run" and the "SA" modes.

It is important to note that in the "Run" mode [19] the priority is given to passing the BC clock and commands to the RODs, in their correct timing relationship, with the absolute minimum of delay to reduce the latency.

In the "SA" mode, both the clock and the commands can arrive from a variety of sources [20]. The clock can be either generated on-board using an 80.16 MHz crystal oscillator, or arrive from external sources in either NIM or differential ECL standards. Similarly, the fast commands can be generated on the command of the local processor, or automatically by the TIM under local processor control. The fast commands can also be input from external sources in either NIM or differential ECL [21]. Thus, any of these internally or externally generated commands must be synchronised to whichever clock is being used at the time, to provide the correctly timed outputs.

In addition, a 'sequencer', using 8x32k RAM, is provided to allow long sequences of commands and serial ID data to be written in by the local processor and used for

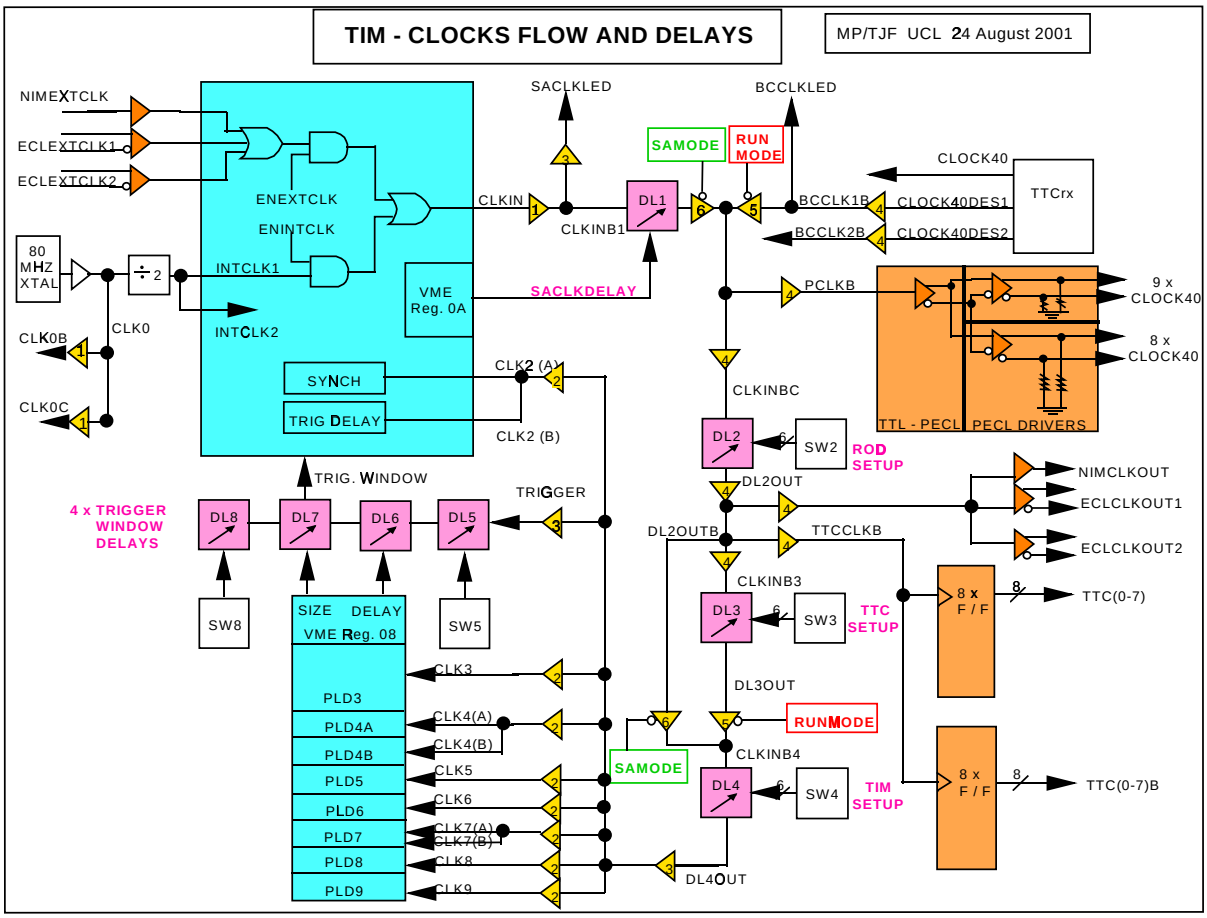

Fig. 5 : Clocks Flow and Delays

testing the FE and off-detector electronics. A 'sink' (receiver RAM) of the same size is also provided to facilitate off-line checking of commands and ID data sent to the RODs [22].

All the backplane signals are also mirrored as differential ECL outputs on the front panel to allow TIM interconnection.

Two prototype TIM-0 modules were designed and manufactured during 1999 - 2000 and have been continuously tested since then, in the stand-alone mode, first at UCL and later also at Cambridge. During May and June 2001, a TIM-0 module was used in the first SCT ROD system test at Cambridge. Meanwhile, the TTC interface has also been tested at UCL using a TTC optical test system incorporating TTCvi and TTCvx modules [1] .

III. SYSTEM TEST

The SCT off-detector electronics is based on 9U-sized modules in a VME64x crate [23]. There will be one TIM, one RCC (Rod Crate Controller) and up to 16 RODs and BOC modules in each ROD crate. Samples of the purpose-designed ROD crates have been manufactured by Wiener. They have been equipped with the custom-designed J3 backplane [24] providing the complex inter-connection between TIM and the RODs and BOCs [25].

The first ROD system test using prototype RCC, ROD, BOC and TIM modules took place in Cambridge in May and June 2001. This demonstrated successfully the feasibility of the whole system design and showed that TIM does correctly source and drive all the timing, trigger and command information to the RODs and BOCs. The timing and signal error rates have also been checked using the stand-alone capabilities of the TIM.

Based on the results of this first system test, two more updated TIM-1 modules have been built and are now starting to be tested at UCL. Together, these four TIM prototype modules will enable further ROD system tests to take place later this year in Cambridge and in USA, to be followed by the first system and beam tests at CERN in 2002. Currently, the design of the final, production version of the TIM is beginning at UCL with the aim of starting the manufacture in the second half of 2002.

IV. ACKNOWLEDGEMENTS

We would like to thank Professor Tegid W. Jones for his continuous support of our work in the ATLAS collaboration. We also wish to thank Janet Fraser who helped to produce the diagrams used in this paper.

V. REFERENCES

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VI. FIGURES

Fig. 1 First TIM-0 Module :
http://www.hep.ucl.ac.uk/~mp/TIM-0_photo-4.jpg
Fig. 2 TIM Functional Model :
http://www.hep.ucl.ac.uk/~mp/TIM_Functional_model.eps.gz
Fig. 3 CPLDs versus Discrete Components :
http://www.hep.ucl.ac.uk/atlas/sct/tim/TIM_PLDs-vs-ICs.pdf
Fig. 4 CPLDs Arrangement on TIM-0 :
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Fig. 5 Clocks Flow and Delays :
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