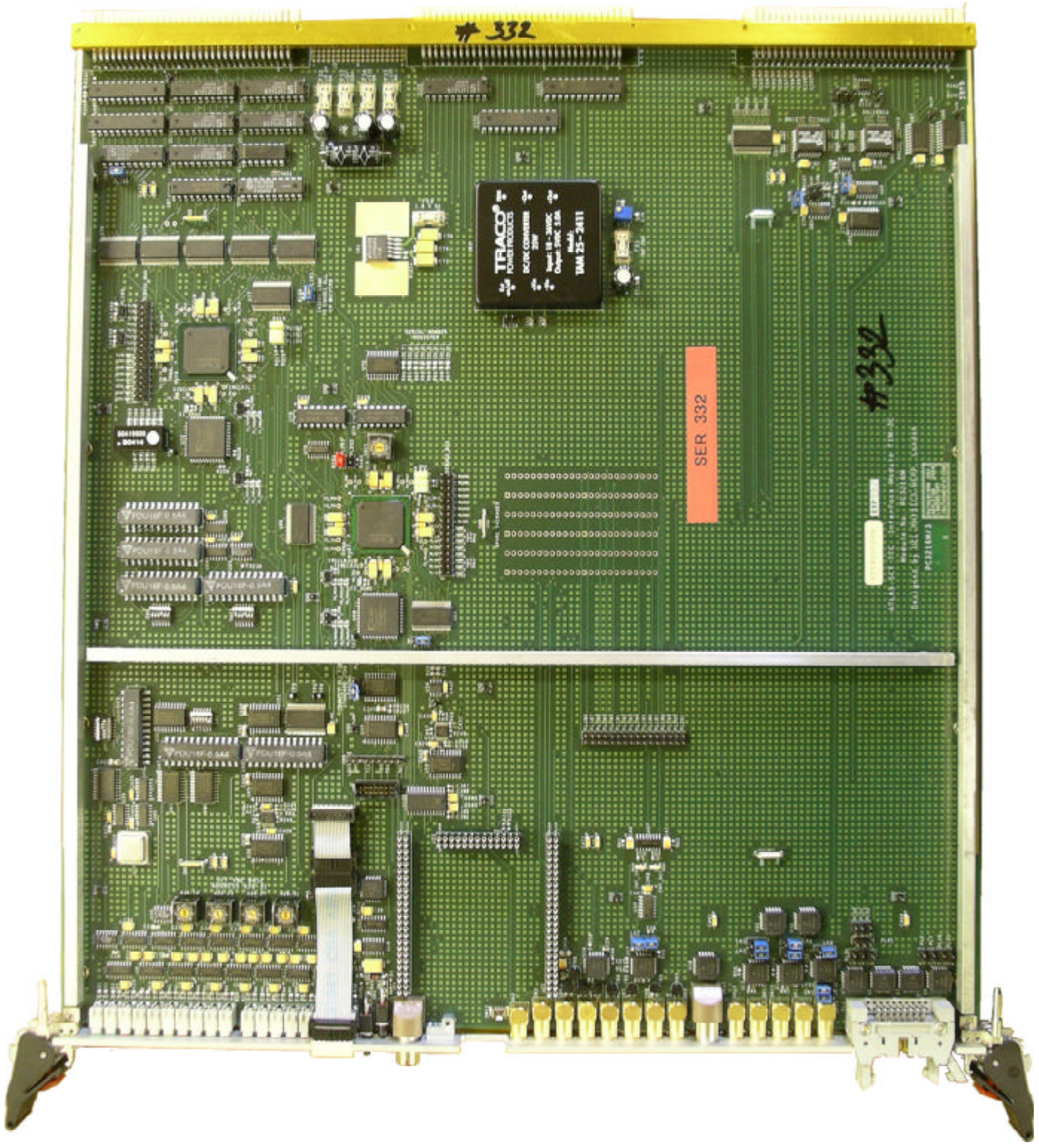
TIM-3C Setup Photos

Accompanies Physical Setup Document

(http://www.hep.ucl.ac.uk/atlas/sct/tim/rel/tim3C/TIM-3C_Setup.txt)



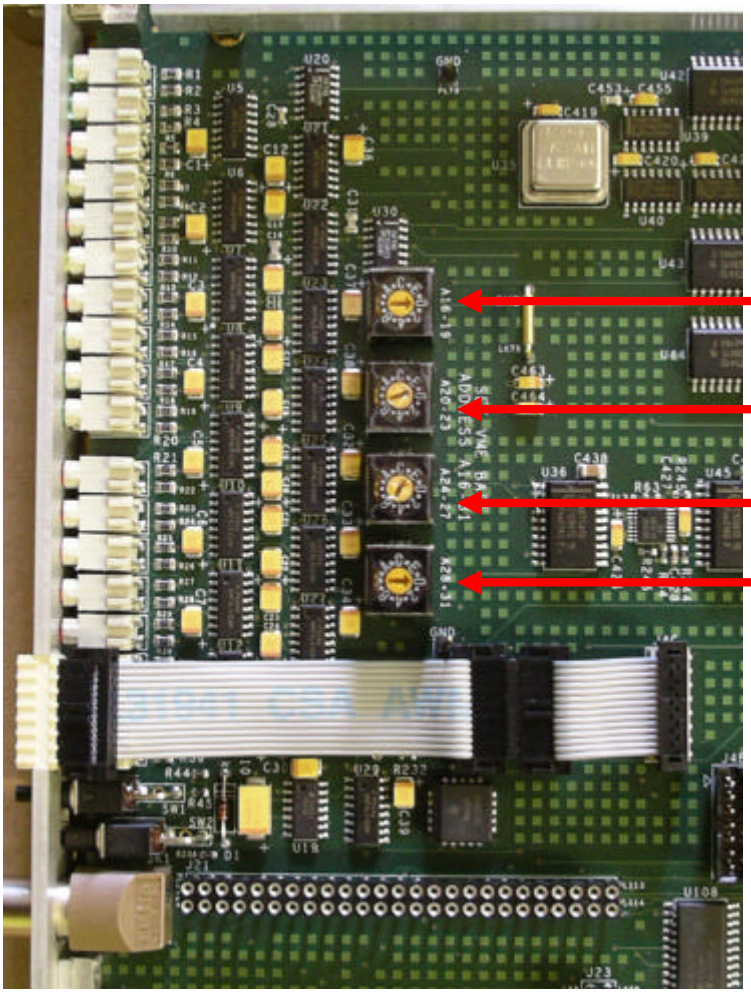


Photo 1

- Base Address Switches
- JTAG Extension Cable

Photo 2

- Timing Setup DIP switches

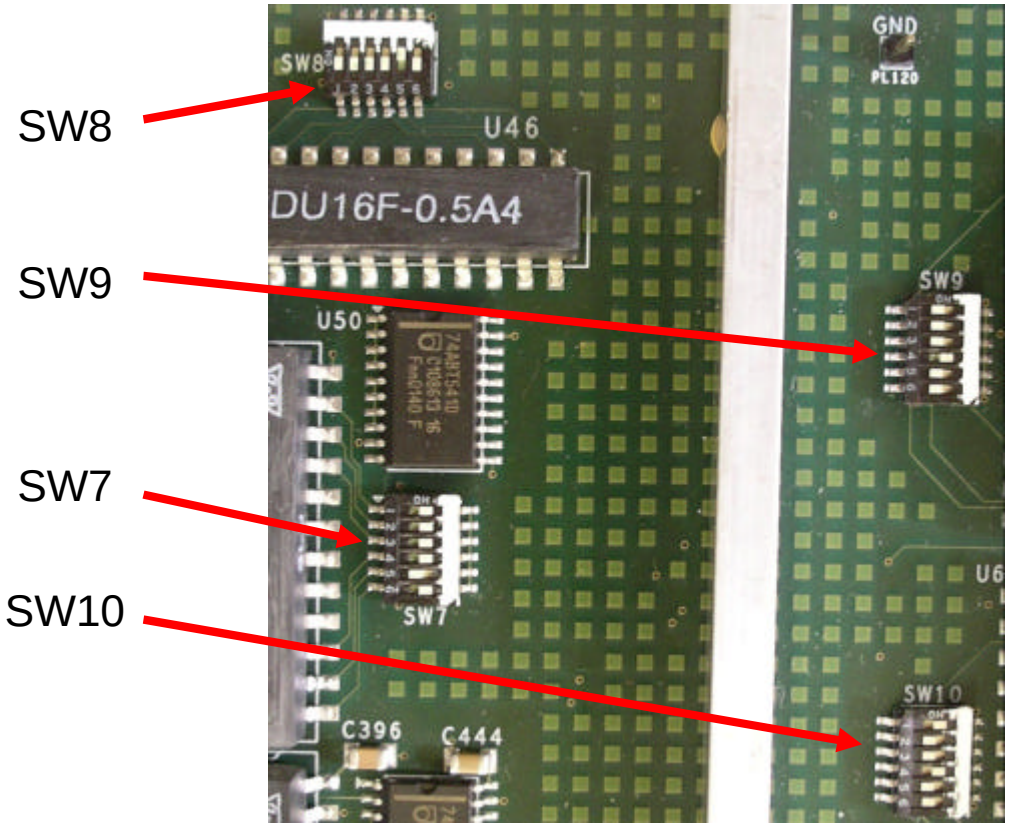


Photo 3

- VME IACK bypass
- FPGA Boot Mode
- LV Buffer Enable

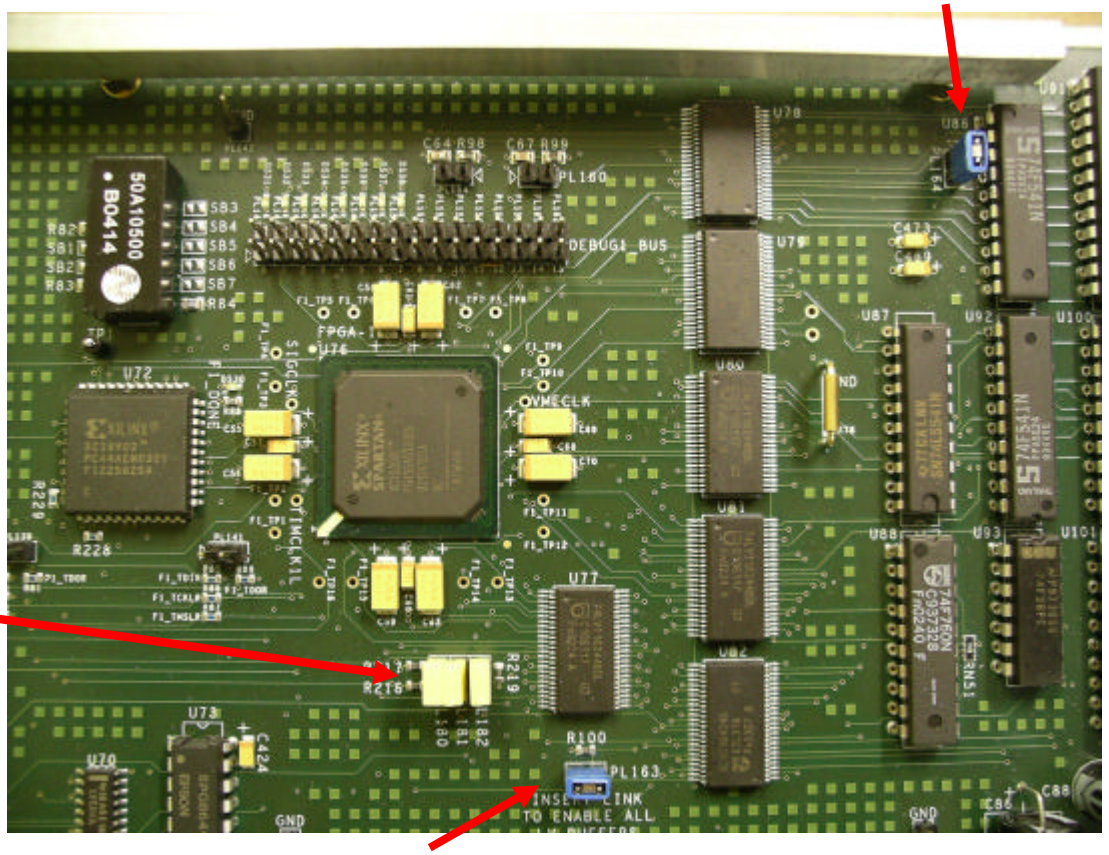


Photo 4

- Enable Clock/ Signals Backplane Drivers
- Enable TIM-OK Driver

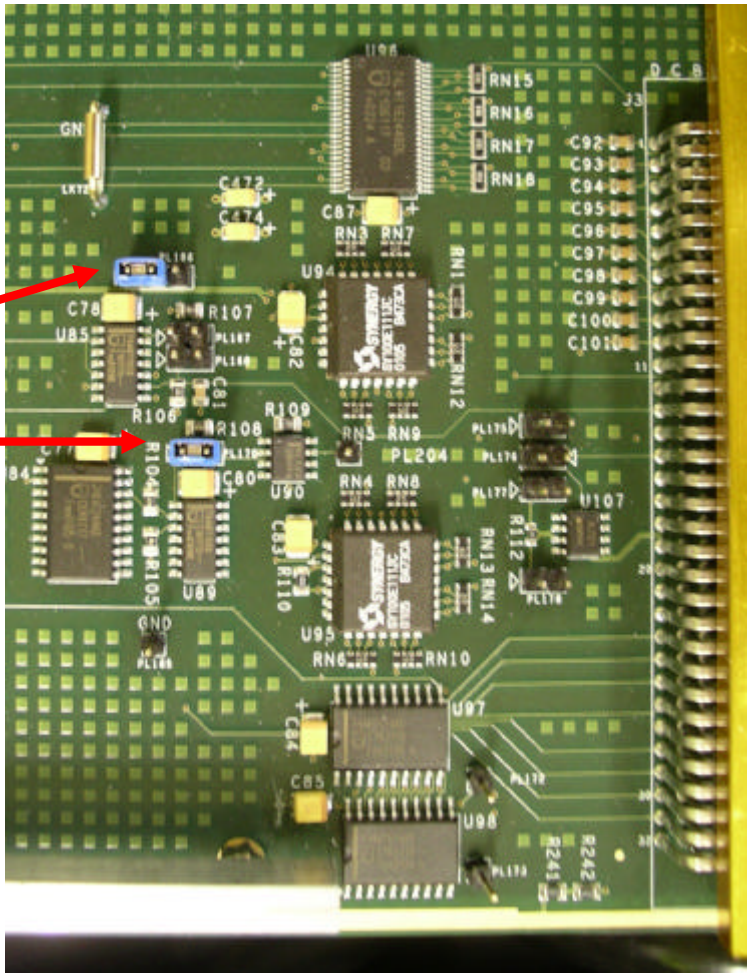


Photo 5

- Front panel I/O polarity/ configuration

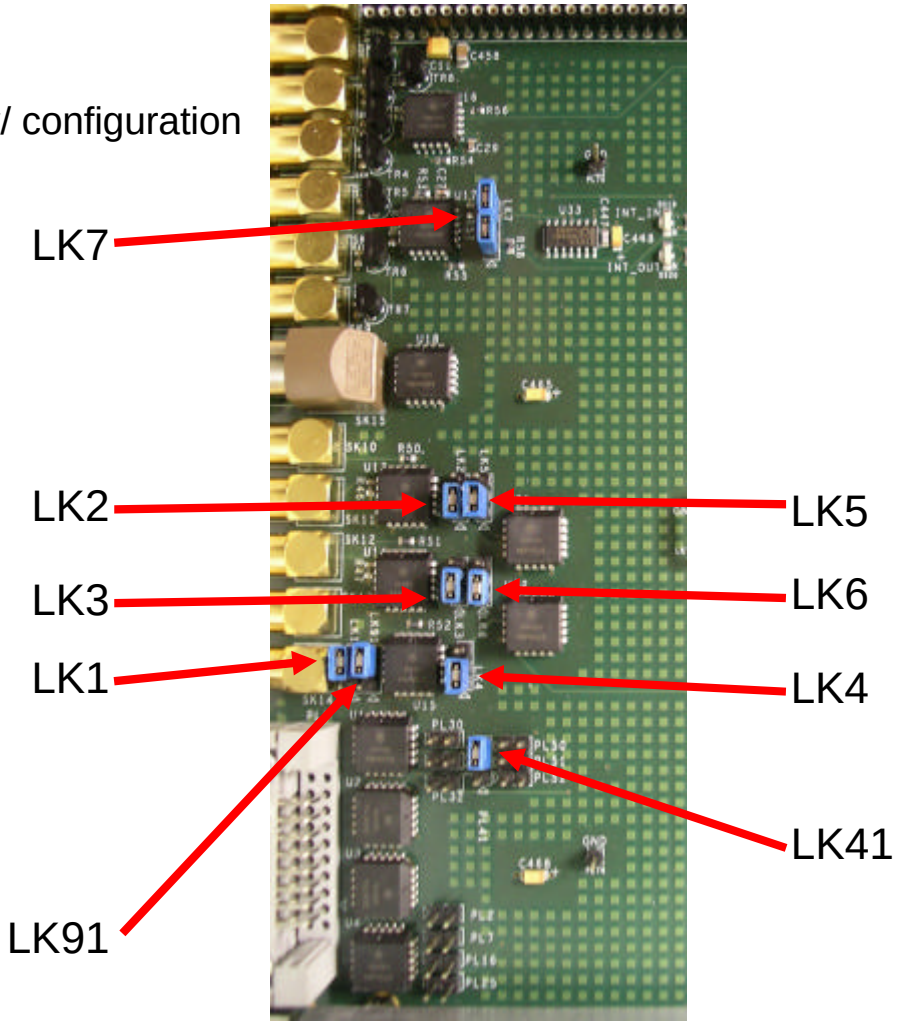


Photo 6

- VME JTAG re-prog enable
- FER source select
- Fixed Frequency Veto disable
- FPGA-2 boot mode

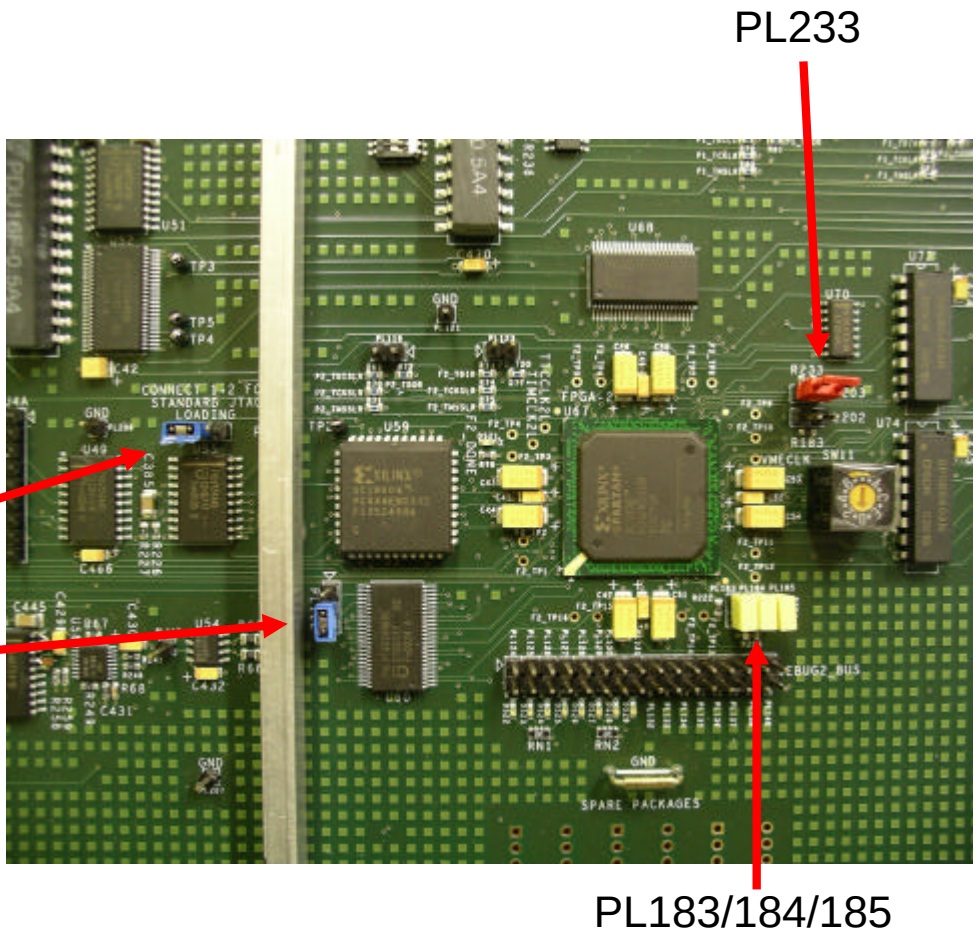


Photo 7

- Hardware ID

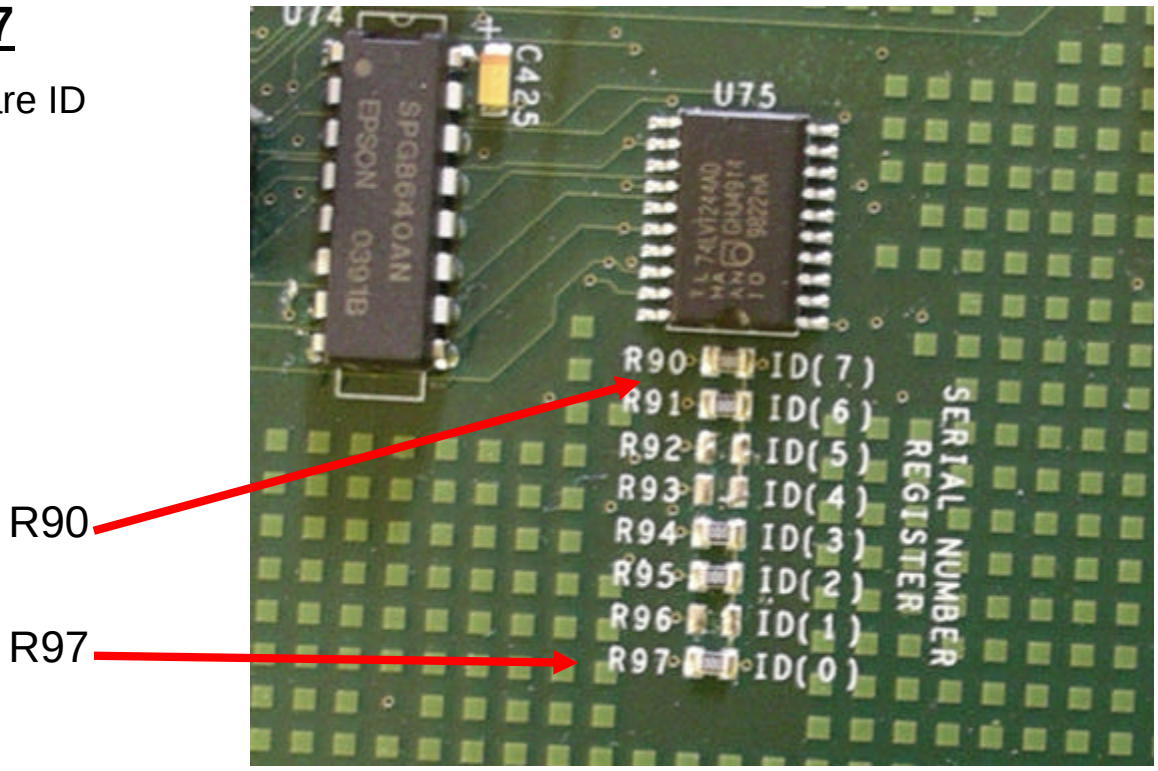
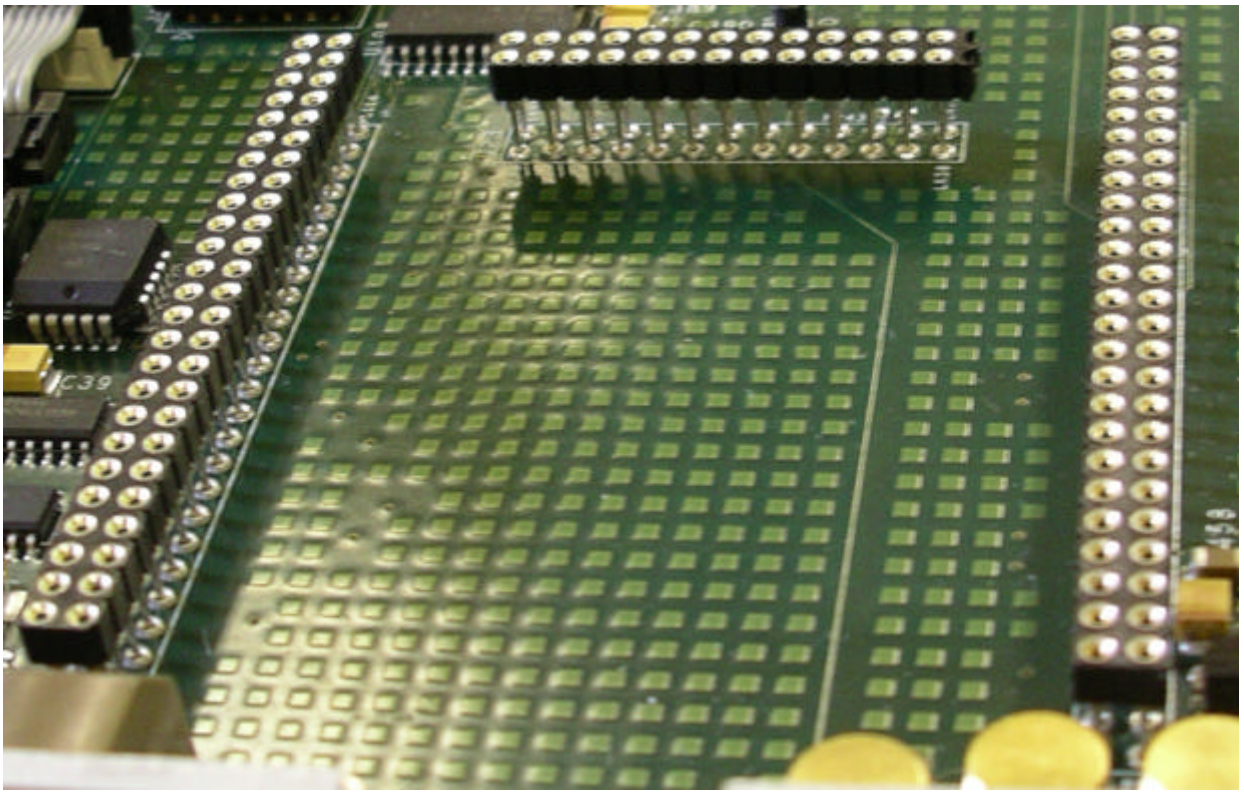


Photo 8

- TTCrq connectors



- JTAG Extension Cable

Photo 9

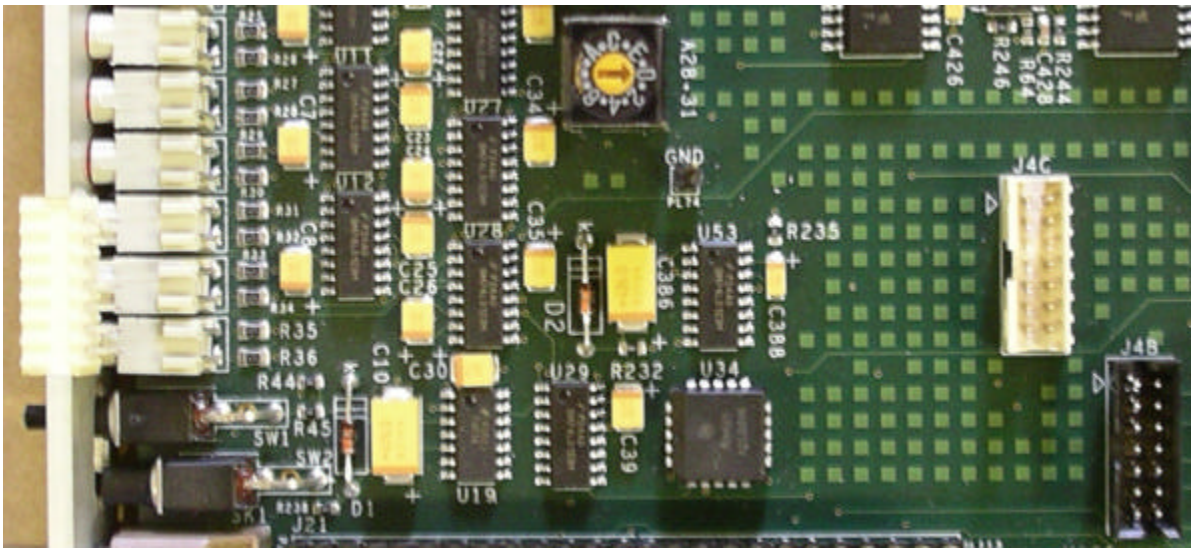


Photo 10

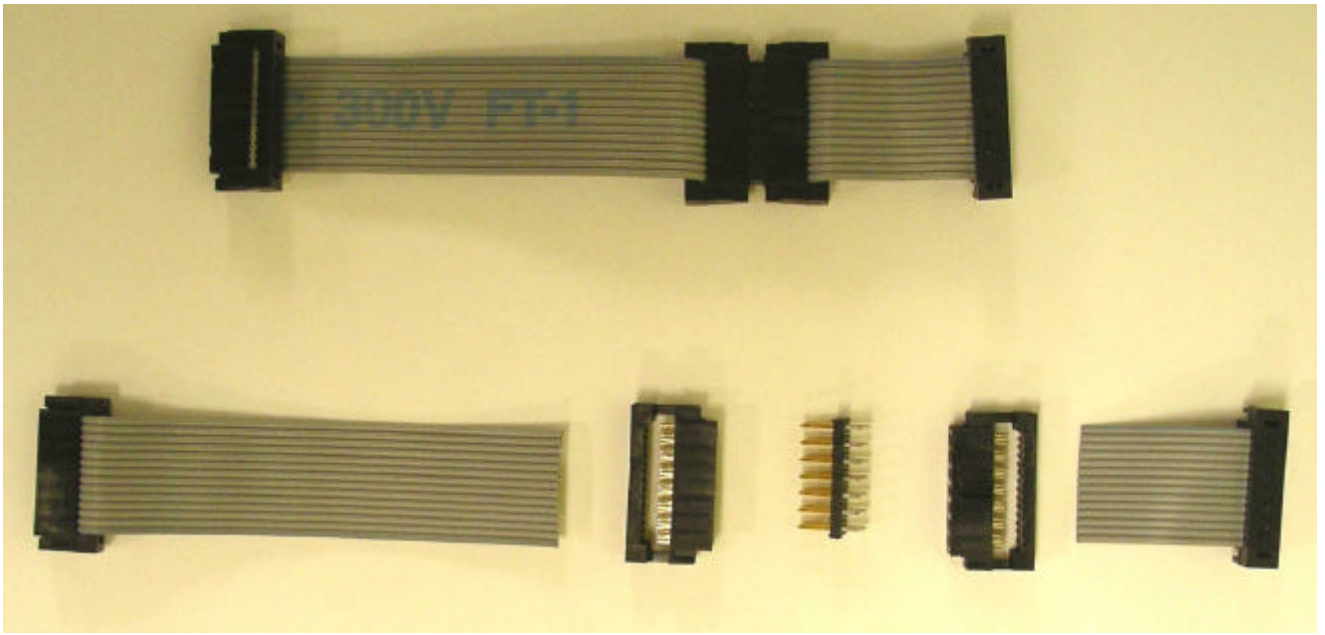


Photo 11

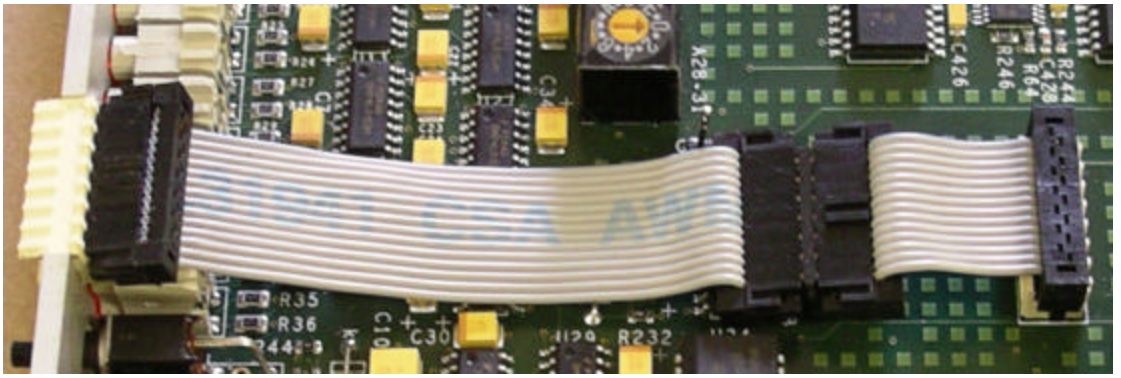


Photo 12

- Stiffening Bars

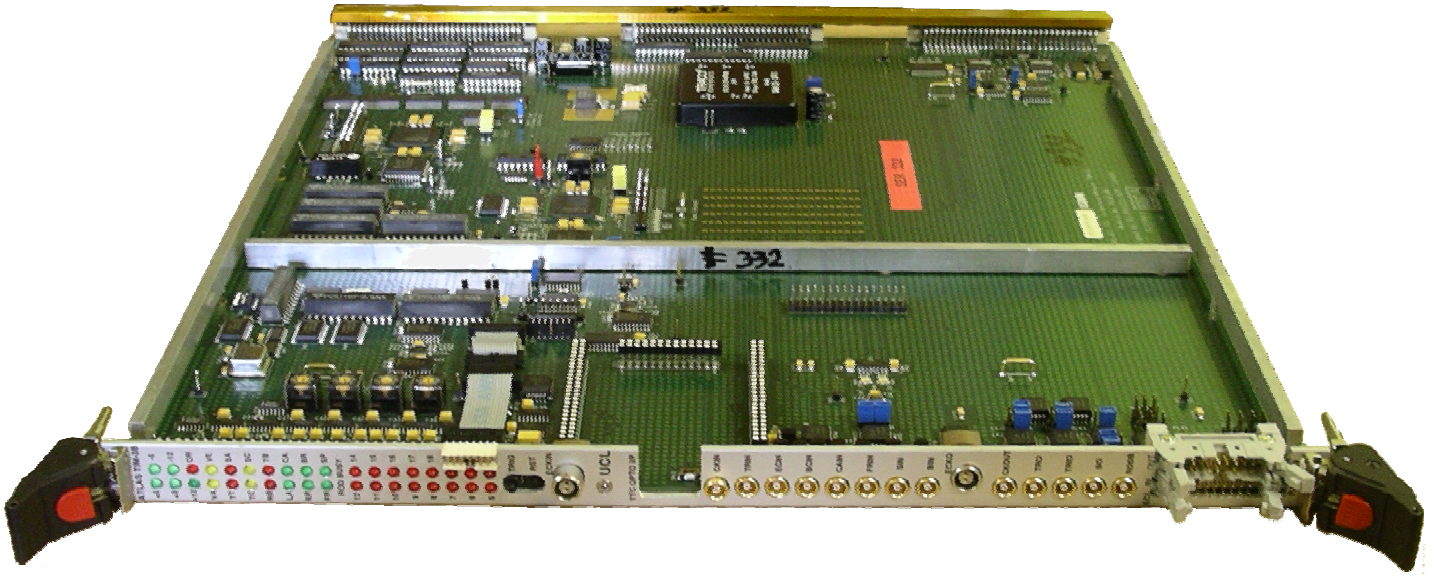


Photo 13

- 5mm spacers for ventilation

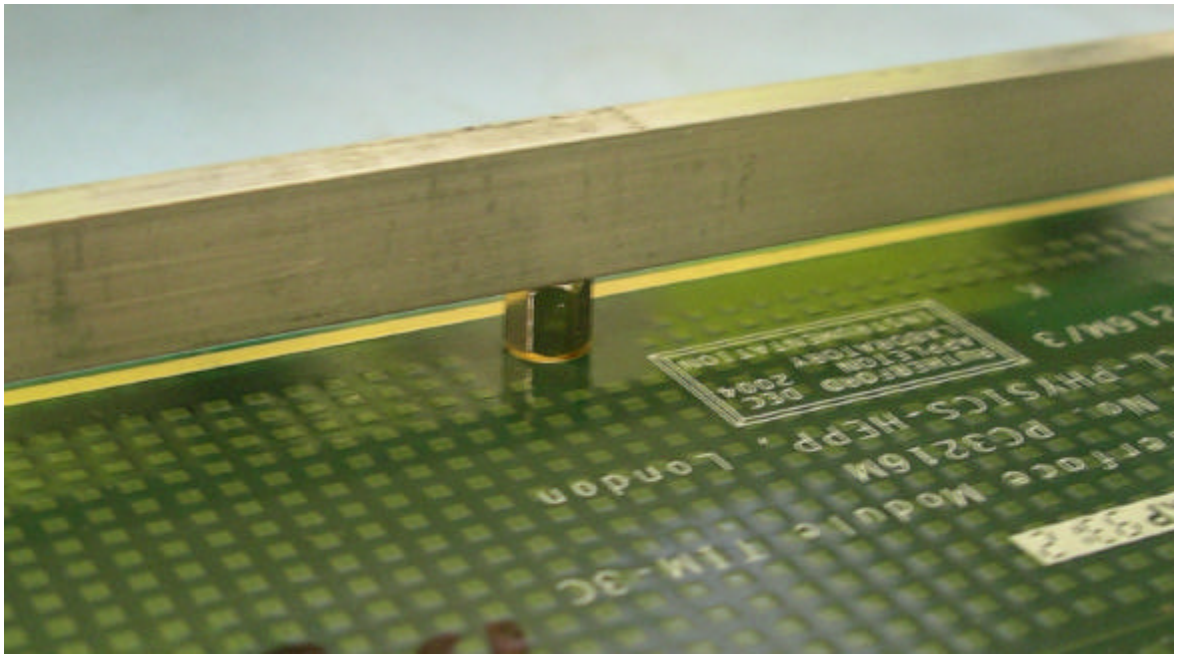


Photo 14

- Extra stiffening bar across J1/J2/J3