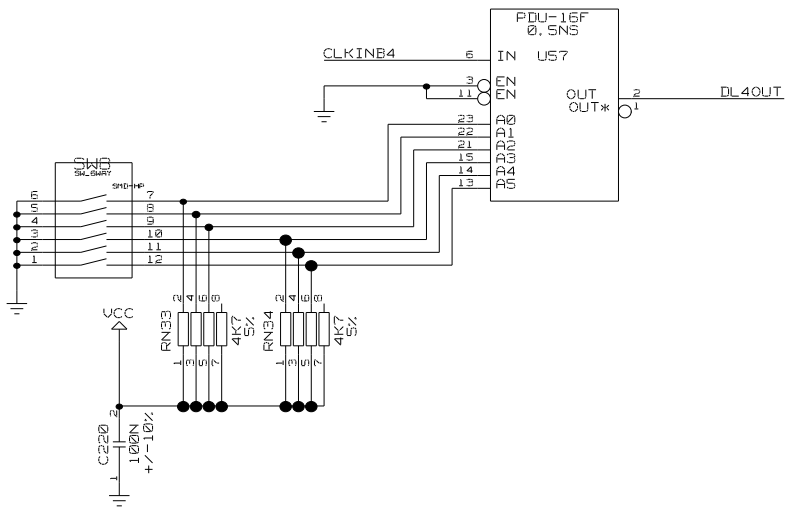
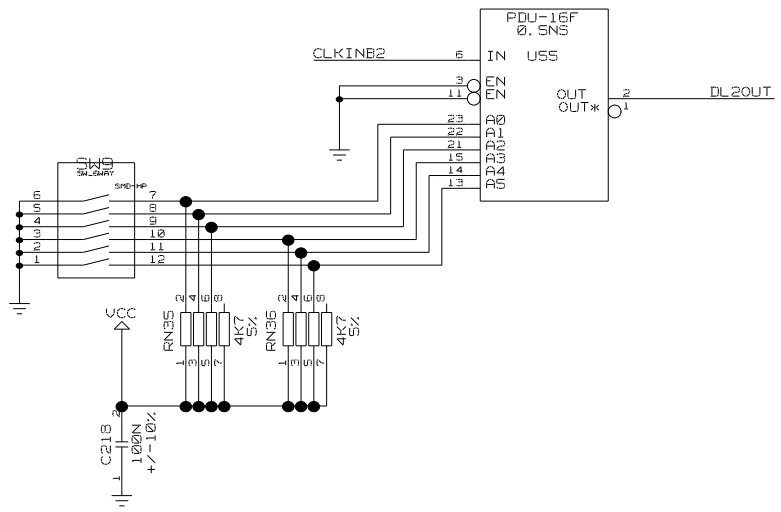
A	2-TE-0102-023-08-B	THIS DRAWING CONFORMS TO B.S. 3939

DL4 - TIM SETUP DELAY



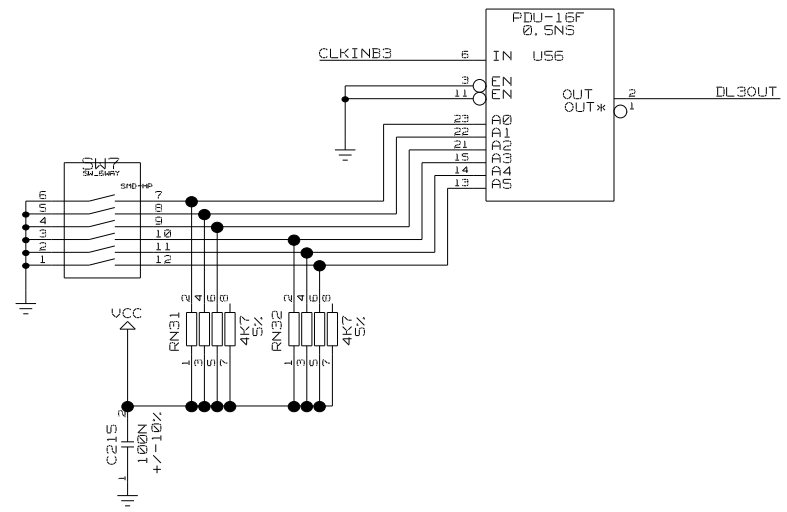
DELAY 9-41USEC IN STEPS OF 0.5USEC

DL2 - ROD SETUP DELAY FOR TTC OUTPUTS



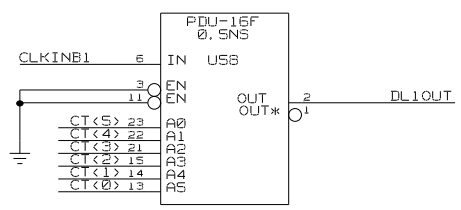
DELAY 9-41USEC IN STEPS OF 0.5USEC

DL3 - BCCLK1 SETUP DELAY



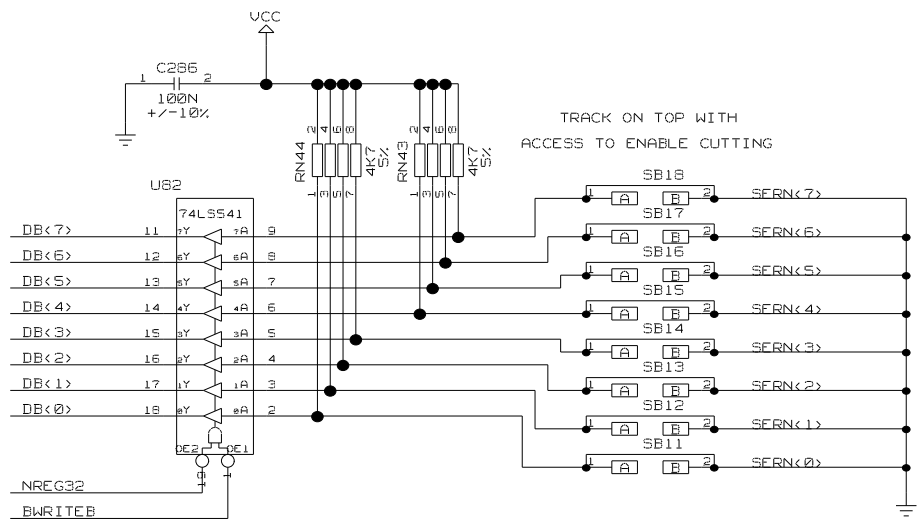
DELAY 9-41USEC IN STEPS OF 0.5USEC

DL1 - SACLK DELAY

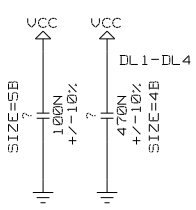


DELAY 9-41USEC IN STEPS OF 0.5USEC

SERIAL NUMBER REGISTER



DECOUPLING



PROVISIONAL

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
B	17-05-2001	TE198	D. J. BECKETT	M. POSTRANECKY	M. POSTRANECKY	
A	14-12-1999	- - - -	D. J. BECKETT	M. POSTRANECKY	M. POSTRANECKY	

USED ON ATLAS SCT

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CCLRC COUNCIL FOR THE CENTRAL LABORATORY OF THE RESEARCH COUNCILS
RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3162M CIRCUIT

TTC INTERFACE MODULE (TIM-1) 02-01

A 2-TE-0102-023-08-B

TOTAL NO. OF SHEETS 17

A 2-TE-0102-023-08-B