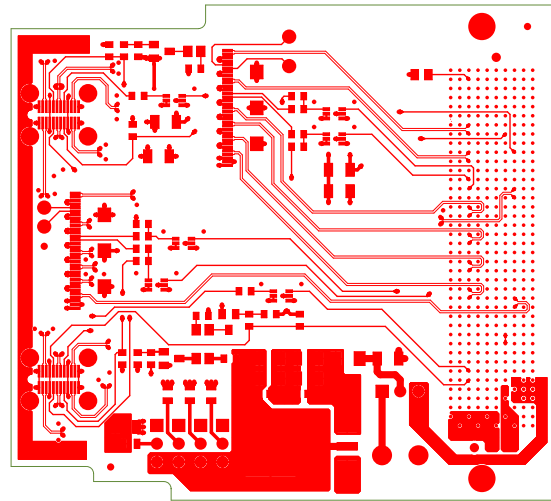
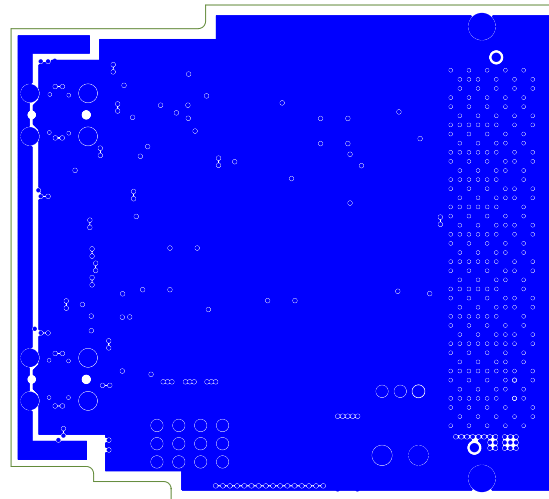


PAGE	CONTENT
2	TOP
3	GND
4	LAYER3
5	LAYER4
6	PWR
7	BOTTOM
8	ASSY_BOT
9	ASSY_TOP
10	BOT_SILK
11	TOP_SILK
12	BOT_PASTE
13	TOP_PASTE
14	BOT_MASK
15	TOP_MASK
16	FAB_DWG




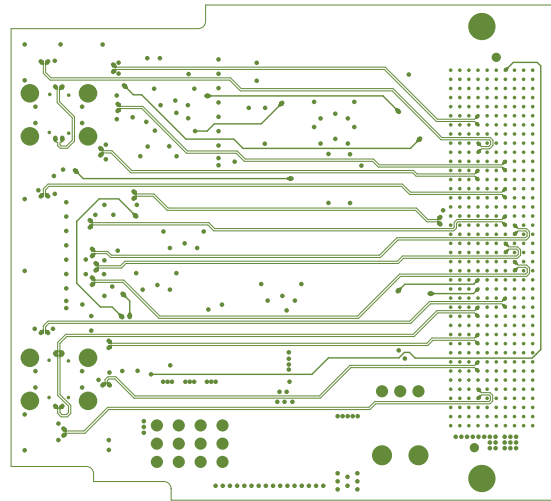
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APPROVED				
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	SIZE	TYPE	DWG.NO.	REV.
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1	



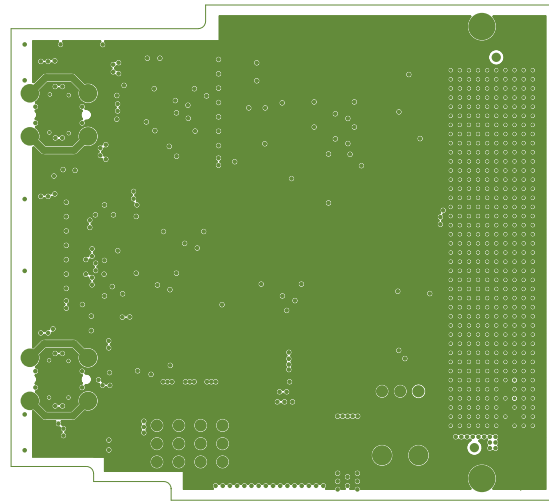
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		COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA						SHEET 1 OF 1	




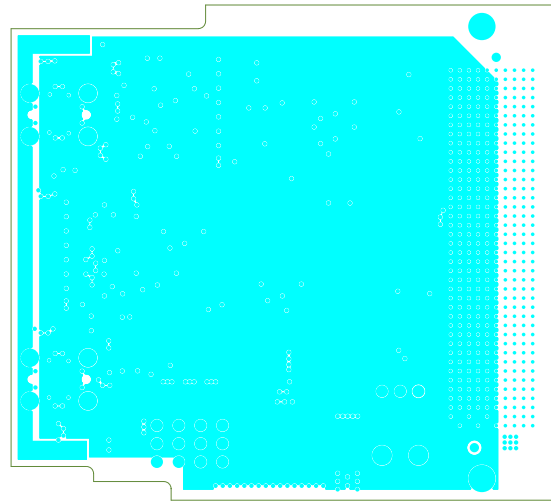
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1	




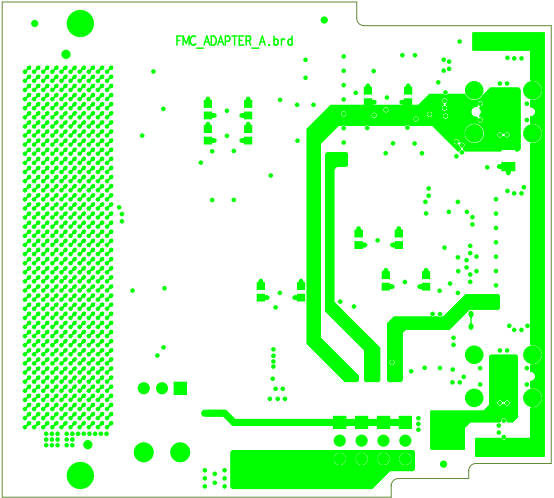
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1		




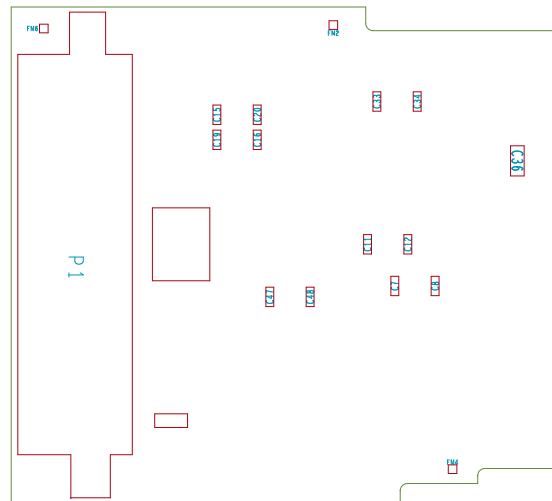
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1		




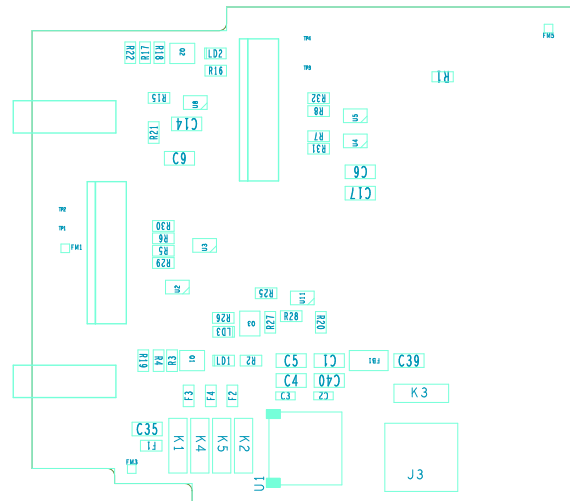
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1		




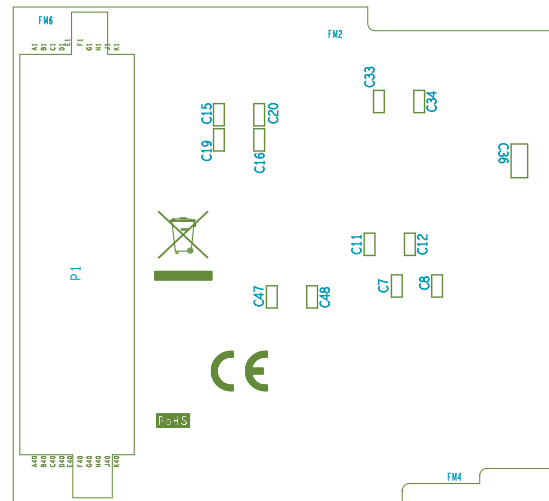
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CONTROL SYSTEM LABORATORY		DWG.NO.	REV. A
COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1




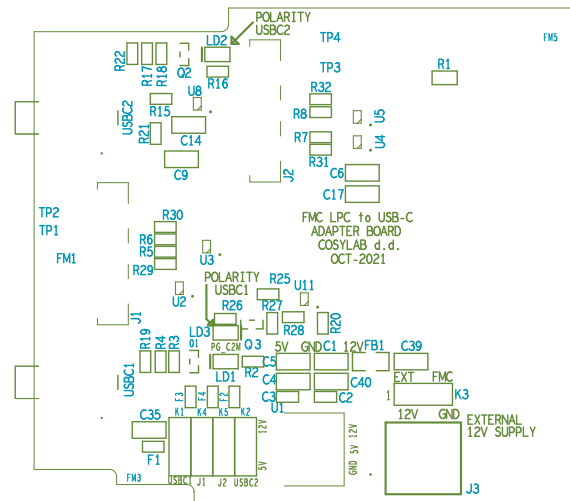
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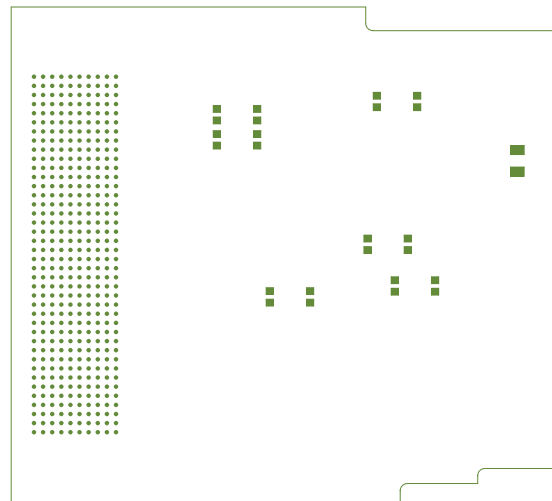
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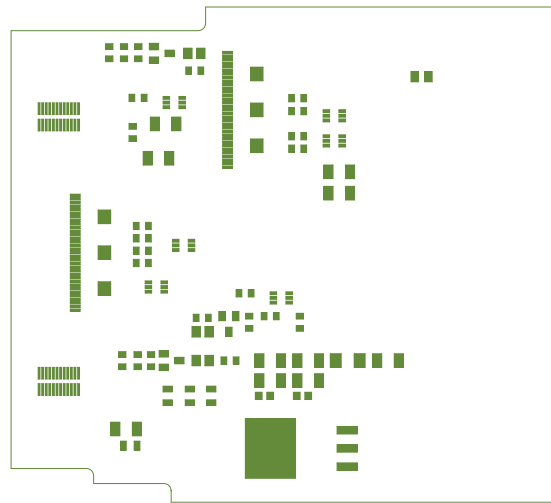
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		COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA						SHEET	1 OF 1



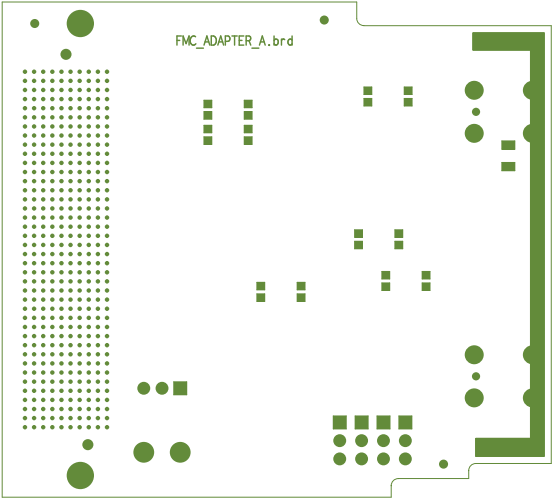
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A4	FAB		A
COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1




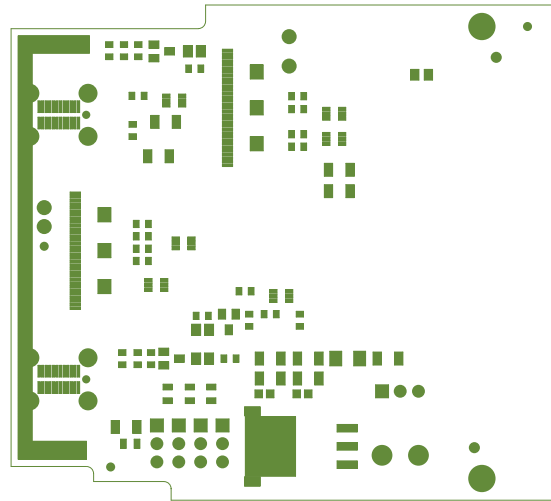
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	COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA		REV. A
			SHEET 1 OF 1



MASK_BOTTOM

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		TITLE FMC to USB-C and FPC adapter board	
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COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA			SHEET 1 OF 1

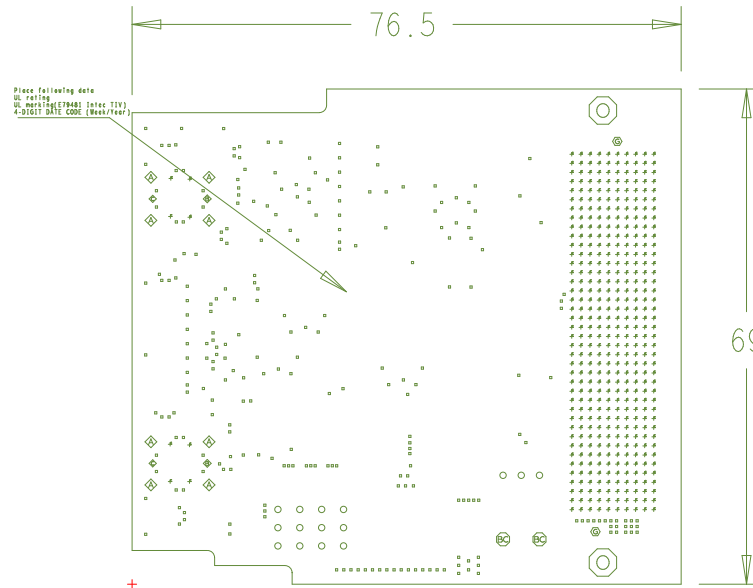


MASK_TOP

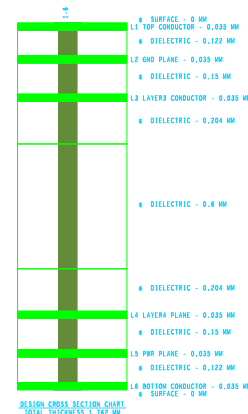
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	A4	FAB		A
	COSYLAB D.D. GERBICEVA ULICA 64 LJUBLJANA		SHEET 1 OF 1	

STANDARD FAB NOTE

- 1 Fabricate conform to the requirements of IPC-A-600, IPC-6011 and IPC-6013, CLASS 2, Type 3 unless otherwise specified.
- 2 Database units are in MM
- 3 Material:
A) Laminate: R-1755M Prepreg: 2116 TG-150
Color: Green, B-staged prepreg
B) Internal layers copper thickness: 35um copper
C) External layers copper thickness: 18um copper
D) See detail "A" for layer stack-up, laminates and Finished thickness details.
- 4 Drilling:
A) Drill size tolerance refer to chart
B) Hole locations not to exceed 0.076mm from true position.
C) See drill table for hole size and plating requirements.
- 5 Plating:
A) Minimum plating thickness in holes = 25um
B) Minimum total copper thickness on external layers after plating = 35um (copper)
- 6 Etching:
A) Layer to layer mis-registration not to exceed 75um from true position.
B) Etched pattern to be with +/- 25um of film pattern.
C) If Controlled Impedance is required, there will be a separate Controlled Impedance Table attached in this drawing. Controlled impedance nets have been routed using track widths listed. PCB supplier can change these parameters to meet his fabrication methods on the conditions the finish impedance is the same as that specified in the table.
- 7 Soldermask:
A) Soldermask to be liquid photoimageable (LPI), color green, over bare copper (SMOBC) on both sides. IPC SM-840, type B, Class 2.
B) Soldermask is not permitted in components holes or on components pads. Soldermask should withstand a minimum of 500 VDC of breakdown voltage.
C) No solder pick up/wicking during wave solder.
D) Meets a minimum insulation resistance of 500 mega ohms.
E) The thickness shall be a minimum of 10um, maximum of 63.5um (25um nominal)
- 8 Finish:
A) Exposed copper to be finished in ENIG Chemical Gold
B) Finished surface to be free of bubbles, blisters, and solder.
- 9 Silkscreen:
A) Apply White silkscreen to both side of the PCB clip silkscreen from any exposed copper and unplated holes.
B) Fine screen required.
C) Ink is not permitted in components holes or on component pads.
D) Mark Fab Dwg Revision inside the box as indicated by the arrow.
E) Vendor Name/Code, UL rating, PCB date code must be marked on the board.
F) Maximum camber allowed is 0.01 mm/mm
- 10 Bare board electrical test required. When space allowed, test stamp should be placed on the PCB to indicate the board has passed electrical testing. Preferred method: Supplied netlist data (*.PC).
- 11 Alternative method: Netlist generated from Gerber data. Unless otherwise specified, dimensions, tolerance and surface finish apply after plating or chemical film treatments and prior to organic coatings. For a list of drill data files refer to the fabrication of this PCB, refer to the file 1.TXT OR see Film set list on the drawing.
- 12 Teardrops allowed on outer layers on pad entry of traces less than or equal to 0.15mm.
- 13 Teardrops allowed on inner layers
- 14 Remove unused pads on inner layers
- 15 Finished board must be RoHS compliant and be able to withstand Pb-Free soldering process.
- 16
- 17



FABRICATION_INFO



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	FINISHED_SIZE	PLATED	QTY
.	0.254	PLATED	408
.	0.3	PLATED	256
o	0.8999	PLATED	15
⊗	1.3	PLATED	2
◆	1.65	PLATED	8
⊙	2.6924	PLATED	2
◆	1.0	NON-PLATED	2
◆	1.1	NON-PLATED	2
⊙	1.2954	NON-PLATED	2

DRAWN	MARKO LEVICNIK	13.10.2021								
CHECKED										
APPROVED										
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