A combination of a general purpose MTCA.4 AMC board and a compatible Rear Transition Module make up the hardware for the Clock and Control (CC) system for the European Free Electron Laser (EuXFEL) megapixel detectors. The AMC board is the DESY designed DAMC2, which has a Xilinx V5LX50T FPGA to provide processing power. The RTM is a custom designed PCB that provides the connectivity to the Front End Electronics (FEE) units at the detector end.

The CC system is responsible for the synchronisation of the detectors and the DAQ system to the general EuXFEL timing. The EuXFEL facility will generate coherent and intense X-ray flashes with a ~4.5 MHz bunch frequency. The Timing Receiver (TR) board housed in the same crate as the CC system delivers the bunch clock to the CC through the MTCA.4 backplane.

The CC system sends a data packet (FAST data) synchronously to the 99 MHz clock. The FPGA firmware for the CC system is built around a busregister structure called the II Bus, whose registers are accessed through either the PCIe link to the crate processor or the blocks attached to the bus. The EuXFEL central software system controls the CC system through the PCIe link. The FAST TX module generates the messages to the FEE units. Additional test modules can be used to test the data link.Telegram RX module receives the telegram data from the TR board through the MTCA.4 backplane and extracts the train ID numbers and the bunch pattern index values from the serial data received.

The Veto logic module processes the veto information coming through the SFPs and formats the data to be sent synchronously to the 99 MHz clock to the FEE units.

The clocking circuitry includes a local crystal oscillator, PLL and non-PLL based multiplexers in order to provide an uninterrupted, stable clock to the final PLL which multiplexes the bunch clock to provide the 99 MHz clock. This clock then goes into a 1:16 LVDS fanout chip. A copy of this clock also goes back to the DAMC2/FPGA through the RTM connector.

The current configuration of the CC RTM showed a high TIE and period jitter reading on the 99 MHz clock with the shape of the histogram suggesting a high amount of deterministic jitter. The high peak around the 780 kHz and a smaller peak at double this frequency in the jitter spectrum corresponds to the switching frequency of the DC/DC converter. Therefore, the main jitter contribution comes from the ripple on the 3.3 V output from the DC/DC converter.

The tests involved applying filtering on the 3.3 V rail to reduce the jitter readings. In order to do this, LTM4600EV was soldered on a small PCB and this PCB is attached to the CC RTM by cables so that it received the 12V RTM power from the DAMC2. The most promising jitter readings were obtained when a LC filter (1µH/100µF) is attached to the output of the DC/DC converter in addition to the required capacitors.

The configuration of the CC RTM with filtering showed a significant reduction in both TIE and period jitter readings.

The link between a FEE unit and the CC system consists of 3 LVDS pairs to transfer the 99 MHz clock, FAST data and the VETO information and 1 pair to receive the status information from the unit. One CC RTM can support up to 16 FEE units which in turn support 1 mega pixel detector.

The tests involved using the worst case signal which would cause maximum DC wander on the AC coupled data link. A prototype FEE board developed by STFC is used as the receiver card. The data is generated such that short bursts of 20-bit Pseudo Random Bit Sequence (PRBS) words are interspersed between long sequences ones or zeros. The sequence always starts with a predefined start word for synchronisation.

The tests were performed using Ethernet cables of lengths 10m, 15m, 20m, 30m and 50m. There were no errors observed during a period of more than 24 hours with the CAT6 SFTP cables up to 30m.

We envisage further improvements when this filtering scheme is employed on the final version of the CC RTM and the voltage plane for the clocking circuitry is separated from the main power plane by a ferrite bead.

In order to synchronise the operation of the master and the slave boards, 99 MHz clock generated on the RTM is put on the TCLUK line and the MTCA.4 backplane. The new version of DAMC2 board is currently developed by DESY supports this feature. With the slave boards in the same 12-slot crate up to a 6 mega pixel detector can be supported.