Design and Development of Electronics for the EuXFEL Clock and Control System

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as part of EuXFEL, WP76 : DAQ and Control

UCL

The European Free Electron laser (EuXFEL) facility will generate coherent and intense X-ray flashes at up to 27000 flashes per second with a ~4.5 MHz bunch delivery rate.
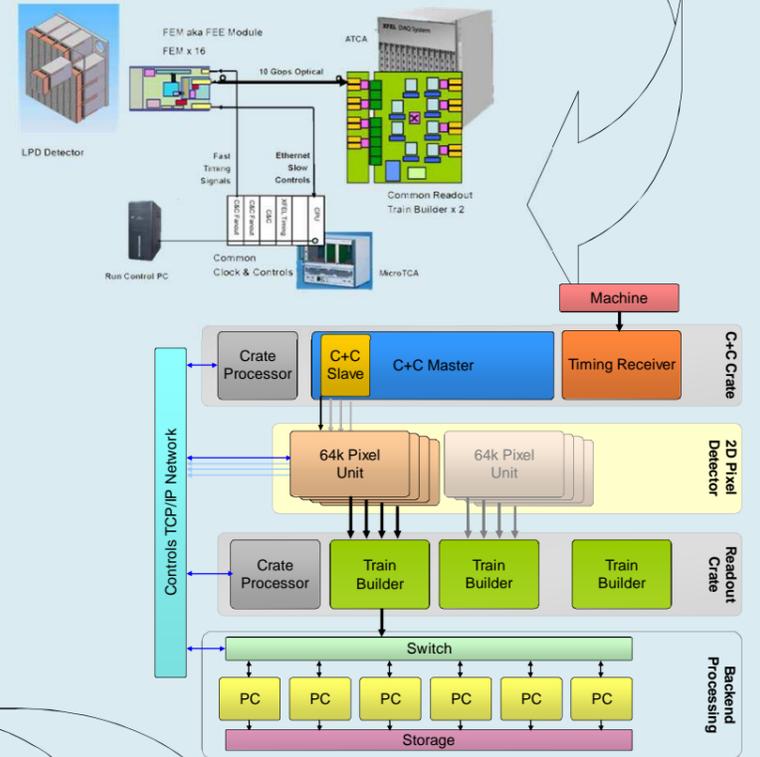
Each flash is intense enough to produce to produce a full diffractive picture of scattering targets.
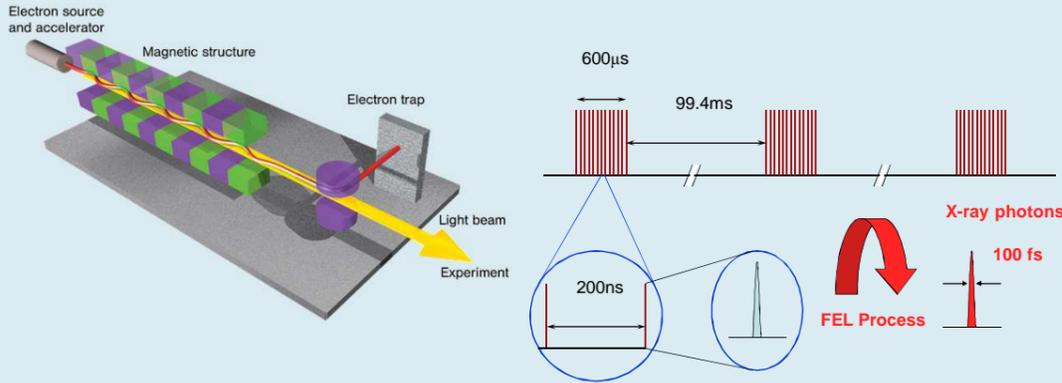
The detectors for the 2D camera systems will be able to capture up to 5000 images/second with a resolution of 1MPixel.

There are three detector designs being developed namely, AGIPD, LPD and DSSC. These three differ in terms of the functionality and the technologies involved in the design, however the overall structure which consists of sensor modules with an ASIC and Front End Modules (FEM) is similar.

Electron source and accelerator
Magnetic structure
Electron trap
Light beam
Experiment
600µs
99.4ms
200ns
X-ray photons
100 fs
FEL Process

LPD DAQ and System Interfaces

The Clock and Control (CC) system provides the synchronising clock and bunch and train related information to the FEM electronics. It also receives status feedback from FEMs and distributes the veto signals to the FEMs to reject some of the detector data

The CC system consists of a MTCA.4 Advanced Mezzanine Card (AMC) board and a Rear Transition Module (RTM)
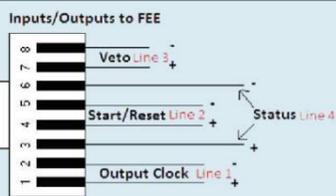
The MTCA.4 AMC board (DAMC2) is designed by DESY as a multi-purpose FPGA hardware platform for various projects in DESY and provides the processing capability for the CC functionality.
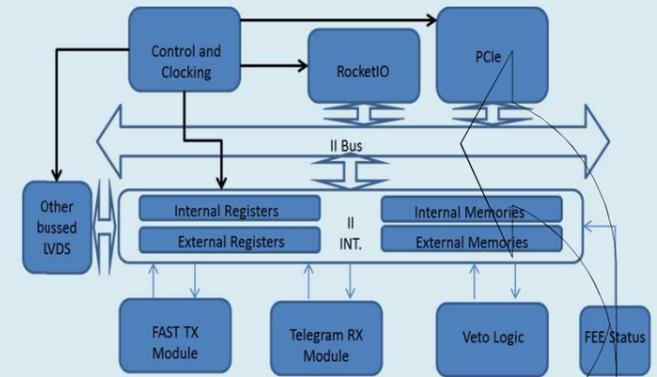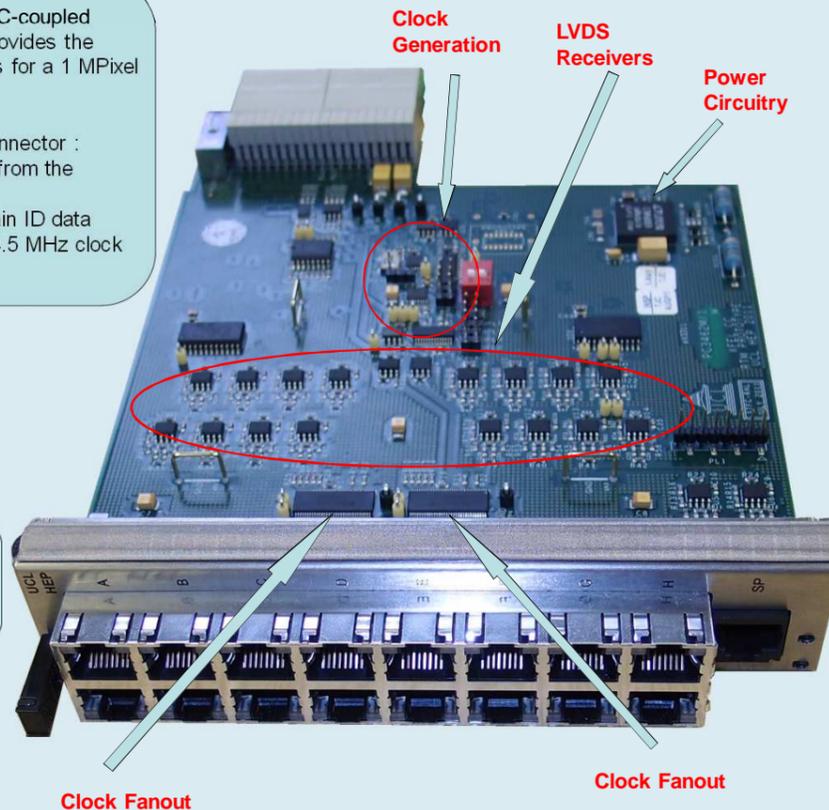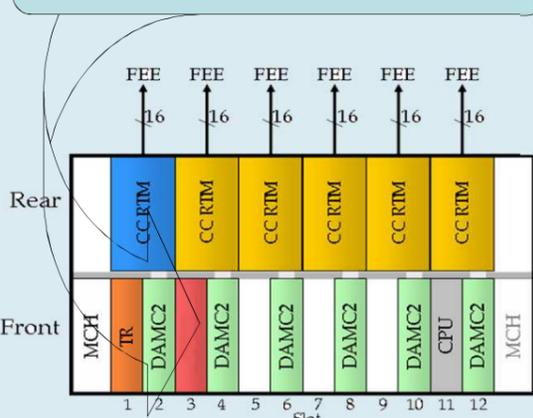
We have developed a custom RTM board according to the MTCA.4 standard which connects to the DAMC2 through two thirty-pair Advanced Differential Fabric (ADF) connectors.

The connections to the FEM boards are realised on AC-coupled LVDS links on CAT5 RJ45 cables. The RTM board provides the number of channels to support up to 16 FEM modules for a 1 MPixel 2D detector.

Each channel comprises 4 LVDS pairs on an RJ45 connector :
• Output clock (FAST clock) : ~99 MHz clock derived from the 4.5 MHz bunch clock.
• Output data (FAST data) : trigger start signal and train ID data
• Veto : bunch reject data encoded on a either 99 or 4.5 MHz clock
• Status : status feedback from the FEMs

Clock Generation
LVDS Receivers
Power Circuitry
Clock Fanout

Inputs/Outputs to FEE
Veto Line 3
Start/Reset Line 2
Status Line 4
Output Clock Line 1

The CC system receives clock and system information from the EuXFEL Timing Receiver (TR) through MTCA.4 crate backplane

FEE FEE FEE FEE FEE FEE
16 16 16 16 16 16
Rear
CC RTM
Front
MCH TR DAMC2 DAMC2 DAMC2 DAMC2 DAMC2 CPU MCH
1 2 3 4 5 6 7 8 9 10 11 12
Slot

The firmware block diagram for the CC board

Control and Clocking — RocketIO — PCIe
II Bus
Other bussed LVDS
Internal Registers — Internal Memories
External Registers — External Memories
II INT.
FAST TX Module — Telegram RX Module — Veto Logic — FEE Status

The FAST TX module generates the FAST data to the FEMs.

The telegram RX module receives and decodes the information coming from TR board on a clock and data pair through the backplane.

The PCIe block provides the connection to the crate CPU to receive configuration data from the control software.

There is a separate module for generating the veto data. The RocketIO module makes use of the SFPs on the DAMC2 board and provides an optional veto source input to the firmware.

All the modules in the firmware are integrated through a bus and a register block called Internal Interface (II) which is developed by DESY.

The CC hardware/firmware system is designed to provide the flexibility, extensibility and scalability to support possible future upgrades to the DAQ.

It also reduces the cost and effort for the development of such system by using a general-purpose MTCA.4 FPGA board as its processing platform and an RTM to provide the custom functionality.