Project Specification

Project Name: ZEUS MVD HELIX Driver Demonstrator

Version: 1.1

Approval:

	name	signature	date
Project Manager	**R. Halsall**	**XXXXXXXXX**	**12 June 98**

Distribution for all updates:

Project Manager: R. Halsall
Customer: Jon Butterworth, Val Noyes
Group Leader responsible for Project: Rob Halsall
Project Managers of related projects:

Additional distribution at PDR and FDR: John Lane

System Design Group Leader: R. Halsall
Micro Electronics Design Group Leader: M. French
Design Support Group Leader: S.P.H. Quinton
Management Support Services Group Leader: Chris Lowe
Electrical Systems Design Group Leader: J.F. Connolly

1.0 Scope

ZEUS Microvertex Detector (ZEUS MVD) upgrade, specifically the clock & control. Helix Interface consists of HELIX fanout module & HELIX Driver module. UCL are responsible for the Clock & Control System & the design of the Masterbox.

This is an R&D Project to build a Helix Driver Demonstrator for the August Beam Test in DESY. The main aim is to investigate key features of the Helix Driver namely;

Running CMOS and LVDS Drivers on shifted power supplies (-2V)
Micro Cable & 'SCSI' connectors
Signal Integrity

2.0 Related projects and documents

ZEUS MVD, ZEUS MVD Masterbox, HELIX Front End, ADC & ZEUS Slow Control DAQ.

Electronics & DAQ Page
http://www-zeus.desy.de/~zeusmvd/MVDeldaq.html

DAQ Document
http://www-zeus.desy.de/~polini/ZEUS_ONLY/mvddaq/mvddaq.html
http://wwwasic.ihep.uni-heidelberg.de/~feuersta/projects/Helix/helix/helix.html

Helix documentation
http://wwwasic.ihep.uni-heidelberg.de/~feuersta/projects/Helix/helix.ps

Masterbox documentation
http://www.hep.ucl.ac.uk/zeus/mvd/candc.html

ADC documentation
http://www-zeus.desy.de/~carlin/microvertex/adcm/sld001.html
http://www-zeus.desy.de/~carlin/microvertex/adc2/index.htm

3.0 Technical Aspects

3.1 Requirements

Receive Clock & Control signals from Masterbox and fanout to 2 chains of HELIX ASICs in the MVD Front End. Additionally receive & fanout Serial download data for HELIX from an external Pattern Generator. Switch in Pattern Generator signals under control of a Pattern Generator run/load' signal

Drive shifted (-2V) CMOS & LVDS signals to the HELIX ASICs at the Front End.

3.2 Specification of deliverables

The module will be a 6U VME Module, Wire Wrap construction, VME provides power only, additional -5.2V supply required on J2.

Inputs from Masterbox;

Signal		frequency	mode	level	pins	connector	
clock	input	10M Hz	clock	Diff ECL	2	IDC
not reset	input	10M Hz	synch	Diff ECL	2	IDC
trigger	input	10M Hz	synch	Diff ECL	2	IDC
test pulse	input	10MHz	vari delay	Diff ECL	2	IDC

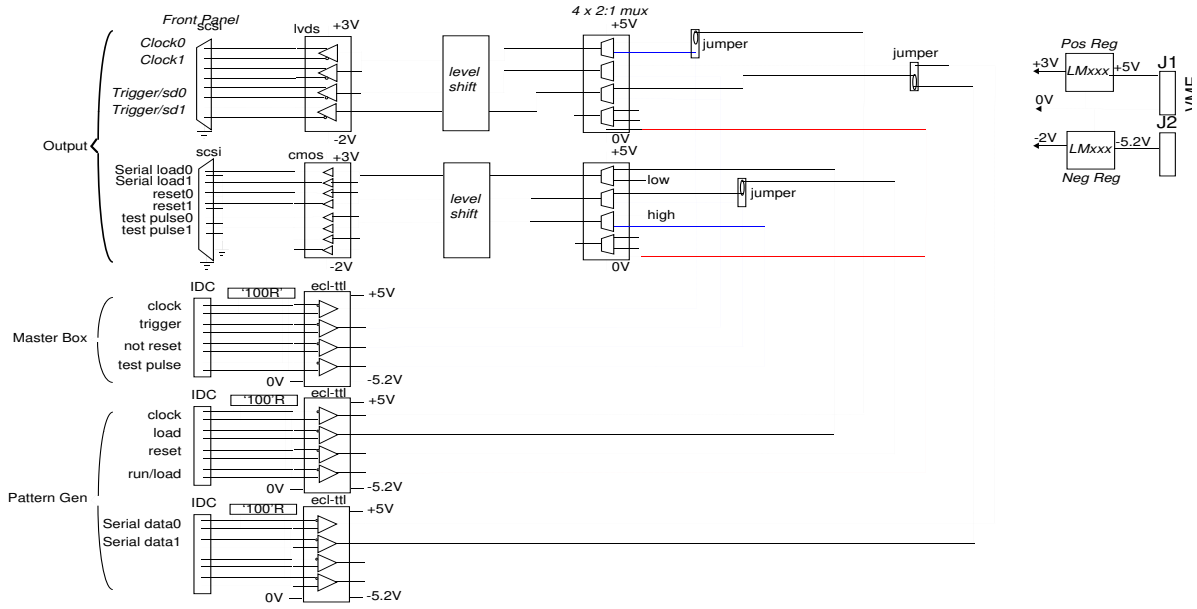
Inputs from Pattern Generator;

Signal		frequency	mode	level	pins	connector	
clock	input	10M Hz	clock	Diff ECL	2	IDC
not reset	input	10M Hz	synch	Diff ECL	2	IDC
load	input	10M Hz	synch	Diff ECL	2	IDC
Serial Data0	input	10M Hz	synch	Diff ECL	2	IDC
Serial Data1	input	10M Hz	synch	Diff ECL	2	IDC
run/load	input		asynch	Diff ECL	2	IDC

Outputs to Helix Front End, fanout x2;

Signal		frequency	mode	level	pins	connector	
Clock	output	10M Hz	clock	LVDS	2	SCSI
Not Reset	output	10M Hz	synch	CMOS	1	SCSI
Trig/Serial D	output	10M Hz	synch	LVDS	2	SCSI
Serial Load	output	10M Hz	synch	CMOS	1	SCSI
Test Pulse	output	10MHz	vari delay	CMOS	1	SCSI

Block Diagram;



3.3 Manufacturing

Wire Wrap construction, constructed in house, through hole - off the shelf components.

3.4 Testing and product control

Construct, Test and develop on the bench. Tests will be carried out as the module is constructed.

Test at RAL standalone
UCL with Masterbox
DESY complete chain

3.5 Shipping and Installation

Ship demonstrator to UCL or DESY as required by customer.

3.6 Maintenance and further orders

TBD

4.0 Project Management

ZEUS MVD, Electronics, Roberto Carlin
ZEUS MVD UK, Val Noyes
ZEUS MVD Clock & Control, Jon Butterworth, John Lane, Martin Postranecky
ZEUS MVD HELIX Driver, RAL Project Manager, RAL Engineer

4.1 Personnel

Project Manager/Engineer	R. Halsall
Project Engineer	S. Galagedera
Technician Engineer	J. Baker

4.2 Deliverables

RAL;

HELIX Driver Demonstrator, 1 Off

Customer Supplied;

VME Crate
VME SBC MVME2600 /Lynx-OS
Software
ECL Pattern Generator
Masterbox

4.3 Project plan

HELIX Driver Demonstrator

Project Spec	June 12
Preliminary Design Review/Sign off	June 12
Construct & Develop	June-July
Ready	3 August

4.4 Design Reviews

Customer will be invited to attend Intermediate & Final Design Reviews

4.5 Training

NA

4.6 CAE and test equipment

NA

4.7 Costs and finance

Estimated Effort (Staff Months);

Project Manager/Engineer	1
Project Engineer	1
Technician Engineer	1
Total Effort	3

Estimated Component Costs;

£1K

Cost Centres;

Effort	QF00510	maps onto FC76000
Travel	FC77400 TDD	
Components	FC76400 TDD	

4.8 IPR and confidentiality

Not confidential, CCLRC owns IPR

4.9 Safety

HELIX Input Protection power supply fail safe - DESY will build in fail-safe series resistors to prevent over current through protection diodes to protect inputs from power supply failure while Helix Driver is driving the HELIX inputs.

4.10 Environmental impact

Standard electronic module.