Survey of SCT Latency

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Outline:

- **Latency budget**
- **Summary table**
- **Timing diagram**

See:

http://www.hep.ucl.ac.uk/~jbl/SCT/SCT_latency.txt

L1 Trigger Latency Budget

The latency is the time from the interaction until the L1A trigger signal is received by the front-end pipeline. We need to make sure that when the L1A arrives at the pipeline of ABC(D) the data is still there.

The following table is a summary of latency budgets (the first column) up to the point of extracting data from the pipeline. The target for the total latency is 128 BC and we are working to reduce the total. The biggest uncertainty is the rack positions in USA15.

Latency summary table

BC is latency in 25ns Bunch Crossings
CK is discrete delay (flip-flop like) which is whole ClocK periods

BC	CK	Item	Comment	Source
77.9	?	CTP output	17.8 BC is contingency L1 TDR p452	Ellis
2	0	8m cable	also includes fanout	L1 TDR p442
0.1	0	TTCvi		L1 TDR p442
0.1	0	cable		L1 TDR p442
0.9	0	TTC crate	last four give TTC 3.1 BC	L1 TDR p442
8	0	40m fibre	conservative	Farthouat
3	?	TTCrx	92 BC so far	Farthouat

SCT latency summary table

BC	CK	Item	Comment	Source
92		TTCrx output		Farthouat
3	2	TIM	1 BC is contingency	Postranecky
0.2	0	Backplane	conservative	Postranecky
4	4	ROD	safe but prefer 7 BC (range 2-7)	Pier/Dao
1	0	BOC card	conservative	Goodrick
2	1	BPM chip	conservative	Wastie
19.4	0	97m fibre	assumes worst case ROD position	Weidberg
1	0	DORIC	conservative	Weidberg
7	7	ABC(D)	conservative by 1 BC	Grillo

129.6		BC total	(units of 25ns)	

Trigger/DAQ latency

My understanding of the advertised 2.5μs (100 BC) is (L1 TDR p452):

```
 BC
 57.9 CTP output: currently 60.1 using up 2.2 BC of contingency
 20.0 contingency
  3.1 TTC
 16.0 80m fibre
  3.0 TTCrx
-----
100.0
```

ROD crate timing diagram to define latencies

```
TTCrx: ----->
          ----------
L1A o/p --          --
             --
CLK o/p    --

TIM:         <----- TIM ----->
                          ----------
L1A o/p                 --          --
                              --
CLK o/p                     --

ROD:                      --->  <--- Backplane
                          ------------
L1A i/p                 ----        ----
                                --                   --
CLK i/p                       --                   --

BOC:                            <------- ROD ------->
                                               ----------
L1A i/p                                      --          --

BPM:                                             --->     <--- BOC
                                                  ----------
L1A i/p                                         --          --
                                                          --
CLK i/p                                                 --
                                                          <----- BPM -----
```