TTC Interface Requirements

J.M.Butterworth, D.A.Hayes, J.B.Lane, M.Postranecky

UCL

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Outline:

- **Essential Model**
- **Requirements**
- **Interface Specs**

See:

http://positron.ps.uci.edu/~roddaq/roddaq.html

Essential Model

- Context
- TTC Interface Module (TIM)
- SCT TTC System
- Busy Module

Requirements

- Interface to ROD
- Interface to TTC
- Interface to CTP
- Interface to local processor
- Transmission of Clock and Control

Requirements

- **Interface to ROD**

Output to ROD

clock:	BC	Bunch Crossing clock
fast command:	L1A	Level 1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	Calibrate signal
event ID:	L1ID	24-bit Level 1 trigger number
	BCID	12-bit Bunch Crossing number
	TTID	8-bit Trigger Type

Front End commands

Busy from ROD

Requirements

• Interface to CTP

SCT Busy signal

ROD Crate Busy signal

• Interface to local processor

VME interface

Configuration and monitoring

Command execution

Requirements

- **Transmission of Clock and Control**

Clock source

Clock stability and jitter

Clock phase delay

Commands required

Origin of commands

Latency of fast commands

Flow control of event ID

Addresses of commands

ROD to/from TTC Distribution

- **Signals**

CLKP, CLKN

`TTC0: L1A`

`TTC1: L1Reset`

`TTC2: BCReset`

`TTC3: CAL`

`TTC4: SerialID`

`TTC5: RODClear`

BUSYN

- **Timing**

- **Electrical Notes**