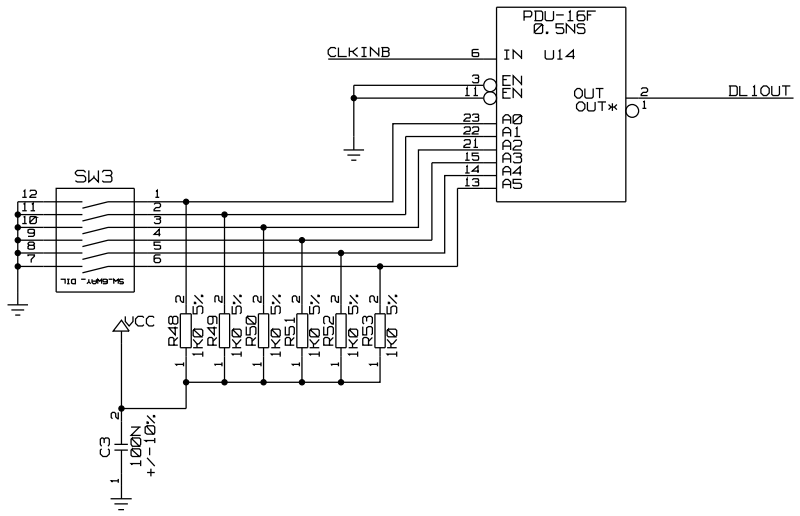
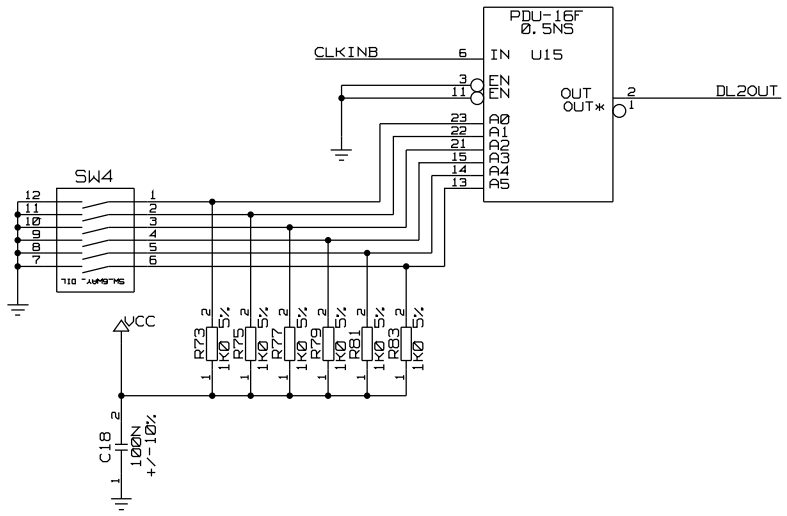
A	2-TE-0095-009-03-A	THIS DRAWING CONFORMS TO B.S. 3939

SET DELAY FOR CLK1



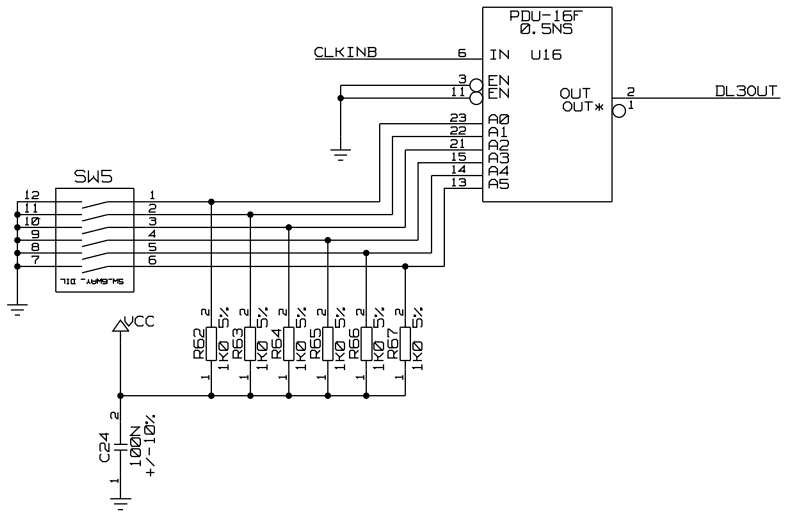
DELAY 9-41USEC IN STEPS OF 0.5USEC

SET DELAY FOR CLK2



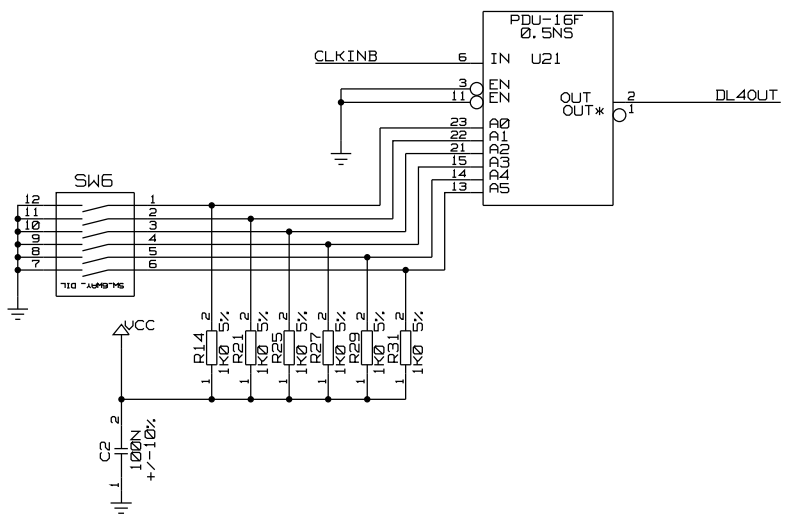
DELAY 9-41USEC IN STEPS OF 0.5USEC

SET DELAY FOR CLK3



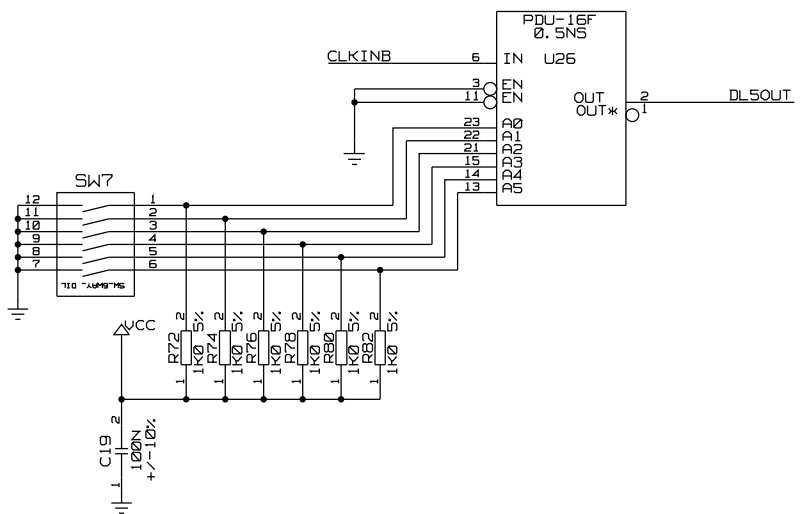
DELAY 9-41USEC IN STEPS OF 0.5USEC

SET DELAY FOR CLK4



DELAY 9-41USEC IN STEPS OF 0.5USEC

SET DELAY FOR CLK5



DELAY 9-41USEC IN STEPS OF 0.5USEC

DECOUPLING

ALL CHIPS IN
DECOUPLED SOCKETS
TO VCC

DRAWING
PC3124M
1798
Thu Jul 16 14:31:39 1998

ISSUE	DATE	MOD NO.	DRN BY.	CHKD.	APPD.	STATUS
A	21-05-1998	- - - -	D. J. BECKETT	M. POSTRANECKY	M. POSTRANECKY	

USED ON ATLAS

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RUTHERFORD APPLETON LABORATORY, CHILTON, OXON OX11 0QX.

TITLE

PC3124M CIRCUIT

C+C MASTER MODULE

A 2-TE-0095-009-03-A

TOTAL NO. OF SHEETS 7

A 2-TE-0095-009-03-A