MUON CLOCK BOARD

Preliminary Design Specification (DRAFT)

Mike Matveev, Paul Padley

Rice University

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Abstract

This document describes the functionality of the Muon Clock Board (CB) for the CMS Endcap Muon System and its communication with other modules of the Trigger System (Anode and Cathode LCT Cards, Trigger Motherboard (TMB), Data Acquisition Motherboard (DAQMB), Muon Port Card (MPC), Sector Receiver (SR) and Sector Processor (SP)).

Introduction

The Muon Cathode Strip Chambers (CSC) Trigger Electronics consists of an on-chamber mounted Front End Boards (FEB), electronics on the periphery of the detector, and preprocessing farm in the counting room. Trigger system on the detector periphery includes anode and cathode LCT cards, TMB, DAQMB and MPC. SR and SP modules are located in the counting room. The current plan is to build LCT, TMB, DAQMB, MPC, SR and SP modules as a standard VME 9U*400 mm cards [1].

All elements of the Muon Trigger System should be synchronized with the LHC operation. The Timing, Trigger and Control (TTC) system for LHC detectors has been specified and detailed description of this system and its functionality can be found, for example, in [3]. The TTC system is based on an optical fun-out system and provides the distribution of the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers from one source to about 1000 destinations. The TTC system also allows to adjust the timing of all of these signals. There are three main components in the TTC system:

- The TTC crate and the fibre network
- The TTC VME Interface (TTCvi)
- The TTC receiver (TTCrx)

On the low level of the TTC system, the TTCrx receives control and synchronization information from the central TTC system through the optical cable and outputs a TTL-compatible TTC signals in parallel form. The TTCrx card is based on custom IC [2]. We propose to build in an TTCrx card into our CB and use it for the synchronization of all CSC muon trigger modules in the 9U VME crates on the detector periphery and in the counting room. All TTC signals which are necessary for the on-chamber FEB will be delivered from the LCT cards via copper links.

TTC Signals

The full list of external signals which are outputs of the TTCrx IC [2] is given in Table 1.

Table 1

Signal	Bits	Short Description
TestIn	1	TTCrx IC test input
TestOut	1	TTCrx IC test output
BcntRes	1	Bunch Counter Reset signal
BCntStr	1	Bunch Counter Strobe. Indicates that a bunch number is present on the output BCnt<11:0> bus
Brcst<7:2>	6	Broadcast commands/data output bus
BrcstStr<2:1>	2	Broadcast messages strobes
Clock40	1	LHC 40.08 MHz non-deskewed reference clock signal
Clock40Des<2:1>	2	LHC 40.08 MHz deskewed reference clock signals
ClockL1Accept	1	This signal combines the non-deskewed clock and the first level trigger-accept information
DbErStr	1	Indicates that a double error or a frame error has occurred
Dout<7:0>	8	Data bus. Normally used to output the data content of an individually-addressed commands/data
DQ<3:0>	4	Data qualifier bits. Indicate the type of data on the data bus register
DoutStr	1	Data out strobe. Indicates valid data on the data bus
EvCntHStr	1	Event counter high word strobe
EvCntLStr	1	Event counter low word strobe
EvCntRes	1	Event counter reset signal
In and In_b	1	Differential analog inputs

JTAGTCK	1	JTAG test clock
JTAGTDI	1	JTAG test data input
JTAGTDO	1	JTAG test data output
JTAGTMS	1	JTAG test mode select
JTAGTRST_b	1	JTAG test reset
L1Accept	1	First level trigger accept signal
PromClock	1	Serial configuration PROM clock signal
PromD	1	Serial configuration PROM data output
PromReset	1	Serial configuration PROM reset signal
Reset_b	1	Active low reset signal
Res and Res_b	2	Analog input bias
Serial_B_Channel	1	This signal is used to make available to the users the serial data received on channel B (including frame, start and stop bits)
SinErrStr	1	Single error strobe
SubAddr<7:0>	8	Subaddress bus. Used to output the subaddress content of an individually address commands/data
TTCReady	1	TTCrx ready
VcoOn	1	A logic "0" in this pin disables the PLL VCO

Signals from TTCrx to trigger modules

The TTCrx signals which are needed for every trigger module are listed in Table 2.

Table 2

Signal	LCT	TMB	DAQMB	MPC	SR	SP
TestIn		-		-		
TestOut		-		-		
BCntRes		+		+		

BCntStr		-		-		
Brcst<7:2>		-		-		
BrcstStr<2:1>		-		-		
Clock40		?		?		
Clock40Des1		+		+		
Clock40Des2		?		?		
ClockL1Accept		-		-		
DbErStr		-		-		
Dout<7:0>		-		-		
DQ<3:0>		-		-		
DoutStr		-		-		
EvCntHStr		-		-		
EvCntLStr		-		-		
EvCntRes		-		-		
In and In_b		-		-		
JTAG signals		-		-		
L1Accept		-		-		
PromClock		-		-		
PromD		-		-		
PromReset		-		-		
Reset_b		-		-		
Res and Res_b		-		-		
Serial_B_Channel		-		-		
SinErrStr		-		-		
SubAddr<7:0>		-		-		

TTCReady		-		-		
VcoOn		-		-		

1. Communication with trigger modules

We propose to use point-to-point signal distribution from CB to trigger modules over unused lines of the VME J0, J1 or J2 backplane or over custom backplane.

2. Mechanics

We propose to build a CB board as a VME transition module [1] located on the dedicated station in VME crate.

3. VME Interface

We intend to make some TTCrx output status signals (like DbErrStr, SinErrStr, TTCReady) available via VME bus.

6. CB Prototype for the CSC Summer 99 beam tests

We plan to build the first CB prototype for the CSC Summer 99 beam tests. It will be able to receive 40 MHz clock signal either from on-board quartz or from external generator and distribute it to limited number (3..5) of VME modules over unused lines of the J2 backplane. The CB prototype will also be able to generate a 25 ns long BcntRes signal on VME command and translate it to trigger modules.

References

[1]. VME64x 9U x 400 mm Format Draft Standard. VITA 1.3-199x. Draft 0.7. 4 June 1997.

[2]. B.G.Taylor. Timing, Trigger and Control (TTC) Systems for LHC Detectors. CERN/ECP http://www.cern.ch/TTC/intro.html

[3]. J.Christiansen, A.Marchioro and P.Moreira. TTCrx Reference Manual. July 1997. Version 2.2. CERN-ECP/MIC, Geneva Switzerland.

[4]. http://www.nsc.com/pf/DS/