

VME 9U MUON CLOCK AND CONTROL BOARD

User's Manual

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Abstract

This document describes the functionality of the 9U Muon Clock and Control Board (CCB) Prototype for the CMS Cathode Strip Chamber (CSC) tests in Summer'99 and its communication with other modules of the Trigger System.

Introduction

The CSC Trigger Electronics consists of an on-chamber mounted Front End Boards (FEB), electronics on the periphery of the detector, and preprocessing farm in the counting room. Trigger/DAQ system on the detector periphery includes anode and cathode LCT boards (ALCT and CLCT), TMB, DAQMB and MPC. SR and SP modules are located in the counting room. The current plan is to build LCT, TMB, DAQMB, MPC, SR and SP modules as a 9U*400 mm cards.

All elements of the Muon Trigger System should be synchronized with the LHC operation. The Timing, Trigger and Control (TTC) system for LHC detectors has been specified and detailed description of this system and its functionality can be found, for example, in [1-3]. The TTC system is based on an optical fan-out system and provides for the distribution of the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers from one source to about 1000 destinations. The TTC system also allows to adjustments of the timing of all of these signals. There are three main components in the TTC system:

- The TTC crate and the fibre network
- The TTC VME Interface (TTCvi)
- The TTC receiver (TTCrx)

On the low level of the TTC system, the TTCrx receives control and synchronization information from the central TTC system through the optical cable and outputs TTL-compatible TTC signals in parallel form. The TTCrx card is based on a custom IC [2], which is programmable through an I2C serial interface. We propose to build in an TTCrx card into our CCB and use it for the synchronization of all CSC muon trigger modules in the 9U VME crates on the detector periphery and in the counting room. All TTC signals which are necessary for the on-chamber FEBs will be delivered from the LCT cards via copper links.

1. TTC Interface

The list of signals which CCB accepts from the TTCrx board is given in Table 1.

Table 1

Signal	Bits	Short Description
BcntRes	1	Bunch Counter Reset signal
BCntStr	1	Bunch Counter Strobe. Indicates that a bunch number is present on the output BCnt<11:0> bus
Brcst<7:2>	6	Broadcast commands/data output bus
BrcstStr<2:1>	2	Broadcast messages strobes
Clock40Des<2:1>	2	LHC 40.08 MHz deskewed reference clock signals
DbErStr	1	Indicates that a double error or a frame error has occurred
Dout<7:0>	8	Data bus. Normally used to output the data content of an individually-addressed commands/data
DQ<3:0>	4	Data qualifier bits. Indicate the type of data on the data bus register
DoutStr	1	Data out strobe. Indicates valid data on the data bus
EvCntHStr	1	Event counter high word strobe
EvCntLStr	1	Event counter low word strobe
EvCntRes	1	Event counter reset signal
L1Accept	1	First level trigger accept signal
SinErrStr	1	Single error strobe
SubAddr<7:0>	8	Subaddress bus. Used to output the subaddress content of an individually address commands/data

In order to perform the programming and testing of the TTCrx chip and TTCrx board, the CCB integrates a Philips PCF8584 I2C-bus controller [4]. This controller is accessible through VME and provides access to the TTCrx ASIC via two wires.

2. TTC Signals for Trigger Electronics

Four signals [3] are needed for Trigger Electronics in order to perform all necessary synchronization and reset procedures. These signals are listed in Table 2. They can be extracted from the signals coming from the TTCrx board (Table 1) or may be generated inside CCB when TTC system is not available (in particular, for the '99 beam test) or for testing purposes. The sources of these signals in "TTC Simulator" mode are also listed in Table 2.

Table 2

Signal	TTC System	TTC Simulator
40MHz Clock	Clock40Des1	40MHz Quartz Oscillator
L1ACC	L1ACC	On Pretrigger *
Bunch Crossing Zero BX0	BX0	VME Command
RESET	RESET	VME Command

* Three sources of Pretrigger signal are possible for the '99 beam test: two pretrigger signals from external sources ("TR1" and "TR2" LEMO connectors on the front panel), and one source on VME Command addressed to CCB. CCB synchronizes any of these signals with its own Master 40MHz clock signal and outputs this resulting Pretrigger signal (100 ns pulse) to NIM trigger logic [5] outside 9U crate. This logic performs general synchronization of the trigger and DAQ for testing setup and returns L1ACC signal to CCB (L1A input on the CCB front panel). CCB internal logic synchronizes this signal with its own 40MHz clock and outputs it to all trigger/DAQ modules in 9U crate. BX0, L1ACC, and RES outputs to trigger/DAQ modules in 9U crate are 25 ns pulses, rising edge of the CLK validates each of these signals.

3. Distribution of the Clock and Control Signals to Trigger Modules

CCB distributes four signals to each trigger module in 9U crate over individual cables. Pin assignment of the 20-pin header (3M 80610565154, Digikey Part Number MHB20K-ND) is given in Table 3. The National DS90LV031/032 chipset is used.

Table 3

Contact	Signal	Contact	Signal
1	GND	2	GND
3	CLOCK+	4	CLOCK-
5	GND	6	GND
7	BX0+	8	BX0-
9	GND	10	GND
11	RESET+	12	RESET-
13	GND	14	GND
15	L1ACC+	16	L1ACC-
17	GND	18	GND
19	GND	20	GND

4. Control and Status Register (CSR)

The data format of the CSR is given in Table 4.

Table 4

Bit	Meaning
0	TTC Simulator/TTCrx Operation (=0: TTC Simulator, =1: TTCrx)
1	Source of LIACC when TTC Simulator (*)
2	Source of L1ACC when TTC Simulator (*)
3	-
4	-
5	-
6	-
7	-
8	-

9	-
10	-
11	-
12	-
13	-
14	-
15	-

*

Bit_1 Bit_2

- | | | |
|---|---|-----------------------------|
| 0 | 0 | Pretrigger from TR1 source |
| 1 | 0 | Pretrigger from TR2 source |
| 0 | 1 | not used |
| 1 | 1 | Pretrigger upon VME Command |

5. VME Interface

The CCB performs A24D16 VME Slave Function. The Base Address is selectable using DIP Switches S4 and S5 on the board (address bits A8..23). Decoded addresses are listed in Table 5.

Table 5

Address	Access	Register
Base + 0	Write	Generate Pretrigger from VME
Base + 2	Write	Generate RESET signal to trigger modules
Base + 4	Write	Generate BX0 signal to trigger modules
Base + 6	Read/Write	CSR1
Base + 8	-	-
Base + a	Write	Reset Internal Logic
Base + c	Read/Write	I2C Controller Philips PCF8584
Base + e	Read/Write	I2C Controller Philips PCF8584
Base + 10	Write	Reset I2C Controller Philips PCF8584
Base + 12	-	Reserved
Base + 14	-	Reserved

6. Front Panel

On the front panel are:

LEMO Connectors:

- TR1 (Input, NIM), External Pretrigger
- TR2 (Input, NIM), External Pretrigger
- L1A (Input, NIM), L1ACC coming from NIM logic
- CLK (Output, NIM), General clock signal for all trigger/DAQ modules in 9U crate
- BX0 (Output, NIM), Output signal to all trigger/DAQ modules in 9U crate

- RES (Output, NIM), Output signal to all trigger/DAQ modules in 9U crate
- L1A (Output, NIM), Output signal to all trigger/DAQ modules in 9U crate
- PRT (Output, NIM), Pretrigger output to NIM logic
- RESERVED (NIM), 3 Inputs and 3 Outputs
- 10-pin JTAG connector for PLD/PROM downloading/programming compatible with Altera Bit/Byte Blaster.

LEDs:

- +3.3V, +5V, -5.2V Power (green)
- CLK, BX0, RES, L1A (red) (Outputs to trigger/DAQ modules in 9U crate)
- TR1, TR2 (green) (Inputs from external Pretrigger sources)
- PRT (green) (Output to NIM logic)
- VME Access, JTAG Access (yellow)

References

- [1]. B.G.Taylor. Timing, Trigger and Control (TTC) Systems for LHC Detectors. CERN/ECP <http://www.cern.ch/TTC/intro.html>
- [2]. J.Christiansen, A.Marchioro and P.Moreira. TTCrx Reference Manual. July 1997. Version 2.2. CERN-ECP/MIC, Geneva Switzerland.
- [3]. W.H.Smith. CMS Synchronization Workshop Conclusions. Version 0.1.
- [4]. Philips Data Handbook IC12. 1997. I2C Peripherals.
- [5]. <http://www-collider.physics.ucla.edu/cms/bmtest99/>