SLOG
Generates test data, with 12 individually programmable channels, with LVDS outputs.
Write-up at http://hepwww.rl.ac.uk/atlas/tracking/mm/slog/slog.ps

RedLITMUS
LITMUS (LInk Test Module Using Seqsi) was a wire-wrapped prototype device which has been used at Oxford for the last year in carrying out bit error rate measurements on fibre-optic links.
RedLITMUS (Redesigned Link Test Module Using SLOG) will perform a similar role in harness testing.
Fig1 shows part of the test system. SLOG is used to generate test data, and this data is compared in RedLITMUS with the data returned from DORIC in one case and from VDC in the other.
The main functions required in RedLITMUS are

Align the returned data to the clock. Propose to use the PHOS4 delay chips (as used in MuSTARD)
Align the test data (in steps of 1 clock period) with the returned data, to compensate for cable and fibre delays and transit times through components.
Compare the aligned test data with the aligned returned data and count the occurrences of differences.

In order to deal with error rates varying from 100% to 10^{-9} or better, there will be 2 modes of error counting. The first, used to deal with high error rates, will involve counting for a fixed period. The second, used when error rates are low, will involve counting for long periods with the timing being done by the host computer.

fig 2 indicates the main functions with a first look at how these might be implemented.
This is very preliminary.

Status: a version of SLOG, modified to suit harness testing, is currently being manufactured and will be available early August.
RedLITMUS will be designed in September, pcb layout October, available end of 99.

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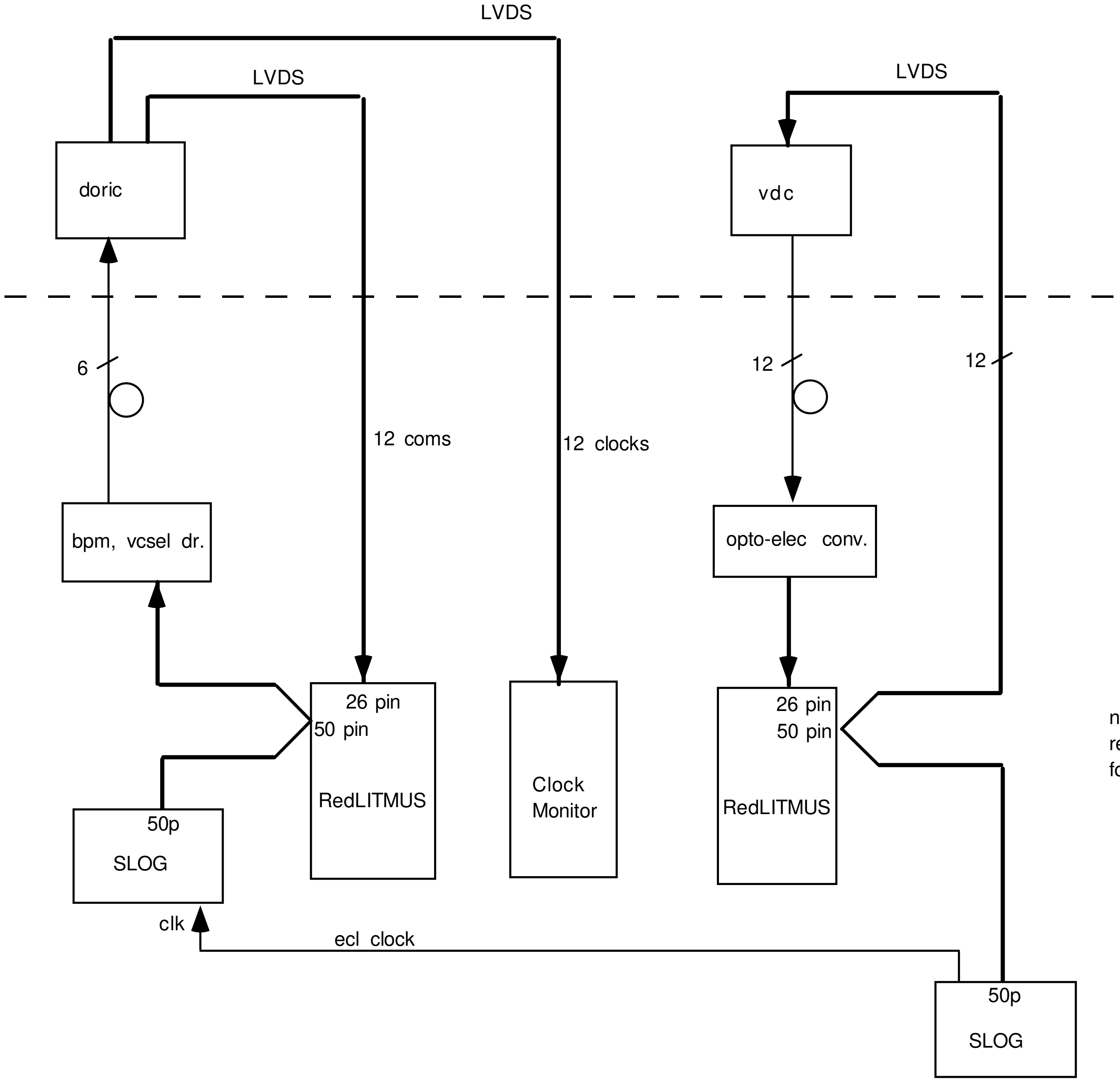
fig 1



note: clock termination requirements are different for the 2 slog/litmus pairs

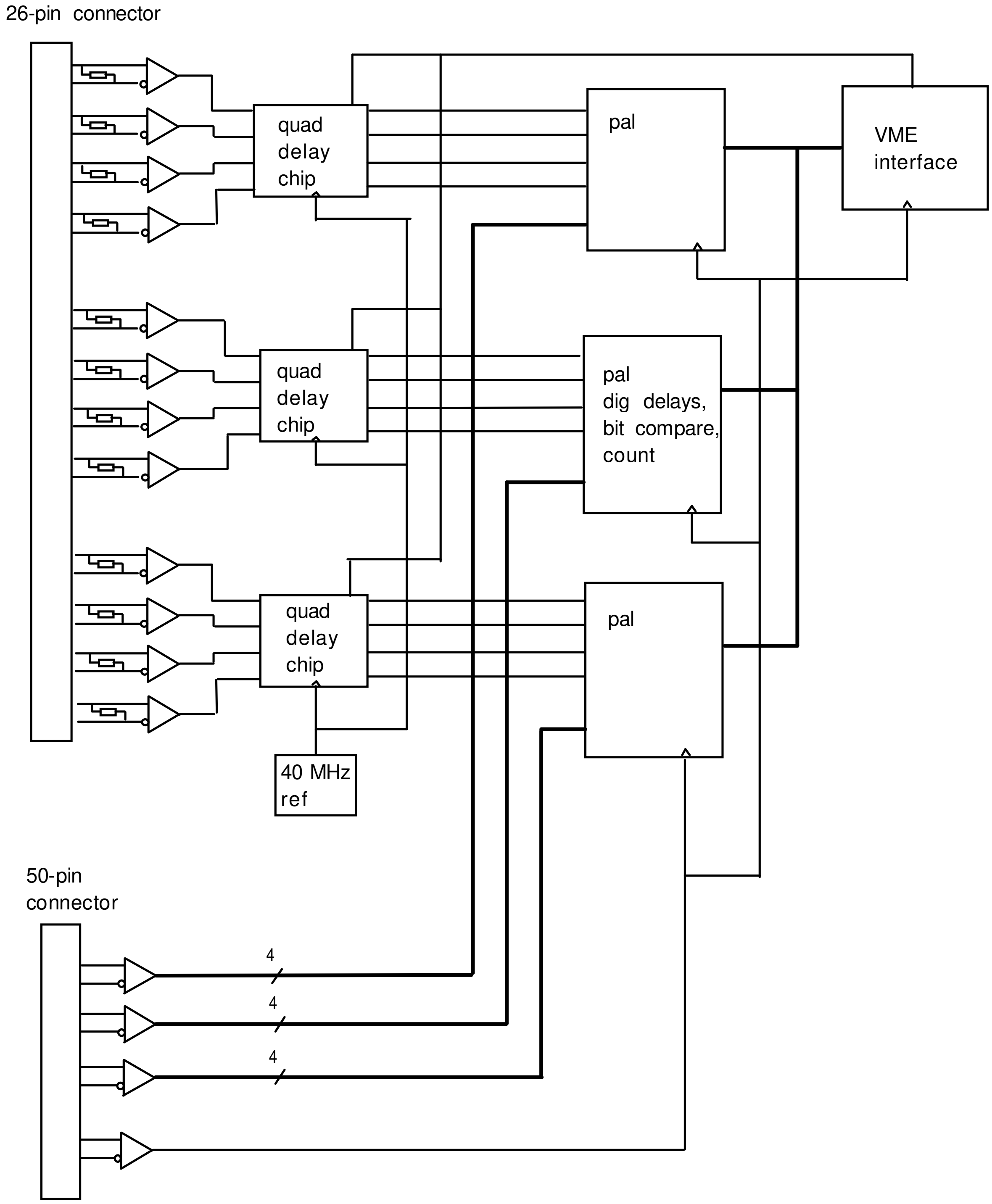

26-pin connector
quad
delay
chip
pal
VME
interface
quad
delay
chip
pal
dig delays,
bit compare,
count
quad
delay
chip
pal
40 MHz
ref
50-pin
connector
4
4
4

fig 2