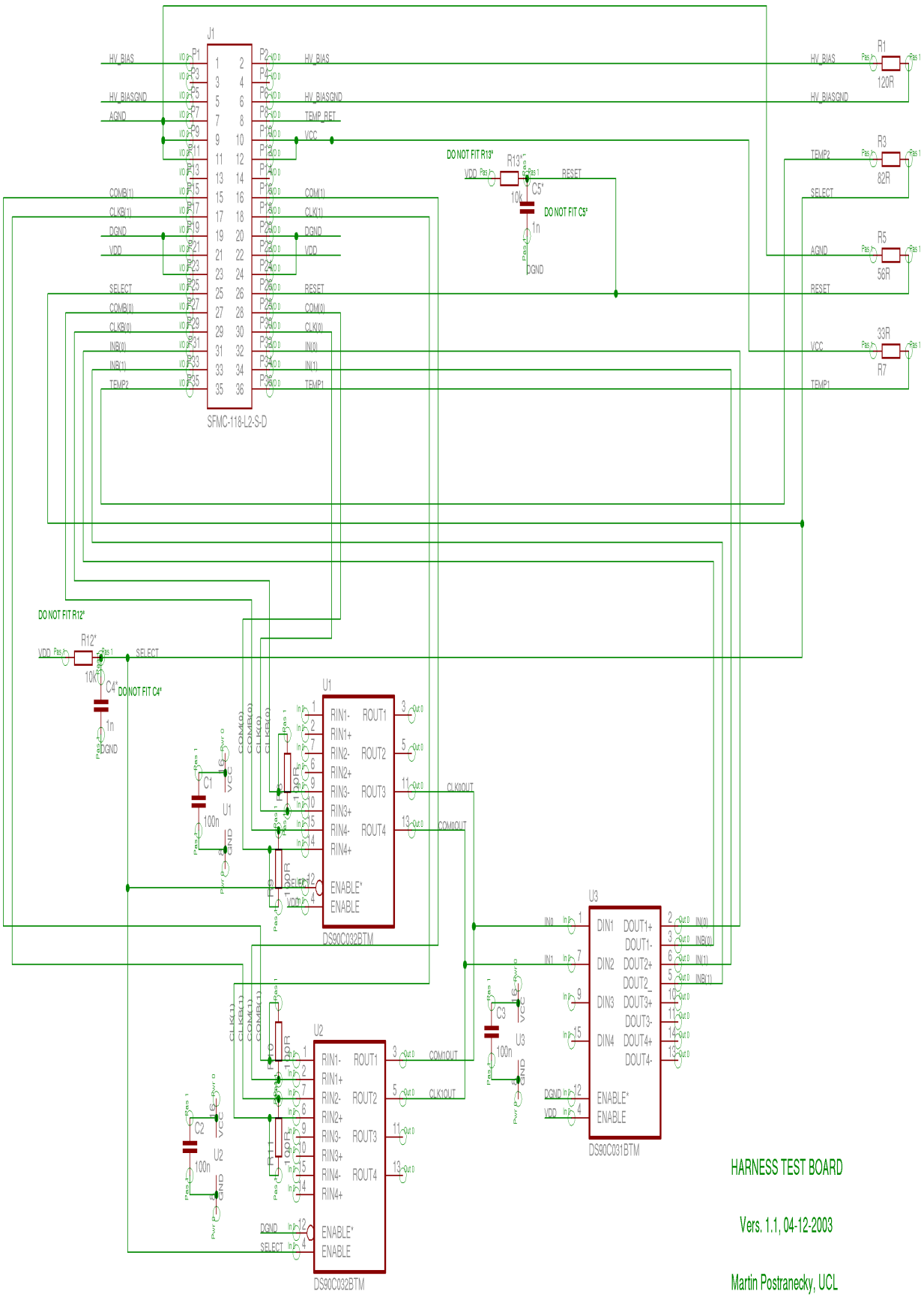
J1
SFMC-118-L2-S-D
HV_BIAS
HV_BIASGND
AGND
VCC
TEMP_RET
COM(1)
CLK(1)
DGND
VDD
RESET
COM(0)
CLK(0)
IN(0)
IN(1)
TEMP2
TEMP1
R1
120R
R3
82R
R5
56R
33R
R7
DO NOT FIT R13*
R13*
C5*
10k
1n
DO NOT FIT C5*
DO NOT FIT R12*
R12*
C4*
DO NOT FIT C4*
U1
DS90C032BTM
RIN1-
RIN1+
RIN2-
RIN2+
RIN3-
RIN3+
RIN4-
RIN4+
ROUT1
ROUT2
ROUT3
ROUT4
ENABLE*
ENABLE
CLK0OUT
COM0OUT
C1
100n
GND
U2
DS90C032BTM
COM1OUT
CLK1OUT
C2
C3
U3
DS90C031BTM
DIN1
DIN2
DIN3
DIN4
DOUT1+
DOUT1-
DOUT2+
DOUT2-
DOUT3+
DOUT3-
DOUT4+
DOUT4-
HARNESS TEST BOARD
Vers. 1.1, 04-12-2003
Martin Postranecky, UCL