Timing, Trigger and Control Interface Module for SCT Read Out Electronics

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ABSTRACT :

The SCT detector interfaces with the ATLAS Level 1 trigger using the LHC-wide TTC (Timing, Trigger, and Control) system. The design of the TIM (TTC Interface Module), part of the SCT off-detector electronics, and the interface with the RODs (Read Out Drivers), is described.

Also described is the forerunner of the TIM, the CLOAC (Clock And Control) module, developed to provide a stand-alone timing and trigger capability in the absence of the TTC system. CLOACs are currently used in the SCT tests at CERN. They are also available to the SCT community for use in front-end modules testing.

SUMMARY :

The TIM (TTC Interface Module) is designed to serve as the interface between the SCT off-detector electronics and the ATLAS first level trigger. Each crate of the ROD (Read Out Driver) modules contains a single TIM, which receives the timing, trigger, and control signals via the optical TTC distribution system.

Each TIM uses a LHC-standard TTCrx receiver chip to decode the signals and provide electrical outputs. The TIM then transmits this information to the RODs, with the correct timing adjustments, via a custom backplane.

The signals required by the RODs are :

Clock:	BC	Bunch Crossing clock
Fast Command:	L1A	Level 1 Accept
	ECR	Event Counter Reset
	BCR	Bunch Counter Reset
	CAL	Calibrate signal
Event ID:	L1ID	24-bit Level 1 trigger number
	BCID	12-bit Bunch Crossing number
	TTID	8-bit Trigger Type

Each TIM is also capable of full stand-alone operation, generating the above signals as requested by the local processor.

Each TIM receives the ROD BUSY returns from each ROD and provides a masked-OR output to a Busy Module.

Each TIM is implemented as a 9U PCB, containing a standard VME Slave interface to allow the local processor access to its registers and control bits, used in monitoring, configuration setup and the issue of stand-alone commands.

To prototype some of the stand-alone functionality of the TIM, and to generate the clock and fast commands to enable front-end modules to be tested in the absence of the TTC system, the CLOAC (Clock And Control) module has been designed.

The CLOAC module generates the clock and the fast commands as above, either on command from a local processor or fully stand-alone. The triggers can either be issued singly or repetitively, with the number and the frequency fully programmable and selectable as either a single frequency or an average random rate.

The CLOAC can also synchronise to an external clock and external fast commands, and it can receive BUSY inputs to provide a masked BUSY output.

The CLOAC provides four separate electrical outputs of the clock and command strings (as specified by the SCT front-end ASIC chip protocol).

The CLOAC module has been implemented as a 6U PCB with a standard VME Slave interface.

Some CLOAC modules have been used in the SCT system and beam test at CERN since 1998.

A number of CLOAC modules has been manufactured and made available to the SCT community.

MP 29 Apr 1999