University of Oxford
Department of Physics

Project Specification

Project Name: Biphase Mark Encoder and VCSEL Drive Control Chip

Project Code: NP-ATL-ROD-BIPHASE

Group: ATLAS

Version: DRAFT 1.0

Date: 26 March, 1998

Approval:

	Name	signature	Date
Project Manager	R. L. Wastie		
Originator	A. R. Weidberg		
Group Leader	R. Nickerson		
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1.0 Project Description

1.1 Abstract

The purpose of this project is to design, fabricate and test a chip that encodes clock, L1 & slow control into one fibre channel for the ATLAS SCT front-end electronics.

1.2 Scope

To design a further iteration of the driver for clock and control optical transmission. The control data will be encoded onto the 40 MHz clock using BiPhase Mark encoding[4]. The driver chip will be optimised for driving VCSELs as the light emitter. The device must be compatible with DORIC4 [4]. The chip will be mounted on to a daugtherboard for the VME Clock & Control Board[1] used in the CERN H8 1995 testbeam.

2.0 Changes from previous version

None.

3.0 Related projects and documents

3.1 Projects

NP-ATL-FEE-ABCRDOT	ABC readout	Oxford University
NP-ATL-ROD-BIPHALD	VCSEL Drive Control Chip	Oxford University

3.2 Documents

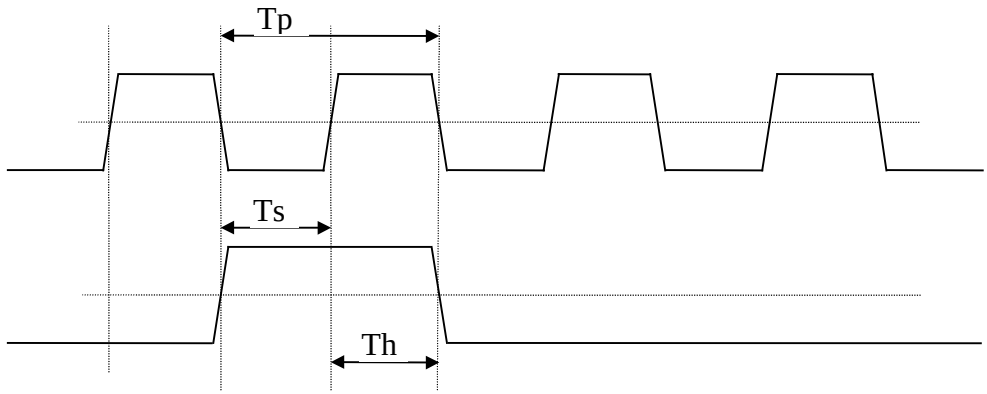
[1] ATLAS VME 8 Channel Fibre Optic Driver, Operating Manual, P. D. Shield, R. L. Wastie, Oxford.
[2] DORIC, A Front End Clock and L1 Distribution Chip, J. R. Gorbold and P. Seller.
[3] ABC (Atlas Binary Chip) Project Specification, D. Campbell, RAL.
[4] DORIC4 (Digital Opto-Receiver Integrated Circuit) Project Specification , D. J. White, RAL.
[5] LDC (LED Driver Circuit) Project Specification, D. J. White, RAL.
[6] Digital Readout Chip for Silicon Strip Detectors at SDC, K. Shankar, RAL, N. Kundu, Oxford.

4.0 Technical Aspects

4.1 Requirements

4.1.1 Input Requirements

The Biphase Mark Encoder VCSEL Drive Chip (BPM) will be a four channel device, it will receive and encode the Trigger Timing and Control (TTC) from the TTCrx chip (RD12) "TTCrx Reference Manual". It requires an input 80MHz Clock (CLK80), 40MHz Clock (CLK40) and 4 data channels, the data is 40MHz NRZ. The input data will be clocked on the positive edge of the 40MHz clock (CLK40), Fig 1.



Tp = 25ns ± 1ns, 3ns ≥ Ts ≤ 9ns, Th ≥ 0.5ns

Figure 1. Input Clock and Data signals

The logic input signals will all be CMOS 0-5 volts (V_{IL} 0.8v MAX, V_{IH} 2v MIN) except the VCSEL driver controls which will be DC voltages in the range 0-4 volts. The BPM will be controlled by a serial interface using two signals and a clock SCLK, DIN and $\overline{CS}$.

4.1.2 Output Requirements

BPM will have four VCSEL driver outputs. Each output will be capable of driving an VCSEL with its anode connected to 5 volts. The specifications for the electrical output of BPM are given in Table 1 below.

Table 1 Specifications for the electrical output of BPM

DC standing current	0-5 mA
Pulse current	1-20 mA
Rise time	<1 ns
Fall time	< 1ns

The specifications for the optical output from a VCSEL (HFE 4080) when driven by BPM are given in Table 2 below. Note that the timing specifications must be valid independently of the transition direction.

Table 2 Specifications for the optical output of a HFE 4080 VCSEL driven by BPM.

Rise Time	< 2 ns
Fall Time	< 3 ns
Width of 40 MHz pulse	11.5 – 13.5 ns
Clock jitter (RMS)	< 0.5 ns
Optical power coupled into 50 μm core fibre	> 1 mW

The BPM will encode the CLOCK and DATA for each channel and produce a Biphase Mark output, Fig 2.

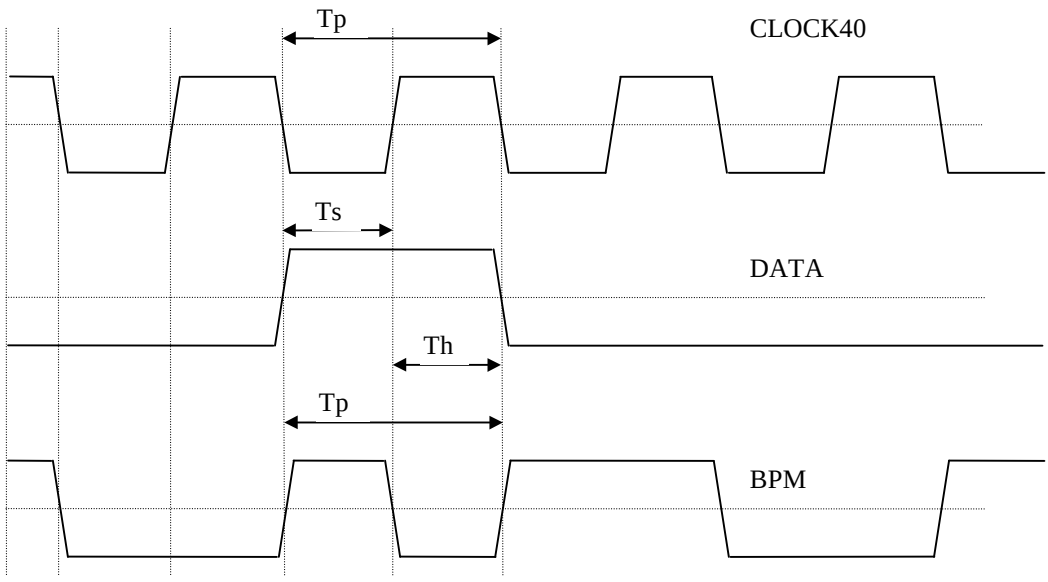


Figure 2. Biphase Mark encoded Clock & Data

4.1.3 General Requirements

1) BPM must be able to delay the input L1 trigger data by up to 32 clock cycles (CLOCK40), and the input ATLAS timing clock in 1ns steps up to 25 steps. The delays will be programmable and setup via a serial interface.
2) Each VCSEL driver output stage will have its own ground return.
3) The device must have separate Digital and Analogue supplies.
4) The BPM will be required to work at ambient temperature in during test and up to a maximum of 70°C when in use on the experiment.
5) Supply voltages nominally +5V for input and output stages.
6) All bond pads must have ESD protection to IEC 801-2 compliance or higher.

4.1.4 Physical Requirements

1) Bond pads or manufactured minimum size requirements should determine chip size.
2) VCSEL driver connections at one end.
3) Digital connections at the other end.
4) Package to be JLCC68.

4.2 Construction and manufacturing

The circuitry will be designed using AMS 0.8 μ CMOS process.
Submission: ???

4.3 Evaluation, testing and product control

The evaluation and test will proceed in three phases
1. Electrical functionality tests
2. With BPM driving HFE 4080 VCSELs the optical output will be measured with an optical probe and the signals compared to the specifications in Table 2.
3. With BPM mounted on the Clock & Control board, TTC data will be sent to DORIC4 mounted on an optoboard together with a GEC package with a fast epitaxial Si PIN diode. The SEQI and LITMUS modules will be used to perform BER tests.

R. Wastie, G. Noyes, D. White, I. Mandic and A. Weidberg, will decide the detailed program of test at a future date.

4.4 Shipping and installation

All work at NAPL Oxford.

4.5 Maintenance and further orders

None.

5.0 Project Organisation

5.1 Personnel

Project manager:	R. L. Wastie	r.wastie1@physics.ox.ac.uk
Originator:	A. R. Weidberg	t.weidberg1@physics.ox.ac.uk
Financial Responsibility:	R. Nickerson	r.nickerson1@physics.ox.ac.uk
Engineering:	R. L. Wastie	r.wastie1@physics.ox.ac.uk

5.2 Milestones

- Preliminary Design Review (PDR) to confirm project Specification. Early April 1998.
- Interim Design Review (IDR) to review progress. Late ??? 1998.
- Final Design Review (FDR) to confirm the device as designed meet requirements of the Project Specification, including any change orders. To be arranged two weeks before submission, ??? 1998.
- BPM chip Submission ??? 1998.
- Concluding Review (CR) and Maintenance Review (MR) after delivery.

5.3 Deliverables

- Project documentation.
- 10 untested packaged dies

5.4 Project plan

See Appendix

6.0 Required Resources

6.1 Manpower

6.1.1 Research Staff

R. L. Wastie Chip design 18 man/weeks

6.1.2 Post-Docs

I. Mandic for testing.

6.1.3 Nominated Technical Staff

None.

6.1.4 Design Office

None.

6.1.5 Computing

None.

6.1.6 Mechanical Workshop

None.

6.1.7 Central Electronics

None.

6.1.8 Building Services

None.

6.1.9 Physics Photographic Unit

None.

6.2 Laboratory space

One chip design seat room 468, week xx-xx

6.3 Existing equipment

Chip Design Sun Workstation and software.

6.4 Cost estimate (excluding Vat)

6.4.1 Capital

None.

6.4.2 Consumables

MPW run with Europractice for prototypes for 10 packaged dies	????	
Total		???

6.4.3 Travel

CERN trip	£500	
Total		£500

6.4.4 Training

None.

6.4.4 Other costs

None.

7.0 Training

None.

8.0 IPR and confidentiality

No additional IPR or confidentiality requirements beyond standard University of Oxford policy.

9.0 Safety

Low voltage, low current circuitry, no particular hazards associated with this project.

10.0 Document Control

All documentation will be archived according to the ATLAS Document Management Protocol. All documents will be kept for the lifetime of the ATLAS experiment.