

5-Sep-2002

Review Committee Report
for the SCT & Pixel ROD US-ATLAS FDR of 20-Aug-2002

Introduction:

A Final Design Review of the Read Out Driver (ROD) intended for use by the ATLAS SCT and Pixel subsystems was held at LBNL on 20-Aug-2002. The primary intent of this review was to evaluate the present status of the ROD design for use by the SCT and Pixels with a goal of approving the build of 9 pre-production RODs so that further user evaluation can be obtained prior to a Production Readiness Review (PRR) as early as possible. While the goal is for the ROD design to be compatible for both SCT and Pixels, it is recognized that there has been as yet no user evaluation of the design with Pixel readout. Given the schedule constraints of the SCT and the overall cost constraints of the project, the plan is to evaluate the appropriateness of the present ROD design for both SCT and Pixels and decide on the pre-production build knowing that further design modifications may be needed for Pixels after appropriate user evaluation is completed with that readout.

Participants:

The review committee included:

Christopher Bebek – LBNL
Kevin Einsweiler – LBNL
Alex Grillo – UCSC
Henrik von der Lippe – LBNL
Abe Seiden - UCSC

Presenters from the ROD design team included:

Doug Ferguson – Wisconsin
Richard Jared – LBNL
John Joseph – LBNL
Sriram Sivasubramaniyan -
Lukas Tomasek – FZU ASCR, Prague

Presentations:

The design team presented material covering the following aspects of the design:

- ROD Overview
- Implementation Model
- ROD Testing and User Evaluation
- Requirements
- Test Stand Software
- Pixel ROD Status
- DSP Software
- Material Costs
- Schedule

Each presentation was quite detailed with a focus on what had changed in the design since the last design review.

Findings:

Four ROD PCBs have been fabricated and loaded for testing. The following changes have been made since the last design review and implemented in these units:

- Formatter changed to increase link-to-link latency by one clock to make Formatter more robust. Throughput still determined by S-link.
- Router trapping of events for DSP more flexible.
- Controller FPGA code upgraded to have L1ID and BCID counters internal for self-triggering mode of operation.
- The number of back-end DSPs loaded for ROD increased from 2 to 4.

In addition to testing the RODs at LBNL with the Test Stand, one ROD was used at Cambridge in a crate with TIM and partially loaded BOC. The ROD/BOC was connected to one SCT module. Since the SCT-DAQ software was not ready, Test Stand software was used for this evaluation at Cambridge. The highlights of testing and user evaluation include:

- Data path processed events at 100kHz.
- Actual SCT modules have been configured.
- Event data read from SCT modules and sent out over VME.
- Histograms of calibration data have been made in slave DSPs and readout over VME.

While the user evaluation is quite limited compared to what is desired, basic functionality with an SCT module has been demonstrated along with the first example of in situ histogramming of data. No failures were observed.

A small number of changes will be made to the layout of the ROD PCB for the pre-production version. Most have already been implemented in the present prototype version via wire patches. The changes foreseen are:

1. Implement ~10 wire patches in present PCB to layout.
2. Fix stacking of board layers to provided desired ground plane shield.
3. Re-route clocks so they no longer pass under DSP1.
4. Change interface to TIM and BOC (~ 3 wires)
5. Possibly modify footprint for Formatter FPGAs to accommodate an alternate model of FPGA for the Pixel application.
6. Eliminate the 2.5V DC-DC converter since it is no longer needed.
7. Move test points to near front panel at request from UK members of the Off-Detector Electronics Group to facilitate debugging.
8. Add wiring to provide D32 slave access to DSP host interface ports.

VHDL code for the Pixel implementation of the ROD is in progress but not yet ready for testing. At the present time, it is believed that the same PCB layout can be used for both SCT and Pixel RODs, however, in addition to VHDL differences, the following differences will exist in the loaded SCT and Pixel ROD board:

1. Instead of the eight 400/E formatter FPGAs used for the SCT ROD, the present plan for the pixel ROD is to load only four. The BOC design for pixels also assumes there are only four formatter FPGAs loaded. However, this does not provide the desired internal FIFO space in the pixel ROD. There are two possible upgrade options. One involves using eight 200/E FPGAs for formatting. This has the disadvantage that it requires a footprint change from the present BGA676 to a BGA456 package. The other option is to use a 405/EM FPGA, which has 5 times more internal BlockRAM, or a 600/E, which also has significantly more logic blocks. The second option is completely pin compatible with the present layout, but will certainly be more expensive. It should also be verified that the present FlashRAM for the FPGA configuration is large enough to accommodate this change.
2. A 64k deep FIFO for pixels instead of a 4k deep FIFO for SCT for input diagnostic memories in the Data Receiver section of the board. These are pin compatible.

Issues and Concerns:

A small number of concerns came to light during the review. They are:

1. The utilization of four FPGAs (Formatter, Event Fragment Builder, Router and ROD Resource Interface) is approximately 80%. This seems to leave too little room for the possible need for additional functionality given the present maturity of the design. John Joseph stated the following plans to reduce this potential problem:

- a) For Formatter, change many registers to block RAM which should drop utilization to ~70%.
- b) Event Fragment Builder will go down by removing debug code.
- c) Router increased from 48% to 84% by adding more complex trapping. This trapping code can be streamlined to reduce the utilization.
- d) ROD Resource Interface cannot be easily decreased in size but he is very confident that this VHDL code is complete enough that 78% is acceptable.

Another last resort would be to upgrade the Formatter or Event Fragment Builder to an upgraded part at increased cost. A decision, however, to do this would have to be made by the time of the PRR.

- 2. S-link interface has been verified only by use of a logic analyzer at the ROD/BOC interface connector. It has not been tested with a real S-link. Only a prototype S-link board exists and ATLAS is redesigning that board now. The specification of this interface is very simple so that any problem will likely be only a timing issue, which could be changed by a VHDL change to the ROD. There is capability to change the relative phases of the S-link signals by $\pm 90^\circ$, $\pm 180^\circ$.
- 3. The ROD cannot meet the Requirement to read out events via VME at 1kHz with a full crate of 16 RODs. This event rate can be met for one ROD/crate. The source of this requirement was to use the ROD for test beam work prior to the existence of S-link readout to ROB. It is not clear if more than 1 ROD (servicing 48 SCT modules) would ever be needed for a test beam application.
- 4. Due to some strange issue with TI's processing, the FPGAs and the fixed point DSPs need a nominal 1.8V supply while the floating point DSPs need a nominal 1.9V supply. Currently, this is managed by setting the DC-DC converter to 1.85V for all. It looks like there is sufficient margin for all the chips to find an overlap in operating voltage provided the regulation of DC-DC converter is sufficiently tight. An alternative would be to use two DC-DC converters, one for 1.8V and one for 1.9V. Given that the 2.5V converter is no longer needed, this could be converted to a 1.9V device, however, this would require splitting the current 1.85V power plane.
- 5. There is a request to provide test-point access, with test points close to the front-panel, to the "raw" data coming into the ROD from the BOC. This is claimed to be needed to study the timing of the data, and so it is requested that data is available before synchronization with the 40MHz crossing clock.

Recommendations:

The committee was impressed with the amount of work accomplished since the last review. Basic functionality of the SCT ROD has been shown along with the first examples of on-board histogramming. While more user evaluation is still needed to be

sure that the ROD meets all requirements for SCT and Pixels, this is at least a good start. The major obstacle to such evaluation is software for a DAQ system and focused attention of users running the ROD through all its necessary operations. User evaluation of the Pixel version is awaiting a Pixel module to readout.

The committee makes the following recommendations to the ROD design group:

1. It is clear that the ROD development is ready to proceed to implement all identified design changes into a new PCB layout. Also, more ROD units will enhance the chances to obtain more, much needed, user evaluation. Therefore, the committee strongly recommends that the design group proceed as quickly as possible to complete layout of the next version of the ROD PCB and fabricate sufficient boards to eventually load 9 boards. Given the changes to be made to the layout, we recommend that initially only two boards be loaded and tested. The committee at first thought that only one should initially be loaded for testing but we have accepted the advice of the ROD design team that the initial debug of two boards facilitates diagnosis of problems by having two samples to compare. Once basic functionality is demonstrated, the remaining 7 boards can be loaded.
2. The alternate footprint (BGA456 in addition to BGA676) for the Formatter on pixel boards should not be executed. We believe that this creates too big a risk in the layout for an option that may not be needed or used. If the planned Formatter FPGA proves to have insufficient performance for the Pixel readout, one of the higher performing FPGAs with the same footprint can be utilized (405/EM or 600/E). The added cost in that case is a worthwhile risk instead of the risk to the layout now.
3. The allowable power supply margins of the FPGAs and DSPs should be analyzed vs. the regulation spec of the DC-DC converter over the temperature and supply range expected for the board. If it is not convincing that a single supply will work reliably for long-term use, the power plane should be split and two DC-DC converters should be employed. While splitting the power plane does imply some risk, care at this time to avoid errors may be a better risk than possible reliability problems over the lifetime of the ROD.
4. Attempt to optimize the FPGA VHDL code as planned to reduce the utilization. At the time of the PRR, the utilization must be reviewed again. If it is still uncomfortably high to accommodate possible needed enhancements during commissioning, a decision will have to be made then to upgrade to the high cost FPGA.
5. A discussion should be held with the person now re-designing the S-link board for ATLAS reviewing the ROD's S-link interface vs. those of the S-link to confirm that there are no compatibility issues.
6. There seem to be legitimate concerns about how the detailed phase of the data streams from the on-detector electronics will be monitored and timed relative to the TIM-generated crossing clock. Since the BOC is the module responsible for this synchronization, it is suggested that this is the correct place to implement monitoring of the timing of the "raw" data streams. The SCT/Pixel off-detector design group should consider how this may best be implemented in the final system. However, we suggest that the pre-production RODs should simply

- provide a reasonable number of header-based test point, close to the FPGAs, for logic-analyzer analysis, but should not attempt to provide multiplexed front-panel access to the full set of input data streams
7. Since the current ROD design does not meet the requirement to readout events via VME at 1kHz with a full 16 RODs/crate and it would require a major redesign to try to accomplish this, but it appears that one ROD/crate would be sufficient for any planned ROD use, the committee recommends that this requirement be changed to “VME readout at 1kHz for 1 ROD/crate.”
 8. The SCT community is strongly urged to devote more resources to write the necessary DAQ software so that more detailed user evaluation can be performed. To expedite this work, it is recommended that one of the existing RODs be sent immediately to Oxford to allow that group to begin learning to use the ROD.

The committee wishes to thank the ROD design group for their time preparing for this review and presenting a clear status of the project. Those members of committee who are members of the ATLAS collaboration would also like to thank Christopher Bebek and Henrik von der Lippe for their contribution to ATLAS by spending the time to review this complex development.