

Dick,

I append below the unedited and unexpurgated comments from the reviewers at the BOC-ROD-TIM review of July 31-August 1. I would like to congratulate you and the rest of the UK and US team for their efforts and hope that the review was useful.

I will not try to summarize the many comments given below but there are a few key global items that should be addressed. These are listed below with my guess as to the approximate dates for resolution of the given issue. Please let me know if there is substantial disagreement from your end.

1. The BOC-ROD-TIM team should plan on an integrated ATLAS FDR by February 2001. An integrated schedule should be part of this review, and thus should be available for internal review in the US and UK by early December at the latest.
2. Having test results from all of the BOC-ROD-TIM, particularly together, was deemed very aggressive to meet the February FDR schedule. An integrated test plan, with responsibilities assigned, should be developed immediately so that it can be reviewed by the appropriate SCT, Pixel, UK and US entities by the end of September.
3. The SCT need for BOC-ROD-TIMs is substantially in advance of the current Pixel schedule and there is some risk that freezing the design too early, necessary for the SCT, may cause problems for the Pixels. This needs to be addressed directly in the integrated schedule, by a combination of sufficient design flexibility and/or phased fabrication.
4. Finally, the goal to complete the fabrication and testing of the RODs (and probably the BOC and TIM but need integrated schedule) by early 2003, practically guarantees that some parts for these items will be obsolete by the time of commissioning in 2005 or so. There should be a clear proposal how to handle this situation for the February FDR with a final proposal to be ready by the ATLAS PRR.

Gil Gilchriese

### **Comments on Off-Detector Electronics Review 31-Jul/1-Aug-2000**

Alex Grillo

The two-day review of the entire Off Detector Electronics System was very informative and provided an excellent opportunity for interaction among the developers, a small subset of the users and the outside reviewers. The developers come from four institutions from the UK and the US and have demonstrated a very satisfactory working relationship in spite of their large geographical separation. The team has the technical expertise to compete the development work and deliver the needed equipment. The presentations and the documentation made available show a good understanding of the requirements and much effort in designing the necessary hardware and software.

The documentation provided includes most of the necessary information, however, the format and organization of the documentation appears not to be as consistent across all components of the system as it could be. This is probably a result of the different working styles of the different groups as anything else. None the less, the result is that it is sometimes difficult to find specific details about all components. Given the available manpower and the tight schedule in the near term, it is not clear that the group should expend a large amount of effort now to improve this condition. However, it would be good to make the Requirements Document for the TIM and BOC more quantitative. This will facilitate demonstrating that the requirements have been met in the system testing phase and documenting that success for the PRR. Also, it will be necessary before the completion of the development work that the documentation be

brought into reasonable conformity so that the system can be maintained properly over the many years of operation.

The following comments are mostly specific details about what was covered during the two-day review.

*Testing:*

It became clear during the review that it will not be an easy task to test all of the components in the ROD crate in fully realistic conditions. One ROD crate services such a large number of detector modules that there will not be enough detector modules in existence to connect a full complement of modules to a ROD crate, not even a full complement for one ROD/BOC card, until much later than the planned FDR. The Off Detector Electronics Group has started to think about this problem and is brainstorming possible ways to work around this problem. One approach that was discussed would be to develop some device which emulated a large number of detector modules thus responding as a real module to commands from the ROD/BOC and furnishing large amounts of data to the ROD/BOC. This may require a substantial amount of development work and it is not clear sufficient manpower exists to complete it on schedule. The group is encouraged to look at alternatives which could test all the requirements of the ROD crate in a more piecewise fashion. A plan should be developed that outlines how each element of the combined TIM/BOC/ROD requirements can be demonstrated prior to the PRR. This could specify a different test for each element of the requirements even though no one test set up emulated the entire SCT or Pixel environment.

*L1 Latency:*

There is a time budget for each component. The design of TIM, BOC and ROD indicate that they will meet their budget maximum. It would be good to confirm that with simulation. Otherwise, we will not know until tests at the end of the year.

*Periodic Reset:*

Need to make sure that the data path exists for the ROD supervisor to know when a periodic reset has been requested by TTC. This will allow us to build in the capability to re-configure some or all FEE ASICs on that key.

*FEE ASIC Reconfiguration:*

SEU measurements are starting to be made on the FE ASICs. As expected the rate is non-zero. We need to start a dialogue between FEE group and Off-Detector Group to develop a plan on how/when to reconfigure FEE ASICs: on demand when problem found, periodically, both. Will depend upon the SEU rate in critical registers and on the time needed to reconfigure.

*Temperature of ROD PCB*

Temperature sensors on the ROD PCB will trip at over temperature. Not clear what temperature the "hot" ICs will be at that point. Need to measure IC package temperatures at PCB trip point and make sure this is below spec limit for packaged ICs.

How will the RCC know that a ROD has tripped off due to temperature?

Is an oscillation mode possible whereby the ROD trips off for over temp and then comes back on-line once cool down occurs only to trip again? If this happens, can the RCC somehow shut down the ROD?

*ROD Cost:*

The new pricing from Xilinx seems to indicate they are favoring their new products and discouraging older ones. We should determine if some of these older products which are designed into the ROD are going to be obsoleted soon. If so, we need to plan accordingly with larger/earlier buys or designing in another part.

*Schedule:*

It appears that schedule has slipped approximately 6-8 weeks since we last looked at it. The reviewers strongly urge that the group try to keep to the schedule of having the FDR in approximately Feb-2001. Every effort should be made to complete the system test in the UK by the end of this calendar year and to start User Evaluation by the start of 2001. This will allow results from both of these to be reviewed as part of the FDR in Feb-2001.

We need an integrated schedule for all components of the Off Detector Electronics showing activities through the completion of production units. This should include when the seven BOC0 units will be available.

One potential delay, which the Off Detector Group has no control of, is the availability of BPM12 and VCSEL12 parts. The time they are needed should be clearly marked on the integrated schedule so it can be tracked with the Links Group.

*Planned FDR & PRR:*

The future FDR and PRR should continue to include all components of the ROD crate: TIM, BOC, ROD, RCC and ROD Crate.

*Operating Environment:*

Add expected operating environment (e.g. temperature, radiation) to requirements of TIM, BOC, ROD (It might already be in the ROD requirements.)

*BOC Command Delays:*

Quantify in the BOC Requirements the delay range for commands.

*SLINK Interface:*

It should be made clear to the ATLAS DAQ Group that we plan to use the mezzanine SLINK card and that the electrical interface, connector and formfactor of that card must be frozen at the time of the Off Detector FDR (i.e. Feb-2001). We should have sign-off by someone in ATLAS-DAQ for that.

*BOC VCSEL Interlock:*

A feature should be added that will allow diagnosis of a broken switch (broken in the closed state) on the VCSEL backdoor. Otherwise, the interlock could be compromised. This may have to be coupled with some maintenance procedure to test opening and closing the door.

The common buss with pull-up OR on each card is not fail-safe. Needs to be fixed.

Need and electrical spec for the output of the "Laser Interlock Control" box such that DCS can buy-off. It would be good if there was some way for the RCC to know the status of the override switch.

*RCC Software:*

It is not clear what software is needed in order for the Off Detector PRR to be completed. The RCC Software development should be included on the Integrated Schedule. It appears that there may be a manpower shortage in this area. Some estimates should be made of what is needed and then discussed with the SCT Steering Group if there is not sufficient manpower within the Off Detector Electronics Group.

*VME Addressing:*

There was a point raised near the end of the second day regarding VME addressing of the 3 different modules (TIM, BOC, ROD) and it sounded like there was a question as to whether all modules in the crate were using the same addressing scheme. It was too late in the day to discuss this further but it should be clear that all modules are using the same addressing scheme for compatibility.

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From Chris Bebek  
High level concerns

ROD simulation of controller section is not ready to help commission first board.

The new issue of a potential high SEU rate in the front-end IC's needs to be absorbed by the SVT group and a statement that the present ROD configuration scheme is flexible enough to deal with this.

Pixel anxiety about signing off on ROD without some relevant test procedure.

BOC1 component availability.

BOC2 schedule and component availability.

TIM design seems to be still in flux even as PCB are being fabbed.

ROD/BOC/TIM/Module test before February FDR will be tough to meet.

ROD

Latency

Latency is being tracked and is under control. There is about 15% contingency within the SVT system if the "inner cable routing" is used. I did not understand if this contingency is different for the pixels. An additional contingency not relied on is a slanted path to the counting house as used by some part of the trigger.

ROD PCB

The issues raised at the May PCB review were mainly addressed and the board is due in 10 days or so.

#### Simulation

To test some of the event data paths, special VHDL code may be developed to test board and assembly integrity. Simulation of the formatter/fragment builder/router is under way and some problems have been exposed and fixed. An unexpected pipeline latency has been found in the router and will be addressed as time permits. It is estimated that this part of the simulation is 75% complete. Simulation of the logically more complex controller section has not begun. This is unfortunate since this section of the board is required to function early in the debugging process. It is noted that this is to be the next area to simulate.

#### Requirements

The requirements document is stable. A new potential issue arose regarding the necessity to reset front-end ICs if SEU rate is large. Presently the ROD can send two independent configuration patterns to any combination of front-ends in parallel with data taking. If each front-end requires a unique configuration pattern and SEU's need to be dealt with by periodic resets as opposed to dealing with each individual occurrence, a lengthy deadtime may occur. Granted, the SEU issue is new and may not persist, the SVT system needs to monitor this issue and understand its impact on the ROD design.

#### Crates

ATLAS-wide crate and rack specs are not finalized but the ROD/TIM/BOC requirements seem to fit well within the parameters that are being discussed.

The ROD/TIM/BOC backplane specs have been finalized and boards are due in November.

#### ROD power density

The ROD power is 82W worst case, probably 62W typical. One reviewer was concerned about a 10W hot spot spanning several square inches. This is not atypical of VME CPU modules and I do not share this concern.

#### DSP software

This seems to be well advanced. The host-masterDSP and masterDSP-slaveDSP communication protocol is done and in fact is done very symmetrically. I like the attention paid to communicating error messages to the host. How to handle these error reports is still in development. A question asked by one reviewer is whether each error condition is assigned an ATLAS-wide number code to make error interpretation easier when ATLAS is an operating experiment. This sounds like a good idea but it also seems that ATLAS DAQ is not advanced enough to have a policy in this regards.

#### Test stand

Software is impressive. It is hard to anticipate if it will meet the demands of the board debuggers, ie, how flexible and easy is it to execute new sequences of commands.

#### ROD test plan

A sequence of steps for commissioning the first ROD board was presented. It seemed to progress logically from the VME interface to greater board depths such as booting FPGA's and testing memories and data paths. As mentioned above, special VHDL code will be developed if time permits, certainly if problems arise, to test the connectivity of the FPGA's and memories.

Offline, I heard that a trivial BOC card will be fabricated that allows 48 channels to be used as output through the backplane pins to the inputs of the 48 other channels. For what it is worth, I offer the suggestion that this board be elaborated to include some logic to test the BOC control and S-link interfaces.

#### Data source emulator

It is unfortunate that the need for this device was not anticipated earlier. I can imagine that the ROD is going to want to be testing the BOC interface not too long after arrival of the first board. A data source using a large collection of existing modules can emulate the entire the electrical-optical paths from front-end IC's to the BOC with the exception of the interaction of front-end configuration registers with the "data stream." This system looks like it would be expensive to replicate for multiple sites. In my opinion, at the minimum, a memory-based LVDS pattern generator should be bought, stolen, or built.

#### Cost

The ROD cost is stable at the 10% level.

#### ROD Schedule

10 Aug 3 PCB's arrive  
01 Sep 1 partially populated board arrives for testing  
01 Oct earliest date for boards 2 and 3  
Nov Boards available for integration with BOC  
??? Success determines acquisition, population, and testing of board 4-10

#### Pixel anxiety

No pixel specific VHDL code exists to "prove" that ROD can deal with pixel issues. Einsweiler asked how can ROD get through a February FDR without this crucial input. In the end, the answer seems to be, "Too bad. If a different ROD is needed by the pixels it will be developed when the pixel system is stable."

#### BOC

The BOC is a board that is probably very dense. We did not see a layout and I cannot really say how difficult this is going to be to debug. The board contains custom ICs provided by other ATLAS groups and there seem to be enough to get three BOC's populated to a partial level but after that it is unclear when additional part become available, e.g, BPM4 die may be available but they are not packaged (or tested?).

There was some concern that BOC2 would be a major iteration of BOC1. It seems to me that all the changes occur within 50 mm of the front panel where higher density BPMs and VECSELS replace lower density ones.

A check should be made if the BOC "idles" in the right state if its corresponding ROD is unplugged.

BOC1 will provide a small number of channels that can be operated in the 80 Mbs mode required by the pixels. Hopefully this will address some of the pixel group's concerns.

#### BOC laser interlock

There was much discussion of the interlock mechanism whereby fibers from the on-detector electronics are disabled if unplugged at the BOC. It seems to me that the design is being driven by anticipation of what may be required instead of being driven by requirements from the group designing the remote laser power supply.

#### BOC1 schedule

7 August - PCB is being quoted and will be order around.

18 August - The PCB should return on.

September - A partial population can be started immediately following. Additional components are due. A VME board to exercise the "setup bus" is in fab. SLOG and MUSTARD boards are being collected for optical link testing.

October - One fully populated board is to be available for ROD testing. Four more partial boards will be available on a similar time scale.

#### BOC2 schedule

unclear

#### TIM

TIM is designed and in fab. (Personal comment, if ever a design should be done in one large FPGA, this is it). The implementation is smallish CPLD's which can be individually simulated but their interaction cannot. The commissioning may take some time as the IC interaction are not simulated. There is discussion about future incorporation of deadtime statistic accumulation per ROD. Fox pointed out that this might be doable with unused resources on each ROD. Another future change to the design is to mount the TTRx logic directly on the PCB instead of continuing with an "ATLAS standard" daughter board. I do not understand the motivation for this.

It was stated that a switch is used to set the board base address. From the discussion that followed it, seems that the ROD used the nGA lines on the backplane to establish the board base address. It did not sound to be strictly VME64x compliant, but it will work fine. The TIM should do what the ROD does so that there is no confusion later on with TIM encroaching on ROD address space due to a mis-set switch.

#### TIM schedule

7 October - Two TIM boards are thought to be available.

#### Integration schedule

As everyone has observed, I do not have a clear picture how all these components come together to be approved at the FDR and PRR level. Nominally, things will come together for the first time in December. In January 2001 (?), front-end modules will be connected. Aggressive is the word that describes this plan.

From jdfox@SLAC.Stanford.EDU Fri Aug 18 17:16:42 2000

Date: Tue, 15 Aug 2000 14:40:53 -0700 (PDT)

From: John D. Fox <jdfox@SLAC.Stanford.EDU>

To: Murdock Gilchriese <gilg@lbl.gov>

Cc: rhminor@lbl.gov,

Alex Grillo <grillo@scipp.ucsc.edu>

Subject: Re: ROD review comments

Here's my (belated) comments - again I thank everyone for their efforts, and our hosts for the hospitality.

John

Date: 5-26-2000

To: ROD Reviewers

From: John Fox

Subject: Thoughts from the 7/31/2000 LBL ROD-BOC-TIM Review

Here's the notes I made during the review we had on Monday and Tuesday

7/31 and 8/1.

Overall - This was my first opportunity to see the functions of the BOC and TIM, and I appreciate the efforts of everyone to explain the overall signal flow, and the interplay of the various functions.

ROD - The prototype cards are in fabrication, and while the state of board level simulation is not very complete, I think that concentrating a significant amount of the design groups' resources on testing the prototypes, and figuring out exactly what and how to test the prototypes, is critical. The design groups' strategy to use special VHDL test codes, and special test data patterns in conjunction with the on-board diagnostic memories, is sound. But there's a lot to do (even testing just a memory function will require special codes). I think that given the time pressure, and the overall flexibility of the reconfigurable logic, I can support a decision to concentrate on verifying the physical implementation, rather than investing resources on board-level simulations.

BOC - The basic design, and interaction with the ROD, is well-understood. Several possible testing schemes and short-term ad-hoc test modules were discussed. I would offer that given the time schedule, and resources, I would look for test approaches for the BOC which minimized developing any new hardware, and which leveraged as much as possible on the test functions in the ROD which might be used as part of a BOC test fixture. The optical signal paths do deserve some test set that allows some verification of receiver sensitivity - I think there are several possible options.

TIM - the basic module functionality is well-defined, and the proposed design, based on a general-purpose array of MACH PLDs, has so much flexibility that I see little risk that the required functionality (or even expanded functionality, such as the dead-time and BUSY statistics) will not be achieved in the first prototype. I think that the design group has made a pragmatic decision to use the programmable devices supported by the software they run and understand, though they expressed some concerns about availability and support for the MACH devices. I think trying to consider alternate implementations is going to have a schedule impact - I'd urge proceeding with the prototype development, and pragmatically expediting a lifetime buy on the MACH plds to insure the boards can be supported in the future years. As I understand the production module numbers, the TIM module is required in much smaller volume than the data processing BOC-ROD modules. As such, I think there are good reasons (and little cost or downside) in just stocking up on the required logic for the entire production to insure availability.

As these individual designs exist as functioning prototypes, it will become increasingly important to build up a complete set of TIM-BOC-ROD processing, and prove the system-level functionality. This is going to be difficult, given the geographical separation of the development teams, schedule uncertainties on the components of the physical detector to provide real input signals, etc. Because of these issues I think a commissioning czar needs to be designated now, and some sort of commissioning plan and schedule, defining who and where what is going to happen when, needs to be sketched out. This realistic commissioning plan needs to be developed now to insure that the schedule implications, and test requirements, and manpower needs can be foreseen before they become obstacles to a timely successful completion of the prototype testing, and approval for volume production of the full detector requirements.

Once again, I want to thank all the presenters for the care and effort

that went into the presentations. I look forward to hearing of future progress.

From premisler@bnl.gov Fri Aug 18 17:07:56 2000  
Date: Wed, 09 Aug 2000 11:32:21 -0400  
From: Lawrence Premisler <premisler@bnl.gov>  
To: Gil Gilchriese <mggilchriese@lbl.gov>  
Subject: ROD-BOC-TIM Design Review Comments

Hi Gil,

Enclosed are my comments to the subject review.

#### General Comments

I was impressed with the amount of good work that was accomplished over the past months with the ROD system. Under the leadership of R. Jared, the ROD team has obtained the sufficient manpower and management structure to organize and complete most of the scheduled detailed tasks in a timely manner. The BOCC, TIMM, and RCC tasks are proceeding at a much slower pace because of poor program planning and lack of manpower.

I noticed a weakness in the coordination between the ROD (US ATLAS responsibility) and the BOC/TIM/RCC (ATLAS responsibility) subsystems. In order for the ROD to proceed into the production parts procurement phase, scheduled for June 2001, the various subsystems (ROD, BOC, TIM and RCC) of the Off Detector Electronics have to be integrated and tested as a subsystem. The date for this to be completed is uncertain because of the lack of a system test plan, and schedule coordination between these two groups. The system test plan should be generated by the two groups as a high priority item. I am recommending that a "centralized" schedule be generated between the groups, that all groups will "sign" up to, and coordinated by a single individual. It was not clearly defined at the review when the BOC/TIM/RCC is scheduled to start production. This date should also be incorporated into the "centralized" schedule.

#### Specific Comments

##### SCT Latency

The 10% contingency on SCT latency is probably not sufficient at the paper design stage. The latency contingency will most likely degrade due to problems encountered at the prototype and production phases of the program.

##### ROD Requirements

The preliminary compliance check list should be reviewed and updated if necessary to make sure that all ATLAS and Interface requirements are met before starting the prototype stage of the program.

##### All Subsystems

There should be an effort to try to increase the number of spare pins on each connector to allow for future changes. There were some connectors that have 0 spare pins.

##### ROD Power Utilization

Evaluating the board layout from a thermal point of view, indicated that



there could be a reliability problem with the two adjacent components that dissipate 5 and 5.5 watts respectively. There is a need to look at the junction temperatures of these devices and to use either conductive or convection cooling or a combination of both to reduce these temperatures. A thermal analysis should be taken to calculate the expected chip temperatures before the prototyping stage.

#### ROD Software Primitives

The completion target date should be defined as a milestone and entered in the ROD internal schedule if this item is on the critical path.

#### ROD Test Plan

Because of the complexity of the the pc board, the pc board fabrication may introduce shorts and or opens in the traces. The shorts and or opens will have to be detected before the boards are populated to eliminate board assembly scrap due to a trace short or open of these expensive board assemblies. The pc board vendors should be explored with the way they check for these items as a function of cost and "thoroughness" and a decision made based on the thoroughness of picking up shorts and opens versus cost of the pc board assembly and not of the pc board fabrication.

Develop two test and shipment plans for prototype and production that include diagnostics. What was presented is probably adequate for prototyping but may not be for production. The production plan should be generated after the prototype test has been completed to learn from the prototype test results.

#### BOC Requirements

The specification should define the operating environment (temperature etc.).

#### Optical Laser Safety

If one of the two micro switches provided for fail safe operation fails, there should be some visual indication with corrective action to prevent a safety hazard condition should the other one fail.

#### SCT DAQ Status & Schedule

The target date for selecting the processor should be defined and be compatible with the the "centralized" schedule. The target date for this was defined at the meeting as the summer of 01.

#### TIM Schematic & Layout

Calculate the board hot spot temperature and determine if there is a reliability problem before the prototyping phase. If this is not done and if there is a problem, the layout will probably have to be changed and another prototyping run will have to be made that will impact schedule and cost.

#### TIM Schedule

In order for the ROD to start production, what is required by the TIM to insure that there will be no interface problems?

From rhminor@lbl.gov Fri Aug 18 17:08:12 2000

Date: Thu, 10 Aug 2000 15:36:49 -0700

From: minor <rhminor@lbl.gov>

To: Murdock Gilchriese <gilg@lbl.gov>

Subject: Re: ROD review comments

Gil,

Comments of Atlas review 7/31--8/1/00

Your general comments made at the close out were good and covered the 'global' issues.

Some details from 7/31.....

- 1) Presentations were excellent, informative, etc..
- 2) Designs are good, but there are still lots of details to sort out including:
- 3) ROD card over temperature monitor needs to be read out remotely- not just as an led on the card.
- 4) A comparison of the performance of all the cards presented should be made against the requirements documents and other known but not documented requirements. Other implied requirements should be incorporated in the formal requirements document.
- 5) A thermal analysis and/or temperature measurements in the high power area of the ROD need to be made.
- 6) Details of the testing of the prototype pc cards prior to loading should be reviewed and a short description made available to the review committee. Clearly, testing of the board integrity prior to loading is essential. A determination is needed of how complete the tests will be that will be performed for prototype and for production.
- 7) Details of the assembly/rework procedures for the partial loading need to be finalized. The BGA assembly process needs to be defined.

from 8/1/00

- 1) A formal interface document describing the Pixel datastream is needed.
- 2) The laser interlock system needs to be analyzed ( and probably modified) to make it failsafe.
- 3) The long term availability of the MACH parts needs to be evaluated. If they are hard to get now, will they be available for production, and will large number of spares be needed?

Bob

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XX

Bob Minor

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From Abe Seiden

Here is my contribution regarding single event upset. I don't have any technical contributions which are mostly in good shape and I certainly agree with the general conclusions which discussed at the closeout.

It is recommended that the ROD group and frontend group appoint an individual each to carefully examine the issue of single event upset. Some of the questions to address:

- 1) What are the possible things that can happen to the frontend. What is the meantime for each problem type.
- 2) Will the ROD system catch all problems? How long will it take to do so and correct the situation? Are we optimally setup to make all corrections?

The result of the study should be a brief document that can be used to compare to when we start data taking. Note, the down-time per chip needs to be much less than  $10^{-4}$  as a time fraction.