# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Components of the Off Detector Electronics**

**Back Of Crate (BOC) card (optical interface), Cambridge**

**Read Out Driver (ROD), Wisconsin**

**Timing Interface Module (TIM), University College London**

**Crate Backplane, Oxford**

**SCT DAQ, Cambridge**

**Pixel DAQ, Iowa State**

## SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Current efforts are to debug the prototype of the three cards (BOC, ROD, TIM) and fabricate and install the crate back plane.  Good progress has been made but the schedule has slipped.**

**The scheduled slippage has caused the following dates to slip.**

| | was | is |
|---|---|---|
| **Cambridge ROD Crate Test** | **5/1/01-1/3/01** | **23/2/01-1/6/01** |
| **CERN System Test** | **13/3/01-5/4/01** | **5/6/00-15/7/01** |

**The new scheduled dates look quite good.  The largest uncertainty is with the ROD debugging.  The card is complex. This results in uncertainty with the debugging time estimate.**

**Overall the progress of the Off detector electronics has been good and the prototypes will be working in a few months.**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Off Detector Test Schedule:**

**Resent successes in debugging cards leads to the following schedule:**

**Feb. 23, 01 First test of crated backplane power (Oxford)**

**Mar. 5, 01 Test of TIM with backplane and crate (Cambridge)**

**Mar. 12, 01 Test of BOC, TIM and backplane (Cambridge)**

**Mar 26, 01 ship ROD and test equipment toCambridge.**

**Apr. 2, 01 Start of testing with ROD (Cambridge)**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the BOC:**

**Accomplishments:**

| | |
|---|---|
| **Old** | **The prototype design has been completed.** |
| | **Down loading of settings into the delay chips has been tested.** |
| | **Request for packaging of BPM4 chips (4 in hand) has been made .** |
| | **Test Card for VME r/w to BOC bus PC card has been fabricated.** |
| | **Three ROD crates have been received.** |
| | **Parts are available for the prototypes.** |
| **New** | **The control paths are working.** |
| | **Mitel can not take orders for optical parts. They are working on production details. We will have to make do with the in hand devices for prototypes. Not a serious problem.** |
| | **Control and data path functionality is just starting to be explored.** |

## SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the BOC Continued:**

**Accomplishments: continued:**

**New In a bit more detail:**

**1) VME <> BOC-RIG(VME test card to r/W BOC) - OK**
**VME <> BOC-RIG <> BOC via SetUp Bus - OK**
**Can load and read-back BOC control registers**
**Can read BOC identifiers (module type, S/N, manufact.,version)**
**Can load a read Variable Clock Control register**
**Can control RX Threshold DACS (sample streams - not all 96 tested)**
**Can control TX Laser current DACS (sample streams - not all 48 tested)**
**Can control RX data delay chips (sample streams - not all 96 tested)**
**BPM internal registers - control signals look OK - action not tested.**

**2) have populated BOC with 1 BPM, 1 VCSEL4 and 1 PIN12**
**just adding SLOG and OptIF modules to the test system to provide test signals for BOC Control and Data streams.**
**Assembling bits of software for these tests.**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the BOC Continued:**

**Prognosis and predictions comment (Feb. 5, 2001 ):**

**Things are going suspiciously well.**

**I didn't foresee this level of progress, so I've given up on the schedule prediction business.**

**Maurice**

**Current work:**

**Control and data path functionality is being explored.**

**Concerns:**

**None**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the ROD:**

**Accomplishments:**

**Old**
- **The design of the ROD has been completed.**
- **Simulation of the ROD is complete with the exception of the resource interface manager that is only 2/3 complete.**
- **Three ROD PC cards have been fabricated.**
- **Two ROD card have been partially loaded.**
- **ROD debugging has started. VME r/w to registers works.**
- **Three crates have been delivered.**
- **The layout of ROD test cards that loop outputs to inputs have been designed and laid out. They are in fabrication.**

**New**
- **VME Read/write via the DSP host port interface to/from DSP program and data memory, SDRAM memory and resource interface FPGA is working. Debugging of the circuitry took about 6 weeks.**
- **Simulation of the resource interface manager continues. It is estimated that 3 weeks of work is required to finish.**

## SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the ROD Continued:**

**Accomplishments continued:**

**Master DSP code has been written**

**Old** **memory map (.h), initialization, process list from RCC state machine, master process list from slave state machine, primitive list handler, interface between master and slave, error diagnostic buffers, transfer text buffer to RCC state machine, readout of slave text buffer state machine, error handling**

**New** **The master DSP code for maintaining communication to the RCC when the slave is processing a primitive is being written. This is the last of the known master DSP code.**

**Primitives code has been written**

**Old** **Echo (diagnostic), R/W field of register or single r/w, r/w block of of data, configure slave DSP (on, off and type (error checking, etc.)).**

**New** **Echo has been tested successfully with the ROD.**

## SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the ROD Continued:**

**Accomplishments continued:**

**The ROD test stand software for initial testing has been written.**

**Windows have been designed that support the following:**

| | |
|---|---|
| **Old** | **VME r/w block (supports create and or store for later use) or single register, Master DSP r/w block (supports create and or store for later use), command and status register r/w (tested), Flash memory r/w (tested), Primitive generation (supports create and or store for later use)** |
| **New** | **Windows have been used to r/w data to the ROD location.** |

**These windows communicate to the following modules:**

| | |
|---|---|
| **Old** | **Buffer handler communicates to ROD( regular r/w, list transfer to DSP, poles and transfers text buffers), Primitive list formatter (format list for transfer to ROD), Reply list processor (check sum, converts data and store/distribute data), Host control (initialization, etc), Text buffer processing (formats data, adds headers and place text in files).** |
| **New** | **Most of the above functions have been successfully used in tests.** |

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the ROD Continued:**

**Current Work:**

**The testing of the ROD is ongoing. It is estimated that the ROD will be functional in 2 month. It is expected that debugging will proceed much faster when simulated VHDL is being debugged.**

**Current work is verification of reading and writing to all control registers and memory on the ROD.**

**Concerns:**

**The ROD is complex. This complexity could result in schedule slippage during the debugging stage. .**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the Crate Backplane:**

**Accomplishments:**
**Prototype backplanes have been fabricated.**
**Backplane test boards have been fabricated**

**Current Work:**
**Test  board are being loaded in 1.5 weeks.**
**Backplane will be mounted in crate in 1 week.**
**Backplane power loading test in 2 weeks.**

**Concerns:**

**None**

## SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the TIM:**

**Accomplishments:**

**Old Two prototype TIMs have been designed, made and delivered to UCL.**
**All CPLDs are loaded and operating, but some need more debugging.**
**Parts are in-hand for 6 or 7 more TIMs; spare parts are ordered.**
**TIM plugs OK into a 9U VME crate (the connectors P1, P2, P3 had to be moved 2.5mm)**
**VME access to all registers and memory is working.**
**Clock and sequencer (ie programmable pattern generator) signals through to backplane is working.**
**New Input and Out puts to from front panel are working**
**Stand-alone signal generators are working ( as well as the sequencer )**
**Debugging is progressing.**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the TIM:**

**Accomplishments continued:**

**Old The TIM is available now to start system testing, (ie output of clocks and sequencer signals to backplane is ready).**

**A TTC system for input to TIM consisting of TTCvi and TTCvx (ie source and transmitter) is working.**

**The TIM printed circuit board itself shows no problems so far.**

**What is to be done**

**Debugging and testing is on-going.**
**Simulation of CPLDs.**
**BCID offset coding.**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**What is to be done, continued:**

**Busy monitor coding.**
**TTCrx I2C interface coding.**
**VME interrupt coding. C**

**Concerns:**

**7 out of 10 CPLDs are not simulated yet.**

**TTC and stand-alone signals need debugging (except sequencer).**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the Pixel DAQ:**

**Accomplishments:**

**Priority has been placed on the ROD DSP primitives.**

**The following primitive have been coded:**

**Old** tell events per burst (number of data word sent to slave DSP from router), mask of events to error buffer (depends on severity), load slave memory (ex. Load code), start slave DSP, halt output (set, reset for block transfer from router, normally automatic), slave get one burst from router (DMA input), slave start data taking from router and slave stop data taking from router, memory test of DSP, flash LED and module histograming

**Have slave DSP stubs for event analysis**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the Pixel DAQ:**

**Current work:**

**Priority is on defining the Pixel DAQ in collaboration with the SCT DAQ.**

**Concerns:**

**The manpower level is low.**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the SCT DAQ:**

**Accomplishments:**

**Old Low level library for TIM written**
**NI-VXI interface + LabWindows + Test Stand Software up and running at Cambridge with 9U crate.**

**Current Work:**

**Looking at detailed changes needed to use the existing SCTDAQ with TIM/ROD/BOC**

# SCT and Pixel Off Detector Electronics Status Feb. 9, 2001

**Detailed status of the SCT DAQ Continued:**

**Concerns:**

**Still a significant amount of work to get the current SCTDAQ into a state that is usable with ROD/BOC/TIM General level of manpower available for SCT DAQ work (and its thinly-spread nature). I mean both the short-term and medium-term in this statement.**