

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization

Change Record		
Date	by	Change
03-May-2000	MJG	Limited distribution as discussion document prior to phone conference on 05-May
09-May-2000	MJG	First general release: +3v3 and +5V available on J3P3, slot compatible power and ground
10-May-2000	MJG	Card sizes, currents, and numbers added at end. Signal classes added to signal summary on Page 3
16-May-2000	RCJ	Added sign off page, 1 bit buss, deleted P0 reference and changed ROD DC power
19-May-2000	RCJ	Added correction from J. Lane. Note TCC and ROD busy active Lo. P5-6 TCC bus terminated on slot 21. P3 row Z changed 3v3 to +5V pins 19-24-29. Updated TIM power for +-12V
22-May-2000	RCJ	Added Crate power to power utilization table, Suggestion of J. Hill
22-May-2000	RCJ	1 Bussed added to table 9 A21 ROD and BOC slots 6-21, corrected typo on -12V power

### Sign off

Name	Subsystem	Date
Roy Wastie	Backplane	16-May-2000
John Lane	TIM	19-May-2000
Maurice Goodrick	BOC	18-May-2000
Richard Jared	ROD	17-May-2000
John Hill	SCT RCC	10-May-2000
Tom Meyer	Pixel RCC	19-May-2000

### Introduction

The back planes provide the interconnection between the ROD Crate Controller (RCC), Timing Interface Module (TIM), Read Out Driver (ROD), the Back Of the Crate (BOC) (optical interface card) and the power supplies. This interface specification defines the assignment of signal and power to the backplane pins. The card utilization of the crate is also defined because this effects the clock and busy signals.

More information on the off-detector electronics can be found at:

<http://www-wisconsin.cern.ch/~atlas/off-detector/off-detector.html>

### General notes:

1. This document is based on an earlier, much modified document, the latest version of which can be found at <http://www.hep.phy.cam.ac.uk/~goodrick/AtBOC/OldBackplane.pdf>
2. All signals are 3V levels, asserted high, unless indicated otherwise. The S-Link signals use a final “#” to indicate active low. Elsewhere, a final “N” is used for the same purpose. In addition, TTC[7:0] and ROD-Busy are active LOW.
3. S-Link UDW[1:0] lines hard wired on BOC. S-Link LRL[3:0] lines not routed.
4. To limit congestion, a maximum of 4 routed signals have been allocated per horizontal row on slots 6-21 of P3J3.
5. The use of series resistors on the outputs of drivers to limit noise generation is recommended for at least some S-Link signals (L-UCLK, L-UWEN#, L-UCTRL#), and for the XC[47:0] (on the ROD) and RD[95:0] (on BOC).
6. TIM, ROD and BOC do not support live insertion.

7. Power pins are used extensively to screen fast signals and to provide good AC return paths; so it is important that they be well by-passed to ground on both ROD and BOC.
8. Tables 8-12 re-present the data given in Tables 5-7 to allow pin usage at different slots to be compared.

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization – Tables and Conventions

Table	Description
1	P1 Connector as used by TIM, Crate Processor and RODs @ Slots 1-21
2	P2/J2 Connector as used by TIM and Crate Processor @ Slots 1-5
3	P2/J2 Connector as used by ROD @ Slots 6-21
4	P2/J2 Connector as used by BOC @ Slots 6-21
5	P3/J3 Connector as used by TIM @ Slot 5
6	P3/J3 Connector as used by ROD.. plugs into Slots 6-21
7	P3/J3 as used by BOC .. plugs into transition (i.e. Back-Of-Crate) slots 6-21
8	P3/J3 Connectors: use of Row Z
9	P3/J3 Connectors: use of Row A
10	P3/J3 Connectors: use of Row B
11	P3/J3 Connectors: use of Row C
12	P3/J3 Connectors: use of Row D

Key to Colours used in Tables for Signal Names	
NC	No Connection
Thru Pin	Through Connection: not bussed
RED	Signal Output
GREEN	Signal Input
BROWN	Bi-Directional
BLACK	Ground/Power
[n]	See Note [n]

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## SCT Off Detector Crate Backplane and Crate Card Utilization – Signal Summary

Summary of Signals					
Signal Group/ Name	Conn.	Description	Direction	Class	
Control	XC[47:0]	P2	Transmit Data	ROD > BOC	LV,Hi,r
RX Data	RD[95:0]	P3	Receive Data	ROD < BOC	LV,Hi,r
SetUp Bus	SD[7:0]	P2	SetUpBus Data	ROD <> BOC	LV,Hi,Bi
	SA[9:0]	P2	SetUpBus Address	ROD > BOC	LV,Hi
	SWRN	P2	SetUpBus Write Line (Lo)	ROD > BOC	LV,Lo
	STBN	P2	SetUpBus Strobe (Lo)	ROD > BOC	LV,Lo
	SBUSY	P2	SetUpBus Busy status line	ROD < BOC	LV,Hi
S-Link	L-UD[31:0]	P2	Link User Data	ROD > S-Link	LV,Hi,r
	L-URESET#	P3	Link User Reset	ROD > S-Link	LV,Lo,r
	L-UWEN#	P3	Link Write Enable	ROD > S-Link	LV,Lo,r
	L-UTEST#	P3	Link Test mode control line	ROD > S-Link	LV,Lo,r
	L-UCLK	P3	Link User Clock	ROD > S-Link	LV,Hi,r
	L-UCTRL#	P3	Link User Control	ROD > S-Link	LV,Lo,r
	L-LDOWN#	P3	Link Failure line (Lo)	ROD < S-Link	LV,Lo,r
	L-LFF#	P3	Link Full Flag (Lo)	ROD < S-Link	LV,Lo,r
Clock Distrib	CLK40+[21:5]	P3	Balanced PECL Clock to BOC slots (+ copy to TIM)	TIM > BOCs	D5vP,Hi
	CLK40-[21:5]	P3		TIM > BOCs	D5vP,Lo
	RCLK40+	P3	Buffered copy of CLK40 for ROD	BOC > ROD	D5vP,Hi
	RCLK40-	P3		BOC > ROD	D5vP,Lo
TIM Signals	TTC[7:0]	P3	Timing, Trigger and Control Bus	TIM > RODs	LV,Lo,T
	ROD-Busy	P3	ROD asking for trigger throttle	RODs > TIM	LV,Lo,l
	TIM-Busy Out	P3	OR of ROD-Busy's	Goes nowhere	LV,Hi
Misc	ROD-sense	P3	Module Mis-Location Interlock	Special	2
	Laser-Ilock	P3	Laser-Access Gate Open on >=1 BOC	BOC >	3

Class Descriptions	
Class	Description
LV	Driver meets or exceeds LV-TTL spec., Receiver can manage with LV-TTL inputs
D5vP	Differential PECL: i.e. ECL running between Ground and +5V. Note 220R resistor to Ground at Driver end: needs 100R between lines at receiver.
Hi	Active HIGH signal sense
Lo	Active LOW signal sense
Bi	Bi-Directional
T	Terminated on Backplane at slot 21
r	Consideration should be given to having a series resistor (of c. 30 $\Omega$ ) at driver end to limit slew rate, ground bounce and EMI.
1	Resistive pull-up on TIM, so empty ROD slot is not seen as BUSY.
2	Pin sensed by TIM and BOC: if HIGH, they disable their outputs. Pulled High by TIM and BOC, grounded by ROD and on backplane at slot 5.
3	Electrical specification for this bussed line is still under consideration.

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## SCT Off Detector Crate Backplane and Crate Card Utilization – Power and Ground Summary

Summary of Power and Ground Pins				
	Connector	# Pins	Description	Notes
Std Gnd	P1	26	Backplane Plane	Not accessible to BOC
Std +3v3	P1	10	Backplane Plane	Not accessible to BOC
Std +5V	P1	3	Backplane Plane	Not accessible to BOC
Std VPC	P1	2	Connected to +5V	Not accessible to BOC
Std +5VS	P1	1	+5v Stand-By conn. to +5V	Not accessible to BOC
Std +12V	P1	1		Not accessible to BOC
Std -12V	P1	1		Not accessible to BOC
Std +V1	P1	1	Ret. For –V1	Not accessible to BOC
Std +V2	P1	1	Ret. For –V2	Not accessible to BOC
Std -V1	P1	1	Nom. 48V	Not accessible to BOC
Std -V2	P1	1	Nom. 48V	Not accessible to BOC
Std Gnd	P2	20	Backplane Plane	
Std +5V	P2	3	Backplane Plane	
Std VPC	P2	1	Connected to +5V	
Std Gnd (ret)	P2	1	Return for VPC: conn to Gnd plane	
Gnd	P2	7	User-Defined (Thru Pins)	
Gnd	P3	22	Backplane Plane	
+3v3	P3	10	Backplane Plane	BOC and ROD use
+5V	P3	8	Backplane Plane	

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P1

**Table 1: P1 Connector as used by TIM, Crate Processor and RODs @ Slots 1-21**

Pin	Row Z	Row A	Row B	Row C	Row D
1	Std Sig	Std Sig	Std Sig	Std Sig	Std VPC
2	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std Gnd</b>
3	Std Sig	Std Sig	Std Sig	Std Sig	<b>Std +V1</b>
4	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +V2</b>
5	Std Sig	Std Sig	Std Sig	Std Sig	Std Sig
6	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std -V1</b>
7	Std Sig	Std Sig	Std Sig	Std Sig	<b>Std -V2</b>
8	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	Std Sig
9	Std Sig	<b>Std Gnd</b>	Std Sig	<b>Std Gnd</b>	Std Sig
10	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	Std GA0
11	Std Sig	<b>Std Gnd</b>	Std Sig	Std Sig	Std GA1
12	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
13	Std Sig	Std Sig	Std Sig	Std Sig	Std GA2
14	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
15	Std Sig	<b>Std Gnd</b>	Std Sig	Std Sig	Std GA3
16	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
17	Std Sig	<b>Std Gnd</b>	Std Sig	Std Sig	Std GA4
18	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
19	Std Sig	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig
20	<b>Std Gnd</b>	Std Sig	<b>Std Gnd</b>	Std Sig	<b>Std +3v3</b>
21	Std Sig	Std Sig	Std Sig	Std Sig	Std Sig
22	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
23	Std Sig	Std Sig	<b>Std Gnd</b>	Std Sig	Std Sig
24	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
25	Std Sig	Std Sig	Std Sig	Std Sig	Std Sig
26	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
27	Std Sig	Std Sig	Std Sig	Std Sig	Std Sig
28	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
29	Std Sig	Std Sig	Std Sig	Std Sig	Std Sig
30	<b>Std Gnd</b>	Std Sig	Std Sig	Std Sig	<b>Std +3v3</b>
31	Std Sig	<b>Std -12V</b>	<b>Std +5VS</b>	<b>Std +12V</b>	<b>Std Gnd</b>
32	<b>Std Gnd</b>	<b>Std +5V</b>	<b>Std +5V</b>	<b>Std +5V</b>	Std VPC

Note that there are no connections to the Back-Of-Crate for P1

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P2/J2

**Table 2: P2/J2 Connector as used by TIM and Crate Processor @ Slots 1-5**

Pin	Row Z	Row A	Row B	Row C	Row D
1			Std +5V		Gnd
2	Std Gnd		Std Gnd		
3			Std Sig		
4	Std Gnd		Std Sig		
5			Std Sig		
6	Std Gnd		Std Sig		
7			Std Sig		
8	Std Gnd		Std Sig		
9			Std Sig	Gnd	
10	Std Gnd		Std Sig		Gnd
11			Std Sig		
12	Std Gnd		Std Gnd		
13			Std +5V		
14	Std Gnd		Std Sig		
15			Std Sig		
16	Std Gnd		Std Sig		Gnd
17			Std Sig		
18	Std Gnd		Std Sig		
19			Std Sig		
20	Std Gnd		Std Sig	Gnd	
21			Std Sig		
22	Std Gnd		Std Gnd		
23			Std Sig		
24	Std Gnd		Std Sig		
25			Std Sig		Gnd
26	Std Gnd		Std Sig		
27			Std Sig	Gnd	
28	Std Gnd		Std Sig		
29			Std Sig		
30	Std Gnd		Std Sig		
31			Std Gnd		Std Gnd (VPC ret)
32	Std Gnd		Std +5V		Std VPC

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P2/J2

**Table 3: P2/J2 Connector as used by ROD @ Slots 6-21**

Pin	Row Z	Row A	Row B	Row C	Row D
1	XC46	XC47	Std +5V	SD0	Gnd
2	Std Gnd	XC45	Std Gnd	SD1	L-UD0
3	XC43	XC44	Std Sig	SD2	L-UD1
4	Std Gnd	XC42	Std Sig	SD3	L-UD2
5	XC40	XC41	Std Sig	SD4	L-UD3
6	Std Gnd	XC39	Std Sig	SD5	L-UD4
7	XC37	XC38	Std Sig	SD6	L-UD5
8	Std Gnd	XC36	Std Sig	SD7	L-UD6
9	XC34	XC35	Std Sig	Gnd	L-UD7
10	Std Gnd	XC33	Std Sig	SA0	Gnd
11	XC31	XC32	Std Sig	SA1	L-UD8
12	Std Gnd	XC30	Std Gnd	SA2	L-UD9
13	XC28	XC29	Std +5V	SA3	L-UD10
14	Std Gnd	XC27	Std Sig	SA4	L-UD11
15	XC25	XC26	Std Sig	SA5	L-UD12
16	Std Gnd	XC24	Std Sig	SA6	Gnd
17	XC22	XC23	Std Sig	SA7	L-UD13
18	Std Gnd	XC21	Std Sig	SA8	L-UD14
19	XC19	XC20	Std Sig	SA9	L-UD15
20	Std Gnd	XC18	Std Sig	Gnd	L-UD16
21	XC16	XC17	Std Sig	SWRN	L-UD17
22	Std Gnd	XC15	Std Gnd	STBN	L-UD18
23	XC13	XC14	Std Sig	SBUSY	L-UD19
24	Std Gnd	XC12	Std Sig		L-UD20
25	XC10	XC11	Std Sig		Gnd
26	Std Gnd	XC9	Std Sig	L-UD22	L-UD21
27	XC7	XC8	Std Sig	Gnd	L-UD23
28	Std Gnd	XC6	Std Sig	L-UD25	L-UD24
29	XC4	XC5	Std Sig	L-UD27	L-UD26
30	Std Gnd	XC3	Std Sig	L-UD29	L-UD28
31	XC1	XC2	Std Gnd	L-UD30	Std Gnd (VPC ret)
32	Std Gnd	XC0	Std +5V	L-UD31	Std VPC



# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P2/J2

**Table 4: P2/J2 Connector as used by BOC @ Slots 6-21**

Pin	Row Z	Row A	Row B	Row C	Row D
1	XC46	XC47	Std +5V	SD0	Gnd
2	Std Gnd	XC45	Std Gnd	SD1	L-UD0
3	XC43	XC44	Std Sig	SD2	L-UD1
4	Std Gnd	XC42	Std Sig	SD3	L-UD2
5	XC40	XC41	Std Sig	SD4	L-UD3
6	Std Gnd	XC39	Std Sig	SD5	L-UD4
7	XC37	XC38	Std Sig	SD6	L-UD5
8	Std Gnd	XC36	Std Sig	SD7	L-UD6
9	XC34	XC35	Std Sig	Gnd	L-UD7
10	Std Gnd	XC33	Std Sig	SA0	Gnd
11	XC31	XC32	Std Sig	SA1	L-UD8
12	Std Gnd	XC30	Std Gnd	SA2	L-UD9
13	XC28	XC29	Std +5V	SA3	L-UD10
14	Std Gnd	XC27	Std Sig	SA4	L-UD11
15	XC25	XC26	Std Sig	SA5	L-UD12
16	Std Gnd	XC24	Std Sig	SA6	Gnd
17	XC22	XC23	Std Sig	SA7	L-UD13
18	Std Gnd	XC21	Std Sig	SA8	L-UD14
19	XC19	XC20	Std Sig	SA9	L-UD15
20	Std Gnd	XC18	Std Sig	Gnd	L-UD16
21	XC16	XC17	Std Sig	SWRN	L-UD17
22	Std Gnd	XC15	Std Gnd	STBN	L-UD18
23	XC13	XC14	Std Sig	SBUSY	L-UD19
24	Std Gnd	XC12	Std Sig		L-UD20
25	XC10	XC11	Std Sig		Gnd
26	Std Gnd	XC9	Std Sig	L-UD22	L-UD21
27	XC7	XC8	Std Sig	Gnd	L-UD23
28	Std Gnd	XC6	Std Sig	L-UD25	L-UD24
29	XC4	XC5	Std Sig	L-UD27	L-UD26
30	Std Gnd	XC3	Std Sig	L-UD29	L-UD28
31	XC1	XC2	Std Gnd	L-UD30	Std Gnd (VPC ret)
32	Std Gnd	XC0	Std +5V	L-UD31	Std VPC

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 5: P3/J3 Connector as used by TIM @ Slot 5

Pin	Row Z	Row A	Row B	Row C	Row D
1	NC	Gnd		+3v3	ROD-Busy6 <sup>1</sup>
2	NC		Gnd	ROD-Busy7	+3v3
3	NC	CLK40+ slot5 <sup>2</sup>	CLK40- slot5 <sup>2</sup>	+3v3	ROD-Busy8
4	Gnd	CLK40+ slot6 <sup>3</sup>	CLK40- slot6 <sup>3</sup>	ROD-Busy9	+3v3
5	NC	Gnd		Gnd	
6	NC	CLK40+ slot7 <sup>3</sup>	CLK40- slot7 <sup>3</sup>	ROD-Busy10	+3v3
7	NC	CLK40+ slot8 <sup>3</sup>	CLK40- slot8 <sup>3</sup>	+3v3	ROD-Busy11
8	NC	CLK40+ slot9 <sup>3</sup>	CLK40- slot9 <sup>3</sup>	+3v3	+3v3
9	Gnd		Gnd	ROD-Busy12	+3v3
10	NC	CLK40+ slot10 <sup>3</sup>	CLK40- slot10 <sup>3</sup>	Gnd	+3v3
11	NC	Gnd		ROD-Busy13	Laser-Ilock <sup>4</sup>
12	NC	CLK40+ slot11 <sup>3</sup>	CLK40- slot11 <sup>3</sup>	ROD-Busy14	Gnd
13	NC	CLK40+ slot12 <sup>3</sup>	CLK40- slot12 <sup>3</sup>	ROD-Busy15	ROD-sense <sup>5</sup>
14	Gnd		Gnd	ROD-Busy16	ROD-Busy17
15	NC	CLK40+ slot13 <sup>3</sup>	CLK40- slot13 <sup>3</sup>	Gnd	ROD-Busy18
16	NC	CLK40+ slot14 <sup>3</sup>	CLK40- slot14 <sup>3</sup>	ROD-Busy19	ROD-Busy20
17	NC	Gnd		ROD-Busy21	+5V
18	NC	CLK40+ slot15 <sup>3</sup>	CLK40- slot15 <sup>3</sup>		CLK40+ _Ret
19	+5V	CLK40+ slot16 <sup>3</sup>	CLK40- slot16 <sup>3</sup>		CLK40- _Ret
20	NC	Gnd		Gnd	+5V
21	NC	CLK40+ slot17 <sup>3</sup>	CLK40- slot17 <sup>3</sup>	Spare 1 bit bus	TIM-Busy Out <sup>6</sup>
22	NC	CLK40+ slot18 <sup>3</sup>	CLK40- slot18 <sup>3</sup>		+5V
23	NC		Gnd		TTC-7
24	+5V	CLK40+ slot19 <sup>3</sup>	CLK40- slot19 <sup>3</sup>		TTC-6
25	NC	CLK40+ slot20 <sup>3</sup>	CLK40- slot20 <sup>3</sup>	Gnd	TTC-5
26	NC	Gnd			TTC-4
27	NC	CLK40+ slot21 <sup>3</sup>	CLK40- slot21 <sup>3</sup>		+5V
28	NC		Gnd		TTC-3
29	+5V				TTC-2
30	NC			Gnd	TTC-1
31	NC	Gnd			TTC-0
32	NC				+5V

Note: TTC-0 to TTC-7 outputs from TIM are bussed to all RODs and terminated on backplane at slot 21. They are active LOW.

<sup>1</sup> These ROD-Busy signals are routed from Slots 6-21, P3J3, pin 21. They are active LOW, LV-TTL totem-pole signals.

<sup>2</sup> This copy of CLK-40 signal is routed to Slot5, P3J3, pins D18 and D19: this path is the same length as CLK-40 signals destined for other slots.

<sup>3</sup> These copies of the CLK-40 signal are routed to the BOCs at slots 6-21; they all have the same electronic length, and are 100 ohm differential impedance.

<sup>4</sup> The state of the bussed Laser-Ilock line appears as a bit in a Set-Up bus register. It is also available to RODs and the TIM.

<sup>5</sup> ROD-Sense grounded on ROD, pulled high through resistor on TIM and BOC. Grounded on backplane at slot 5.

<sup>6</sup> TIM-Busy Out is provided by TIM, but is not routed on the backplane.

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

**Table 6: P3/J3 Connector as used by ROD.. plugs into Slots 6-21**

Pin	Row Z	Row A	Row B	Row C	Row D
1	RD94	Gnd	RD95	+3v3 <sup>7</sup>	L-UWEN#
2	RD92	RD93	Gnd	L-URESET#	+3v3
3	RD89	RD90	RD91	+3v3	L-UCLK
4	Gnd	RD87	RD88	L-UTEST#	+3v3
5	RD85	Gnd	RD86	Gnd	L-UCTRL#
6	RD82	RD83	RD84	L-LDOWN#	+3v3
7	RD79	RD80	RD81	+3v3	L-LFF#
8	RD76	RD77	RD78	+3v3	+3v3
9	Gnd	RD74	Gnd	RD75	+3v3
10	RD71	RD72	RD73	Gnd	+3v3
11	RD68	Gnd	RD69	RD70	Laser-Ilock <sup>8</sup>
12	RD64	RD65	RD66	RD67	Gnd
13	RD60	RD61	RD62	RD63	ROD-sense <sup>9</sup>
14	Gnd	RD58	Gnd	RD59	
15	RD55	RD56	RD57	Gnd	RCLK40+ <sup>10</sup>
16	RD51	RD52	RD53	RD54	RCLK40-
17	RD48	Gnd	RD49	RD50	+5V
18	RD44	RD45	RD46	RD47	NC
19	+5V	RD41	RD42	RD43	NC
20	RD39	Gnd	RD40	Gnd	+5V
21	RD36	Bussed	RD37	RD38	ROD-Busy <sup>11</sup>
22	RD32	RD33	RD34	RD35	+5V
23	RD29	RD30	Gnd	RD31	TTC-7
24	+5V	RD26	RD27	RD28	TTC-6
25	RD23	RD24	RD25	Gnd	TTC-5
26	RD20	Gnd	RD21	RD22	TTC-4
27	RD16	RD17	RD18	RD19	+5V
28	RD13	RD14	Gnd	RD15	TTC-3
29	+5V	RD10	RD11	RD12	TTC-2
30	RD7	RD8	RD9	Gnd	TTC-1
31	RD4	Gnd	RD5	RD6	TTC-0
32	RD0	RD1	RD2	RD3	+5V

Note: TTC-0 to TTC-7 outputs from TIM are bussed to all RODs and terminated on backplane at slot 21. They are active LOW.

<sup>7</sup> BOC 3v3 power is only drawn exclusively from these 3v3 supply pins – the RODs may also draw some of their 3v3 power from them.

<sup>8</sup> The state of the bussed Laser-Ilock line appears as a bit in a Set-Up bus register. It is also available to RODs and the TIM.

<sup>9</sup> ROD-Sense grounded on ROD, pulled high through resistor on TIM and BOC. Grounded on backplane at slot 5.

<sup>10</sup> RCLK-40 is buffered copy of CLK-40 signal received by BOC on P3J3, pins D18 and D19.

<sup>11</sup> These ROD-Busy signals are routed to pins on P3J3 @ Slot5. They are active LOW, LV-TTL totem-pole signals.

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

**Table 7: P3/J3 as used by BOC .. plugs into transition (i.e. Back-Of-Crate) slots 6-21**

Pin	Row Z	Row A	Row B	Row C	Row D
1	RD94	Gnd	RD95	+3v3 <sup>12</sup>	L-UWEN#
2	RD92	RD93	Gnd	L-URESET#	+3v3
3	RD89	RD90	RD91	+3v3	L-UCLK
4	Gnd	RD87	RD88	L-UTEST#	+3v3
5	RD85	Gnd	RD86	Gnd	L-UCTRL#
6	RD82	RD83	RD84	L-LDOWN#	+3v3
7	RD79	RD80	RD81	+3v3	L-LFF#
8	RD76	RD77	RD78	+3v3	+3v3
9	Gnd	RD74	Gnd	RD75	+3v3
10	RD71	RD72	RD73	Gnd	+3v3
11	RD68	Gnd	RD69	RD70	Laser-Ilock <sup>13</sup>
12	RD64	RD65	RD66	RD67	Gnd
13	RD60	RD61	RD62	RD63	ROD-sense <sup>14</sup>
14	Gnd	RD58	Gnd	RD59	
15	RD55	RD56	RD57	Gnd	RCLK40+ <sup>15</sup>
16	RD51	RD52	RD53	RD54	RCLK40-
17	RD48	Gnd	RD49	RD50	+5V
18	RD44	RD45	RD46	RD47	CLK40+
19	+5V	RD41	RD42	RD43	CLK40-
20	RD39	Gnd	RD40	Gnd	+5V
21	RD36	Bussed	RD37	RD38	NC
22	RD32	RD33	RD34	RD35	+5V
23	RD29	RD30	Gnd	RD31	NC
24	+5V	RD26	RD27	RD28	NC
25	RD23	RD24	RD25	Gnd	NC
26	RD20	Gnd	RD21	RD22	NC
27	RD16	RD17	RD18	RD19	+5V
28	RD13	RD14	Gnd	RD15	NC
29	+5V	RD10	RD11	RD12	NC
30	RD7	RD8	RD9	Gnd	NC
31	RD4	Gnd	RD5	RD6	NC
32	RD0	RD1	RD2	RD3	+5V

<sup>12</sup> BOC 3v3 power is only drawn exclusively from these 3v3 supply pins – the RODs may also draw some of their 3v3 power from them.

<sup>13</sup> The state of the bussed Laser-Ilock line appears as a bit in a Set-Up bus register. It is also available to RODs and the TIM.

<sup>14</sup> ROD-Sense grounded on ROD, pulled high through resistor on TIM and BOC. Grounded on backplane at slot 5.

<sup>15</sup> RCLK-40 is buffered copy of CLK-40 signal received by BOC on P3J3, pins D18 and D19.

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 8: P3/J3 Connectors: use of Row Z

Pin	TIM @ Slot 5	Backplane @ Slot 5	Backplane @ Slots 6-21	ROD @ Slots 6-21	BOC @ rear of Slots 6-21
1	NC	Thru Pin	Thru Pin	RD94	RD94
2	NC	Thru Pin	Thru Pin	RD92	RD92
3	NC	Thru Pin	Thru Pin	RD89	RD89
4	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
5	NC	Thru Pin	Thru Pin	RD85	RD85
6	NC	Thru Pin	Thru Pin	RD82	RD82
7	NC	Thru Pin	Thru Pin	RD79	RD79
8	NC	Thru Pin	Thru Pin	RD76	RD76
9	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
10	NC	Thru Pin	Thru Pin	RD71	RD71
11	NC	Thru Pin	Thru Pin	RD68	RD68
12	NC	Thru Pin	Thru Pin	RD64	RD64
13	NC	Thru Pin	Thru Pin	RD60	RD60
14	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
15	NC	Thru Pin	Thru Pin	RD55	RD55
16	NC	Thru Pin	Thru Pin	RD51	RD51
17	NC	Thru Pin	Thru Pin	RD48	RD48
18	NC	Thru Pin	Thru Pin	RD44	RD44
19	+5V	+5V.. Plane	+5V.. Plane	+5V	+5V
20	NC	Thru Pin	Thru Pin	RD39	RD39
21	NC	Thru Pin	Thru Pin	RD36	RD36
22	NC	Thru Pin	Thru Pin	RD32	RD32
23	NC	Thru Pin	Thru Pin	RD29	RD29
24	+5V	+5V.. Plane	+5V .. Plane	+5V	+5V
25	NC	Thru Pin	Thru Pin	RD23	RD23
26	NC	Thru Pin	Thru Pin	RD20	RD20
27	NC	Thru Pin	Thru Pin	RD16	RD16
28	NC	Thru Pin	Thru Pin	RD13	RD13
29	+5V	+5V .. Plane	+5V.. Plane	+5V	+5V
30	NC	Thru Pin	Thru Pin	RD7	RD7
31	NC	Thru Pin	Thru Pin	RD4	RD4
32	NC	Thru Pin	Thru Pin	RD0	RD0

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 9: P3/J3 Connectors: use of Row A

Pin	TIM @ Slot 5	Backplane @ Slot 5	Backplane @ Slots 6-21	ROD @ Slots 6-21	BOC @ rear of Slots 6-21
1	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
2			Thru Pin	RD93	RD93
3	CLK40+ slot5	To J3D18, slot 5	Thru Pin	RD90	RD90
4	CLK40+ slot6	To J3D18, slot 6	Thru Pin	RD87	RD87
5	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
6	CLK40+ slot7	To J3D18, slot 7	Thru Pin	RD83	RD83
7	CLK40+ slot8	To J3D18, slot 8	Thru Pin	RD80	RD80
8	CLK40+ slot9	To J3D18, slot 9	Thru Pin	RD77	RD77
9			Thru Pin	RD74	RD74
10	CLK40+ slot10	To J3D18, slot 10	Thru Pin	RD72	RD72
11	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
12	CLK40+ slot11	To J3D18, slot 11	Thru Pin	RD65	RD65
13	CLK40+ slot12	To J3D18, slot 12	Thru Pin	RD61	RD61
14			Thru Pin	RD58	RD58
15	CLK40+ slot13	To J3D18, slot 13	Thru Pin	RD56	RD56
16	CLK40+ slot14	To J3D18, slot 14	Thru Pin	RD52	RD52
17	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
18	CLK40+ slot15	To J3D18, slot 15	Thru Pin	RD45	RD45
19	CLK40+ slot16	To J3D18, slot 16	Thru Pin	RD41	RD41
20	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
21	CLK40+ slot17	To J3D18, slot 17	Thru Pin	Bussed	Bussed
22	CLK40+ slot18	To J3D18, slot 18	Thru Pin	RD33	RD33
23			Thru Pin	RD30	RD30
24	CLK40+ slot19	To J3D18, slot 19	Thru Pin	RD26	RD26
25	CLK40+ slot20	To J3D18, slot 20	Thru Pin	RD24	RD24
26	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
27	CLK40+ slot21	To J3D18, slot 21	Thru Pin	RD17	RD17
28			Thru Pin	RD14	RD14
29			Thru Pin	RD10	RD10
30			Thru Pin	RD8	RD8
31	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
32			Thru Pin	RD1	RD1

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 10: P3/J3 Connectors: use of Row B

Pin	TIM @ Slot 5	Backplane @ Slot 5	Backplane @ Slots 6-21	ROD @ Slots 6-21	BOC @ rear of Slots 6-21
1			Thru Pin	RD95	RD95
2	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
3	CLK40- slot5	To J3D19, slot 5	Thru Pin	RD91	RD91
4	CLK40- slot6	To J3D19, slot 6	Thru Pin	RD88	RD88
5			Thru Pin	RD86	RD86
6	CLK40- slot7	To J3D19, slot 7	Thru Pin	RD84	RD84
7	CLK40- slot8	To J3D19, slot 8	Thru Pin	RD81	RD81
8	CLK40- slot9	To J3D19, slot 9	Thru Pin	RD78	RD78
9	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
10	CLK40- slot10	To J3D19, slot 10	Thru Pin	RD73	RD73
11			Thru Pin	RD69	RD69
12	CLK40- slot11	To J3D19, slot 11	Thru Pin	RD66	RD66
13	CLK40- slot12	To J3D19, slot 12	Thru Pin	RD62	RD62
14	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
15	CLK40- slot13	To J3D19, slot 13	Thru Pin	RD57	RD57
16	CLK40- slot14	To J3D19, slot 14	Thru Pin	RD53	RD53
17			Thru Pin	RD49	RD49
18	CLK40- slot15	To J3D19, slot 15	Thru Pin	RD46	RD46
19	CLK40- slot16	To J3D19, slot 16	Thru Pin	RD42	RD42
20			Thru Pin	RD40	RD40
21	CLK40- slot17	To J3D19, slot 17	Thru Pin	RD37	RD37
22	CLK40- slot18	To J3D19, slot 18	Thru Pin	RD34	RD34
23	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
24	CLK40- slot19	To J3D19, slot 19	Thru Pin	RD27	RD27
25	CLK40- slot20	To J3D19, slot 20	Thru Pin	RD25	RD25
26			Thru Pin	RD21	RD21
27	CLK40- slot21	To J3D19, slot 21	Thru Pin	RD18	RD18
28	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
29			Thru Pin	RD11	RD11
30			Thru Pin	RD9	RD9
31			Thru Pin	RD5	RD5
32			Thru Pin	RD2	RD2

# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 11: P3/J3 Connectors: use of Row C

Pin	TIM @ Slot 5	Backplane @ Slot 5	Backplane @ Slots 6-21	ROD @ Slots 6-21	BOC @ rear of Slots 6-21
1	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
2	ROD-Busy7	From J3D21, slot 7	Thru Pin	L-URESET#	L-URESET#
3	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
4	ROD-Busy9	From J3D21, slot 9	Thru Pin	L-UTEST#	L-UTEST#
5	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
6	ROD-Busy10	From J3D21, slot 10	Thru Pin	L-LDOWN#	L-LDOWN#
7	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
8	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
9	ROD-Busy12	From J3D21, slot 12	Thru Pin	RD75	RD75
10	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
11	ROD-Busy13	From J3D21, slot 13	Thru Pin	RD70	RD70
12	ROD-Busy14	From J3D21, slot 14	Thru Pin	RD67	RD67
13	ROD-Busy15	From J3D21, slot 15	Thru Pin	RD63	RD63
14	ROD-Busy16	From J3D21, slot 16	Thru Pin	RD59	RD59
15	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
16	ROD-Busy19	From J3D21, slot 19	Thru Pin	RD54	RD54
17	ROD-Busy21	From J3D21, slot 21	Thru Pin	RD50	RD50
18			Thru Pin	RD47	RD47
19			Thru Pin	RD43	RD43
20	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
21	Spare 1b Bus		Thru Pin	RD38	RD38
22			Thru Pin	RD35	RD35
23			Thru Pin	RD31	RD31
24			Thru Pin	RD28	RD28
25	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
26			Thru Pin	RD22	RD22
27			Thru Pin	RD19	RD19
28			Thru Pin	RD15	RD15
29			Thru Pin	RD12	RD12
30	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
31			Thru Pin	RD6	RD6
32			Thru Pin	RD3	RD3



# Interface Specification

## SCT Off Detector Crate Backplane and Crate Card Utilization of P3/J3

Table 12: P3/J3 Connectors: use of Row D

Pin	TIM @ Slot 5	Backplane @ Slot 5	Backplane @ Slots 6-21	ROD @ Slots 6-21	BOC @ rear of Slots 6-21
1	ROD-Busy6	From J3D21, slot6	Thru Pin	L-UWEN#	L-UWEN#
2	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
3	ROD-Busy8	From J3D21, slot8	Thru Pin	L-UCLK	L-UCLK
4	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
5			Thru Pin	L-UCTRL#	L-UCTRL#
6	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
7	ROD-Busy11	From J3D21, slot11	Thru Pin	L-LFF#	L-LFF#
8	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
9	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
10	+3v3	+3v3 .. Plane	+3v3 .. Plane	+3v3	+3v3
11	Laser-Ilock	Laser-Ilock-Bussed	Laser-Ilock-Bussed	Laser-Ilock	Laser-Ilock
12	Gnd	Gnd .. Plane	Gnd .. Plane	Gnd	Gnd
13	ROD-sense	Gnd .. Plane	Thru Pin	ROD-sense	ROD-sense
14	ROD-Busy17	From J3D21, slot17	Thru Pin		
15	ROD-Busy18	From J3D21, slot18	Thru Pin	RCLK40+	RCLK40+
16	ROD-Busy20	From J3D21, slot20	Thru Pin	RCLK40-	RCLK40-
17	+5V	+5V .. Plane	+5V .. Plane	+5V	+5V
18	CLK40+ _Ret	CLK40+ Routed	CLK40+ Routed	NC	CLK40+
19	CLK40- _Ret	CLK40- Routed	CLK40- Routed	NC	CLK40-
20	+5V	+5V .. Plane	+5V .. Plane	+5V	+5V
21	TIM-Busy Out	TIM-Busy Out	ROD-Busy-Routed	ROD-Busy	NC
22	+5V	+5V .. Plane	+5V .. Plane	+5V	+5V
23	TTC-7	TTC-7- Bussed	TTC-7- Bussed	TTC-7	NC
24	TTC-6	TTC-6- Bussed	TTC-6- Bussed	TTC-6	NC
25	TTC-5	TTC-5- Bussed	TTC-5- Bussed	TTC-5	NC
26	TTC-4	TTC-4- Bussed	TTC-4- Bussed	TTC-4	NC
27	+5V	+5V .. Plane	+5V .. Plane	+5V	+5V
28	TTC-3	TTC-3- Bussed	TTC-3- Bussed	TTC-3	NC
29	TTC-2	TTC-2- Bussed	TTC-2- Bussed	TTC-2	NC
30	TTC-1	TTC-1- Bussed	TTC-1- Bussed	TTC-1	NC
31	TTC-0	TTC-0- Bussed	TTC-0- Bussed	TTC-0	NC
32	+5V	+5V .. Plane	+5V .. Plane	+5V	+5V

## Interface Specification

### SCT Off Detector Crate Backplane: Utilization of Slots and Power Requirements

The crate has 16 slots for the RODs (16 ea.) with the BOCs (16 ea.) plugged into the card cage behind the backplane, 1 slot for the TIM, 1 slot for the 6U to 9U divider and 2 slots for the crate processor. The table below shows the assignments.

Slot Number	Item in slot
1	Crate processor, Front 6Ux160 mm
2	Reserved for crate processor use, Front 6Ux160mm
3	TBD, Front card 6Ux160 mm
4	Divider for 6U to 9U card sizes
5	TIM <i>Terminate all ROD-Busy on TIM</i>
6	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
7	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
8	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
9	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
10	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
11	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
12	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
13	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
14	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
15	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
16	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
17	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
18	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
19	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
20	ROD and BOC Front 9Ux400 mm, Back 9Ux240 mm
21	ROD and BOC <i>Terminate TTC-0 to TTC-7 here on backplane</i>

### Power Utilization:

Item	Number Of Cards	5 Volts	3.3 Volts	-12 volts	+12 Volts
ROD	16	9 A each 144 A total	11 A each 176 A total	0	0
BOC	16	4.5 A each 72 A total	3 A each 48 A total	0	0.1A each 1.6 A total
TIM	1	15 A each	8 A each	1.5A each	1.5
RCC	1	3.5 A each	0	1 A each	0
Total Amps:		234 A	232 A	2.5A	3.1 A
Power		1170W	765W	30W	37W

Crate Total Power 2002W

## Interface Specification

### **SCT Off Detector Crate Backplane: General Information**

#### **Number of RODs and BOCs (1 BOC needed per ROD) :**

The number of RODs and BOCs is reasonably stable but changes of a few percent could be needed.

<b>Application</b>	<b>Number Needed</b>
SCT barrel	44
SCT forward	48
Total SCT	92
Pixel barrel	49
Pixel forward disks 1-3	13
Pixel forward disk 4	9
Pixel B-layer	39
Total Pixels	110
<b>Grand Total RODs + BOCs</b>	<b>202</b>

#### **Number of crates:**

The number of crates should be stable.

<b>Application</b>	<b>Number Needed</b>
SCT	8
Pixel	8
<b>Total SCT Crates</b>	<b>16</b>