

SCT/Pixel ROD Slot Pinout

Features:

- Supports 18 modules using P3 only (mini link board).
- Supports 48 modules using P3 and P2 (see 'Variations' below).
- Standard VME J1/J2 backplane OK for ROD99 and system tests (if mini link board is used, but see 'Variations' below).
- Standard VME J1 backplane OK for final crate.
- Plug-and-play ROD: hard-wired slot ID on backplane.

Variations:

- Pixels may prefer a 1:1 control-to-data stream ratio; the pinout below implements a 1:2 control-to-data stream ratio.
- The many control streams shown below might be replaced with 2 to 4 control streams.
 - On the link board, the streams would be enabled (via the setup bus) on a per-link basis and OR'd together.
 - For example, one stream could be used to broadcast fast commands, another to send slow commands to individual links.
 - Using 2 to 4 control streams would eliminate the pixel/strips control-to-data stream ratio problem.
- Some ROD99 and ROD implementation proposals call for electrical connections to an S-LINK on the back-of-crate card.
 - A back-of-crate S-LINK would require about 40 signal pins, not provided for below.
 - The extra signal pins would be available if the number of supported modules is reduced or the number of control streams is reduced.
 - It may not be practical to use a standard J2 backplane for ROD99 if S-LINK connections are required.
- The MCCC slot may be near the center of the crate; 'bussed' signals might be driven onto separate busses on either side of the MCCC.

Notes:

- MCCC = Master C&C Controller.
- ROD's mate with slot connectors installed in front of the backplane.
- Link boards mate with slot connector pins protruding behind the backplane.
- J3/P3 and J2/P2 are five-row connectors; J1/P1 is a standard VME three-row connector.
- Signals are active high unless noted otherwise.
- Each slot receives a single differential ECL clock, which is shared by both the ROD and the link board.
- The clock signal is terminated on the ROD; bussed signals are terminated on the backplane.
- Explanation of Backplane column:
 - pass-thru = the signal is connected between a ROD and its link board with no connection made with the backplane
 - bussed = (see 'Variations') all ROD and MCCC slots are connected together on the backplane either via traces or power/ground planes
 - pt-to-pt = traces on the backplane form separate point-to-point connections between ROD slots and dedicated MCCC pins
 - hardwired = signals are hard-wired either high or low on backplane

Pin Counts and Connector Assignments

Description	Symbol	Level	Backplane	Pin Count			
				J3/P3	J2/P2	Total	
Transmit control stream	XC0 - XC47	3V	pass thru	18	30	48	
Receive data stream	RD0 - RD95	3V	pass thru	36	60	96	
Setup Bus data	SD0 - SD7	3V	pass thru	8		8	
address	SA0 - SA9	3V	pass thru	10		10	
read/write (low = write)	WRN	3V	pass thru	1		1	
strobe (active low)	STBN	3V	pass thru	1		1	
TTC (from MCCC board) clk	CLKP, CLKN	dif PECL	pt-to-pt	2		2	
others (active low, details TBD)	TTC0 - TTC7	3V	bussed	8		8	
Busy (active low, to MCCC board)	BUSYN	3V	pt-to-pt	1		1	
Slot ID (hardwired high or low)	ID0 - ID4	3V	hardwired	5		5	
Reserved for future use (bussed)	FB0, FB1	TBD	bussed	2		2	
Reserved for future use (not bussed)	FN0, FN1	TBD	pass thru	2		2	
Signal Subtotal				94	90	184	
Power							Max Current @ 1.25 A per pin
+5V (see VME P1 and P2 below)	P5V		bussed	5		5	6.25
+5V for PECL (quiet)	PECL5V		bussed	5		5	6.25
+3.3V	P3V		bussed	15	5	20	25
PIN bias (25V min)	PINBIAS		bussed	1		1	1.25
analog supplies (TBD)	TBD		bussed	4		4	5
analog ground	AGND		TBD	4			
Ground	GND		bussed	32	33	65	
Non-VME Subtotal				160	128	284	

Description	Symbol	Level	Backplane	Pin Count			
				J3/P3	J2/P2	Total	
VME							
signals	VSIG		bussed		25	25	
ground	VGND		bussed		4	4	
+5V	V5		bussed		3	3	3.75

Total	160	160	316	
Available	160	160	320	
Signal-To-Ground Ratio, Non-VME	2.94	2.73	2.83	
Signal-To-Ground Ratio, All	2.94	3.11	3.03	

VME P1 is not considered above

VME P1 has:

- (8) GND pins
- (3) +5V pins
- (1) +12V pin
- (1) -12V pin

Pin Count Notes:

3V = 3.3V CMOS levels.

P3V is expected to be the main logic supply.

Some 3.3V devices may have +/- 5% supply tolerances, hence the many P3V pins.

Pin Assignments

Actual pin assignments will appear below some day.