ROD Essential Model

The web page http://positron.ps.uci.edu/ rodatlas/rodwork.html holds all documents referred to in what follows, unless otherwise noted.

This document along with the accompanying figures, ROD_essential_figs.ps describes the essential features of the ROD card. It should be consistent with the interface specification documents, various. The model should include the facilities to satisfy the requirements set out in ROD99reqmt.pdf. Though at this time one has tried to identify the requirements and essential features of the ROD card, it is unavoidable that the figures will in places appear to suggest an implementation. Such suggestions should not be considered final unless explicitly stated.

- **0.0 Context**

  This figure illustrates the main function of the ROD, which is to interface the detector specific front end (FE) electronics to the outside world (ATLAS TTC and ATLAS ROB) and to the local crate processor.

  1. The ROD must transmit the LVL1 trigger, BCR and LV1R fast commands from the TTC to the FE electronics.
  2. The ROD must pass configuration and control commands from the local processor to the FE electronics according to the protocols and formats defined by the FE systems.
  3. The ROD must transmit event data and calibration information from the FE electronics to the ATLAS ROB or the local processor or both.
  4. The ROD must transmit FE and ROD status information and register contents to the local processor.
  5. The ROD must provide information on ROB and ROD buffer status to the TTC system via the BUSY signal.

- **1.0 Preprototype ROD Card**

  The ROD must receive and transmit fast signals over long distances. The bulk of the signals are transmitted optically. Dedicated interface cards handle timing of signals as well as receipt and transmission of optical signals. A VME crate processor allows communication between the ROD and ATLAS DCS.

1. The Back of Crate Card interfaces the ROD to the FE electronics and to the ATLAS ROB. This card receives and transmits optical signals via an S-LINK for communication with the ROB and via the FE links for communication with the FE modules.
2. The Clock and Trigger Distribution Card interfaces the ATLAS TTC with the RODs.
3. The ROD cards sit in a VME crate. A processor, ROC (readout controller) in the crate communicates with the ROD over the VME bus.
4. A single crate should support 16 Preprototype RODs.

- **1.1 Optical Interface**

An interface to the optical links is necessary to condition signals coming from the ROB or FEs to the ROD and going from the ROD to the ROB or FEs.

1. The optical interface must be able to transmit commands from the ROD to 18 SCT or 36 pixel modules via optical fibers.
2. The optical interface must transmit bitstreams arriving on optical fibers from 18 SCT or 36 pixel modules to the ROD. The receiver circuitry must include phase adjustment circuitry which is configurable from the ROC via the ROD.
3. The receiver amplifier/discriminator must be configurable from the ROC via the ROD.
4. The optical interface must transmit formatted event data from the ROD to the ROB via an S-LINK.
5. The optical interface must receive the XON/XOFF bit via an optical link from the ROB and transmit it to the ROD.

- **1.2 ROD Card**

The preprototype ROD card must receive register contents as well as event and calibration data from 18 SCT or 36 pixel modules. Depending on the type of information received and the desired operation, the ROD must check it for errors checking, format it and pass it on to the desired destination. Error recovery will also be performed when practical.

1. The ROD Receiver/Formatter, 1.2.2, receives bitstreams on 36 serial lines, 1 per pixel module or 2 per SCT module. It must be able to handle event and calibration data as well as register contents.

2. The received bitstreams are checked for format errors which are counted, 1.2.7, and flagged in the output. The types of format errors which can occur and the method of indicating them in the output depend on the type of information received (data or configuration). There is much, though not 100%, overlap in the types of format errors which can occur in the SCT and pixel detectors, abc_mcc.ps.
3. There are many types of errors which may occur. The event counters are configurable via VME to count only specified errors in a single counter per link.
4. During normal data taking, the event FIFO, 1.2.3, passes the BCID and L1ID to the ROD Receiver/Formatter so that consistency checks may be performed on the incoming data and so that they may be included in the outgoing data stream.
5. The ROD may be able to recover from some errors. Others may need the intervention of the ROC. Interrupts are provided for this function. The ROC may also need to pass error information to a still higher authority, hence it has access to the error counters via the VME slave interface, 1.2.6.
6. Data may be output to the ROB or made available to the ROC. A memory, 1.2.4, is provided for the latter possibility. It may be used to store histograms during a calibration run. It may also be used as a simple memory for monitoring purposes during normal data taking or for temporary storage of register contents during read back. The ROC has access to this memory via the VME slave interface.
7. Block 1.2.1 receives and formats LVL1 triggers and broadcasts them to all enabled modules. It also receives, formats and transmits configuration commands to selected modules. It provides BCID and L1ID to the "ROD Receiver/Formatter" for error checking and for inclusion in the data transmitted to the ROB or ROC. It transmits calibration signals to enabled modules. The possibility exists that it can be set up to perform calibration runs without intervention, storing the data in an on-board histogramming memory.

Notes and Questions:

- The number of receive and transmit lines is to be studied.

- **1.2.1 Control Block: Normal Running, Configuration and Calibration**

The ROD must include logic to decode incoming commands and to format outgoing commands prior to sending them downstream.

1. The control block can be configured for normal data taking, for calibration or for configuration.
2. During normal running the trigger decoder writes BCID and L1ID to the Event FIFO so that the ROD Receiver/Formatter has access to them. LVL1 triggers are formatted and transmitted to the FE modules.
3. Two options are foreseen for calibration runs. The control block can be set up so that it can coordinate a calibration run autonomously. Alternatively, the trigger decoder can be set up so that it passes TTC calibration strobes to the modules followed by formatted LVL1 trigger commands.
4. During configuration, the control block is responsible for passing the incoming control/configuration bits downstream according to the protocol defined by the modules or by the back of crate card, whichever is being configured.

– **1.2.2 ROD Receiver/Formatter**

The primary purpose of the ROD is to format event data from the FE electronics and transmit it to the ATLAS ROBs. The ROD Receiver/ Formatter illustrates the features which are required to perform this task. Register contents will arrive at the ROD on the same fibers and so the ROD Receiver/Formatter will also handle this type of information.

1. The serial to parallel conversion stage, 1.2.1.1, formats the incoming streams for output. It is the natural place to search for certain types of errors, e.g. format errors, bit errors and errors specifically flagged by the front end electronics.
2. A FIFO, 1.2.1.2, is necessary between the serial to parallel conversion, where the channels are still separate, and the stage where the information from different incoming streams are combined. A FIFO full flag should be available to the deserialization logic, telling it to log an error and interrupt the ROC. A FIFO almost full flag should be available to the deserialization logic so that it can take measures to prevent a FIFO full condition, for example by going into a "header only" mode.
3. In the gatherer, 1.2.1.3, information from all enabled links is packed into a single block. In normal data taking there will be one block per LVL1 with appropriate headers and trailers added by the gatherer. There are some errors which can be flagged at the gatherer stage, e.g. missing

links. There may be nonfatal errors which are counted or fatal errors which generate an interrupt to the ROC. The ROB XON/XOFF bit is available here so that it may be flagged in the output data.

4. A derandomizing buffer, 1.2.1.4, is necessary before the output stage. It should alert the gatherer when it is full and almost full so that appropriate measures can be taken. A full condition may cause the ROC to be interrupted. An almost full condition may generate a BUSY to the TTC, be be logged or both.
5. There must be some output control logic, 1.2.1.5, which can send output to the Back of Crate Card for transmission to the ROB during normal data taking or to the on board memory during calibration runs and register read back. The possibility to send monitoring data to the on board memory during normal data taking w/o interfering with data transmission to the Back of Crate Card is also desirable.
6. Output is formatted for transmission via a 32 bit wide S-LINK.
7. The ROD must have high level debugging capabilities. A trap and playback feature allows incoming bitstreams to be trapped and subsequently played back. Known patterns can also be written to this block from VME and the output checked against what is expected.