SCT/Pixel ROD Slot Pinout

Features:

- Supports 18 modules using P3 only (mini link board).
- Supports 48 modules using P3 and P2.
- Standard VME J1/J2 backplane OK for ROD99 and system tests (if mini link board is used).
- Standard VME J1 backplane OK for final crate.
- Plug-and-play ROD: hard-wired slot ID on backplane.

Notes:

- MCCC = Master C&C Controller.
- ROD's mate with slot connectors installed in front of the backplane.
- Link boards mate with slot connector pins protruding behind the backplane.
- J3/P3 and J2/P2 are five-row connectors; J1/P1 is a standard VME three-row connector.
- Each slot receives a single differential ECL clock, which is shared by both the ROD and the link board.
- The clock signal is terminated on the ROD; bussed signals are terminated on the backplane.
- Explanation of Backplane column:
  - pass-thru = the signal is connected between a ROD and its link board with no connection made with the backplane
  - bussed = all ROD and MCCC slots are connected together on the backplane either via traces or power/ground planes
  - pt-to-pt = traces on the backplane form separate point-to-point connections between ROD slots and dedicated MCCC pins
  - hardwired = signals are hard-wired either high or low on backplane

Pin Counts and Connector Assignments

Description	Symbol	Level	Backplane	Pin Count J3/P3	Pin Count J2/P2	Pin Count Total	
Transmit							
data	XD0 - XD47	3V	pass thru	18	30	48	
Receive							
data	RD0 - RD95	3V	pass thru	36	60	96	
Setup Bus							
data (8 bits ok)?	SD0 - SD7	3V	pass thru	8		8	
address	SA0 - SA9	3V	pass thru	10		10	
read/write*	WR*	3V	pass thru	1		1	
strobe	STB*	3V	pass thru	1		1	
TTC (from MCCC board)							
clk	CLK, CLK*	dif ECL	pt-to-pt	2		2	
others (details TBD)	L1A,etc.	3V	bussed	8		8	
Busy (to MCCC board)		3V	pt-to-pt	1		1	
Slot ID (hardwired high or low)	ID0 - ID4	3V	hardwired	5		5	
Reserved for future use (bussed)	FB0, FB1	TBD	bussed	2		2	
Reserved for future use (not bussed)	FN0, FN1	TBD	pass thru	2		2	
Signal Subtotal				94	90	184	
Power							Max Current @ 1.25 A per pin
+5V (see VME P1 and P2 below)	P5V		bussed	4		4	5
+3.3V	P3V		bussed	15	5	20	25
-5.2V	N5V		bussed	5		5	6.25
-2V	N2V		bussed	2		2	2.5
link supply 1 ?	LS1		bussed	3		3	3.75
link supply 2 ?	LS2		bussed	3		3	3.75
Ground	GND		bussed	34	33	67	
Non-VME Subtotal				160	128	288	

Description	Symbol	Level	Backplane	Pin Count J3/P3	J2/P2	Total	
VME							
signals	VSIG		bussed		25	25	
ground	VGND		bussed		4	4	
+5V	V5		bussed		3	3	3.75

Total	160	160	320
Available	160	160	320
Signal-To-Ground Ratio, Non-VME	2.76	2.73	2.75
Signal-To-Ground Ratio, All	2.76	3.11	2.94

VME P1 is not considered above
VME P1 has:
(8) GND pins
(3) +5V pins
(1) +12V pin
(1) -12V pin

Pin Count Notes:
3V = 3.3V CMOS levels.
* = active low.
P3V is expected to be the main logic supply.
Some 3.3V devices may have +/- 5% supply tolerances, hence the many P3V pins.

Pin Assignments

Actual pin assignments will appear below some day.