TIM Essential Model

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Abstract

This document is a preliminary and incomplete draft of the essential model of the SCT TTC Interface Module and its interfaces. Feedback is welcome.

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Introduction

The SCT interface with ATLAS Level 1 receives the signals through the Timing, Trigger, and Control (TTC) system and returns the SCT Busy signal to the Central Trigger Processor (CTP). This interface is with the SCT off-detector electronics, in particular with the Read-Out Driver (ROD), and is known as the SCT TTC system.

The SCT TTC system consists of the standard TTC system distributing the signals to a custom TTC Interface Module (TIM) in each crate of RODs. In addition, a Busy module returns the SCT Busy signal.

This document along with the accompanying diagram [ref. TIM_figure.pdf or .ps] describes the essential features of the TIM. It should be consistent with the interface specification documents [ref. TIM_interfaces] [ref. TIM_interface_BOC] [ref. TIM_interface_ROD]. The model should satisfy the requirements set out in the SCT TTC Interface Requirements document [ref. TIM_requirements]. A brief summary is given in [ref. TIM_talk].

Context

The accompanying diagram [ref. TIM_figure.pdf or .ps] illustrates the main function of the TIM which is to interface the off-detector electronics, in particular the ROD, with the outside world of Level-1 electronics. Diagrams showing an overview of the SCT system [ref. SCT_system] and the TTC context [ref. TTC_context.pdf or .ps] are also available.

1. The TIM transmits the clock, fast commands and event ID from the TTC system to the RODs. The clock is also transmitted to the BOC.
2. The TIM passes the Busy from the RODs via a Busy module to the CTP in order to stop it sending triggers.
3. The TIM can send standalone clock, fast commands and event ID to the RODs under control of the local processor.
4. The TIM is configured by the local processor setting up its registers. They can be inspected by the local processor.

TTC Interface Module

The TIM receives the TTC signals and passes the required subset to the RODs.

The optical TTC signals are received by a receiver section containing a standard TTCrx receiver chip, which decodes the TTC information into electrical form. This may not be implemented on the preprototype TIM.

The TTC information which may be required is:

```
       clock: BC   Bunch Crossing clock
fast command: L1A  Level-1 Accept
              ECR  Event Counter Reset
              BCR  Bunch Counter Reset
              CAL  Calibrate signal
    event ID: L1ID 24-bit Level-1 trigger number
              BCID 12-bit Bunch Crossing number
              TTID  8-bit Trigger Type
```

The TIM outputs the above information onto the backplane of a ROD crate with the appropriate timing. The event ID is transmitted with a serial protocol and so a FIFO (First In First Out) buffer is required in case of rapid triggers.

The TIM can generate the above information standalone at the request of the local processor. It can also be connected to another TIM for multi-crate operation. Standalone functionality has been implemented on the CLOck And Control Master used in the SCT system tests [ref. SCT_CLOAC].

The TIM has programmable timing adjustments and control functions.

The TIM has a VME slave interface to give the local processor read and write access to its registers.

The TIM does a masked OR of the ROD Busy signals and outputs Busy to a Busy module.

A brief note on TIM and CLOAC is in [ref. TIM_note].

SCT TTC System

A partition [ref. TTC_partition.pdf or .ps] of the TTC system [ref. TTC_TDR] [ref. TTC_PhF] consists of a TTC VMEbus Interface (TTCvi) module, a TTC transmitter crate and an optical network. The SCT has been allocated 4 partitions. Each partition is capable of running independently.

The TTCvi module receives global ATLAS Level-1 signals such as the LHC clock and Level-1 Accept triggers. It can be programmed to generate SCT specific signals like Front-End Reset and Calibrate, and to run standalone.

A possible layout of an SCT partition is shown in [ref. SCT_partition_v0.pdf or .ps]. However, as we foresee only two ROD crates per partition, we expect to use a TTC VME transmitter (TTCvx) module instead of a TTC transmitter crate. This scheme is shown in [ref. SCT_partition.pdf or .ps] with daisy-chained ROD crate Busy signals, instead of a Busy module per partition. A Local Trigger box can generate local triggers and deadtime for each partition (these functions may be implemented in the TTCvi module).

Busy Module

The ROD Busy signals are combined into a Busy signal per partition, and then into the SCT Busy to the CTP in order to stop it sending triggers. Note that a partition Busy signal is input to both the SCT Busy and the Local Trigger box.

The standard Busy module [ref. BSY_TDR] does a masked OR of the ROD Busy signals to give the SCT Busy, and it monitors each input Busy channel.

Each individual ROD Busy signal could be monitored either by a Busy module per crate or by implementing the Busy module design onto the TIM.

References


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SCT_system         http://positron.ps.uci.edu/~roddaq/offdet.pdf
TIM_interfaces     http://positron.ps.uci.edu/~roddaq/roddaq.html
TIM_interface_BOC  http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_interface_BOC.txt
TIM_interface_ROD  http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_interface_ROD.txt
TIM_figure         http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_figure.pdf
TIM_requirements   http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_requirements.txt
TIM_talk           http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_talk.ps
TIM_note           http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_note.txt
TTC_context        http://www.hep.ucl.ac.uk/~jbl/SCT/TTC_context.pdf
TTC_partition      http://www.hep.ucl.ac.uk/~jbl/SCT/TTC_partition.pdf
SCT_partition      http://www.hep.ucl.ac.uk/~jbl/SCT/SCT_partition.pdf
SCT_partition_v0   http://www.hep.ucl.ac.uk/~jbl/SCT/SCT_partition_v0.pdf
SCT_CLOAC          http://www.hep.ucl.ac.uk/atlas/sct/#CLOAC
TTC_PhF    http://nicewww.cern.ch/~mclaren/atlas/conferences/ROD/ttc.pdf
TTC_TDR    http://www.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/V1REV1/L1TDR_TTC.*
BSY_TDR    http://www.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/V1REV1/L1TDR_Deadtm.*

            .* = .pdf or .ps
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History:

0.1  3Nov98 JBL First draft
0.2 16Jul99 JBL Update and minor changes
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Last update: 16 July 1999 by John Lane (UCL) email: jbl@hep.ucl.ac.uk

http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_model.html