SCT TIM-RCC Interface Specification

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Draft 0.1 by John Lane <jbl@hep.ucl.ac.uk>

Abstract

This document is a VERY preliminary and incomplete draft of the SCT interface specification between TIM and RCC. Feedback is welcome.

Introduction

The TTC Interface Module (TIM) communicates with a local processor, the ROD Crate Controller (RCC) via a VME slave interface.

This document should satisfy the interface requirements set out in the RCC requirements document [ref. RCC_requirements] and the TIM requirements document [ref. TIM_requirements].

Notes

The following notes are extracted from Martin's CLOAC writeup at

http://www.hep.ucl.ac.uk/~mp/C-C_Master_regs+busy_memo.txt

to give an idea of the VME interface for TIM stand-alone functionality...

SOME NOTES ON DESIGN AND FUNCTIONALITY OF THE "CLOAC" VME MODULE

The "CLOAC" (CLOck And Control) MASTER Module has been designed and built for the later stages of the ATLAS-SCT FE System Tests and Beam Tests.

As well as the master 40.08 MHz clock, the "CLOAC MASTER" Module generates the fast commands : "Level 1 Trigger", "Soft Reset" and "BC Reset".

Also supported is the "Calibration Pulse" sequence, which includes automatic "Cal. trigger" after a programmable delay.

The "CLOAC MASTER" module is capable of a stand-alone operation as well as of being synchronised to external sources.

* Each "CLOAC MASTER" VME module has the following inputs and outputs :

A) Internal Hardware-generated signals are as follows :

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40.08 MHz clock ( 50% M/S ratio, +/- 5% )
Level 1 Trigger - single
                - repetitive with selectable
                  frequency between 50 Hz - 600 kHz
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                    - repetitive with randomly spaced triggers
                      with selectable average frequency
                      between 12.5 Hz - 150 kHz
        Soft Reset  - repetitive at selectable
                      frequency between 0.005 Hz - 60 Hz
        BC Reset    - repetitive about every 88.924 usec
                      ( LHC beam crossing rate of 11.2456 kHz )
```

All these signals can be enabled/disabled via VME

B) The following commands can be issued via the VME :

Level 1 Trigger	=	VSINGLETRIG
Soft Reset	=	VSRST
BC Reset	=	VBCRST
Calibration Pulse	=	VCAL
Busy	=	VBUSY
Overall Reset	=	VOARST
Select "burst" mode	=	VBURST

* VME interface :

A) The "CLOAC MASTER" is a single width, A24/D16 slave VME module, with the base address A16 - A23 selectable by the 8-bit switch

B) Address Line A0 is always assumed to be ZERO, ie. no byte transfers - D16 transfers only
No block transfers are allowed for

C) Address lines A8 - A15 are not decoded or used on this module (ie. the address space wraps around)

* REGISTERS :

0. INPUTS / OUTPUTS ENABLE
1. VME COMMANDS
2.(COMMAND STRINGS - CLOAC only, not TIM)
3. REPETITIVE FREQUENCY SELECT
4.(TRIGGER INPUT WINDOW SIZE AND DELAY SELECT - CLOAC only, not TIM?)
5. TRIGGER DELAY SELECT
6. BUSY STATE

Register 1 : VME COMMANDS

Base Address + 02 VME read/write access

Bit 0	VSINGLETRIG	*	writing "1" gives a single	TRIGGER
1	VSRST	*	-"-	SRST
2	VBCRST	*	-"-	BCRST
3	VCAL	*	-"-	CALIBRATE
4				
5	VOARST	*	-"-	OARST
6	VBURST		writing "1" enables the 'burst' mode	
7	VBUSY		BUSY input ("1"= asserted, "0"= not asserted)	

```
                NOTE :  * For each single command, write "1", followed by "0"
                ======  to clear the command


* ABBREVIATIONS USED :  BCRST : BC ( Beam Crossing ) Reset
                        BURST : 'Burst' of a pre-set number of Triggers
                        CAL   : Calibration Test Pulse
                        DLY   : Delay
                        EN    : Enable
                        EXT   : External ( Input from NIM or IDC socket )
                        INT   : Internal ( Hardware generated )
                        OARST : Overall On-board Electronics Reset
                        RP    : Repetitive
                        SRST  : Soft Reset
                        TRIG  : Level 1 Trigger
                        V     : VME-generated command


References
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RCC_requirements http://www.hep.phy.cam.ac.uk/atlas/hill/rcc_tim.html
TIM_requirements http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_requirements.txt

http://www.hep.ucl.ac.uk/~mp/C-C_Master_regs+busy_memo.txt

History:

0.1 30Jul99 JBL First draft

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http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_interface_RCC.txt
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