SCT TIM-ROD Interface Specification

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Abstract

This document is a preliminary and incomplete draft of the SCT interface specification between TIM and ROD. Feedback is welcome.

Introduction

The TTC Interface Module (TIM) interfaces to a crate of Read-Out Drivers (RODs) via a custom backplane.

This document should satisfy the interface requirements set out in the ROD requirements document [ref. ROD_requirements] and the TIM requirements document [ref. TIM_requirements].

Signals

* The TIM delivers the following signals to each ROD slot:

Name	Level	Description
TTC0-TTC7	3V	miscellaneous signals synchronized to clock

TTC0 - TTC7 should be generated by programmable logic on the TIM and received by programmable logic on the ROD, allowing the meaning of the signals to be changed as the TIM and ROD designs solidify.

* Signal assignments for TTC0 - TTC7:

Name	Signal	Comment
TTC0	L1Accept	Level-1 trigger Accept decision
TTC1	ECReset	Event Counters (L1ID) are reset periodically
TTC2	BCReset	Bunch Counters (BCID) are reset once per LHC orbit
TTC3	CAL	Issue Calibration Pulse command to front-end amplifiers
TTC4	SerialID	1 start bit + 24 L1ID bits + 12 BCID bits
TTC5	SerialTT	1 start bit + 8 trigger type bits + 2 reserved bits
TTC6	reserved	maybe separate periodic reset (Soft Reset command)
TTC7	unused	

All the signals above are active-low; unused signals are held high. L1Accept, ECReset, BCReset and CAL are active for one clock cycle. In response to these signals, the ROD generates the control bit sequence appropriate to the module type: strips (SCT) or pixels.

* The TIM receives the following signal from each ROD slot:

Name Level Description

BUSY 3V   active-low ROD busy

Timing
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* The clock for each ROD is passed from its back-of-crate (BOC) card.

* At each ROD slot, the TTC0-TTC7 signals from the TIM must satisfy the setup and hold timing specification relative to the active edge of the clock. The TIM takes into account the delay of buffering the clock in the BOC and the timing skew due to the backplane.

* Latency adjustment to the signals L1Accept, ECReset, BCReset and CAL is done in the Timing, Trigger and Control (TTC) system.

* The ROD BUSY signal is asynchronous.

Electrical Notes
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* TTC0-TTC7 are bussed and terminated on the backplane; only the trace end that is most distant from the driver is terminated, assuming the TIM slot is at the other end.

* RODs should minimally load TTC0-TTC7 so that transmission line characteristics are affected as little as possible by the presence or absence of RODs.

* Negative (active-low) logic is preferred for low duty-cycle signals (all signals).

* The ROD BUSY from each slot is routed to a separate pin on the TIM slot.

* The TIM should pull all BUSY signals high (inactive) through a resistor, or they should be similarly terminated on the backplane.

References

ROD_requirements http://positron.ps.uci.edu/~roddaq/ROD99reqmt.pdf
TIM_requirements http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_requirements.txt

http://www.hep.ucl.ac.uk/~jbl/SCT/Crate-backplane.ps

http://positron.ps.uci.edu/~pier/ROD/pdf/ROD_BOC_Interface0.PDF
http://positron.ps.uci.edu/~pier/ROD/pdf/RodPinoutVME64x0.PDF

History:

0.3 11Nov98 UCI http://positron.ps.uci.edu/~pier/ROD/pdf/RODtofromTTC1.PDF
0.4 29Jul99 JBL New version

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