TIM Registers

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This document is a preliminary and incomplete description of the TIM registers. Feedback is welcome.

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Introduction

The TTC Interface Module (TIM) has a VME slave interface to give the local processor read and write access to its registers.

This document supports the interface specification [ref. TIM_interface_RCC]. TIM stand-alone operation is described in [ref. TIM_manual].

Address Map

The VME address space is A24 or A32 with the Base Address offset selected by Geographical Address or switches. The Base Address uses address lines A31 - A16, leaving an A16 address space of 64K bytes, using address lines A15 - A0.

- VME access is D16 only, ie A0 is not used and always assumed to be zero
- Registers are addressed by decoding A15 - A1, with A15 = 0
- Sequencer memory addresses are given by A15 - A1, with A15 = 1

The VME Address is given as hexadecimal bytes in the following tables.

Address Map	
Offset by Base Address (A31 - A16)	
Address	**D16 Field**
0000 - 003E	Register address space
0040 - 7FFE	Reserved address space
8000 - FFFE	First word of Sequencer RAM Last word of Sequencer RAM

Register Address Map			
Address	**Read/ Write**	**16-bit Field**	**PLD**
00	R/W	0. Enables	2
02	R/W	1. Command	2
04	R/W	2. Burst Count	3
06	R/W	3. Frequency	3
08	R/W	4. Window	3

0A	R/W	5. Delay	2
0C	R	6. Status	3
0E	R	7. FIFO	5
10	R(/W)	8. Trigger IDlo	4a
12	R(/W)	9. Trigger IDhi	4a
14	R(/W)	10. Trigger Bunch	4b
16	R(/W)	11. Trigger Type	4b
18	R/W	12. Run Enables	6
1A	R/W	13. Sequencer	7
1C	R/W	14. Sequencer End	7
1E	R/W	15. ROD Mask	8
20	R	16. ROD BUSY	8
22	R	17. ROD Latch	8
24	R	18. ROD Monitor	8
26	R	19. TTC Data	9
28	R/W	20. TTC Select	9
2A	R	21. TTC BCID	4b
2C	R/W	22. TTCrx Access	9
2E	R	23. TTC Status	9
30	R	24. TIM Output	6
32	R	25. TIM ID	5

Registers

- TIM RESET means power-up reset, push-button reset, or vRESET command bit
- reserved bits are either Read/Write or = 0 if Read only
- undefined bits are not implemented and read as any value

0. Enables Register

Register 0	Stand-alone Enables
VME Address: 00	R/W

bit	Field	Function
0	-	reserved
1	EnIntTRIG	Enable internal repetitive trigger
2	EnIntECR	Enable internal repetitive ECReset
3	EnIntBCR	Enable internal repetitive BCReset
4	EnRandom	Enable internal trigger randomizer
5	EnIntFER	Enable internal repetitive FEReset
6	EnWindow	Enable trigger window
7	EnIntBUSY	Enable internal BUSY
8	EnExtCLK	Enable external clock inputs
9	EnExtTRIG	Enable external trigger inputs
10	EnExtECR	Enable external ECReset inputs
11	EnExtBCR	Enable external BCReset inputs
12	EnExtCAL	Enable external Calibrate inputs
13	EnExtFER	Enable external FEReset inputs
14	EnExtSEQ	Enable external Sequencer Go inputs
15	EnExtBUSY	Enable external BUSY inputs

Register is reset to 0 by TIM RESET

Note: external means ECL or NIM front-panel inputs. EnExtCLK disables the internal clock.

Note: IntECR is only available if the internal ECR = FER link is inserted (this is the default hardware setup).

1. Command Register

Register 1	VME Commands
VME Address: 02	R/W

bit	Mode	Field	Function
0	-	-	reserved
1	edge	vTRIG	Single trigger
2	edge	vECR	Single ECReset
3	edge	vBCR	Single BCReset
4	edge	vCAL	Single Calibrate strobe
5	edge	vFER	Single FEReset
6	edge	vSpare	Single Spare command
7	level	vBUSY	Set BUSY
8	level	vRODBUSY	Set ROD BUSY
9	level	vBurstMode	Set BURST mode - disable triggers
10	edge	vBurstGO	Start BURST triggers - Int or Ext
11	-	-	reserved
12	level	SetRunMode	Enable Run Mode
13	level	EnTestBUSY	Enable BUSY for testing
14	level	ClrTestBUSY	Clear BUSY for next event
15	edge	vRESET	Overall TIM RESET

Register is reset to 0 by TIM RESET

Note: a command bit has one of two modes of operation:

1. level : command is asserted while the bit is set (to 1)
2. edge : command is generated by setting the bit (from 0 to 1, ie the bit must be cleared to re-enable operation)

2. Burst Count Register

Register 2	Burst Count
VME Address: 04	R/W

bits	Field	Function
0-15	BurstCount	Number of triggers in BURST

Register is reset to 0 by TIM RESET

3. Frequency Register

Register 3	Repeat Frequencies
VME Address: 06	R/W

bits	Field	Function
0- 4	IntTRIGfreq	Internal trigger look-up table
5- 7	-	reserved
8-12	IntFER_freq	Internal ECR/FER look-up table
13-15	-	reserved

Register is reset to 0 by TIM RESET

Note that in the two tables below, the frequency values in row 1 are not in sequence with other rows.

IntTRIGfreq look-up table				kHz
bits 4-3	**0**	**1**	**2**	**3**
bits 2-0				
0	600	60	6.0	0.60
1	60	6	0.6	0.06
2	300	30	3.0	0.30
3	200	20	2.0	0.20
4	150	15	1.5	0.15
5	120	12	1.2	0.12
6	100	10	1.0	0.10
7	50	5	0.5	0.05

IntFER_freq look-up table				Hz
bits 12-11	**0**	**1**	**2**	**3**
bits 10- 8				
0	60	6.0	0.60	0.060
1	6	0.6	0.06	0.006
2	30	3.0	0.30	0.030
3	20	2.0	0.20	0.020
4	15	1.5	0.15	0.015
5	12	1.2	0.12	0.012
6	10	1.0	0.10	0.010
7	5	0.5	0.05	0.005

Note: if the EnRandom bit is set, the average frequency of the random triggers is one quarter of the above internal trigger frequency table.

Example: write 0E06 hex for triggers at 100 kHz and front-end resets at 1 Hz.

4. Window Register

Register 4		**Trigger Window**
VME Address: 08		R/W
bits	**Field**	**Function**
0- 5	WinSize	Trigger window size (0.5ns steps)
6- 7	-	reserved
8-13	WinDelay	Trigger window delay (0.5ns steps)
14-15	-	reserved
Register is reset to 0 by TIM RESET		

Note: the Trigger Window register is for External Trigger input only.

5. Delay Register

Register 5		**Stand-alone Delays**
VME Address: 0A		R/W
bits	**Field**	**Function**
0- 7	TrigDelay	Stand-alone trigger pipeline delay (clock steps)
8-13	ClkDelay	Stand-alone clock delay (0.5ns steps)
14-15	-	reserved
Register is reset to 0 by TIM RESET		

6. Status Register

Register 6	Status
VME Address: 0C	R

bit	Field	Function
0	ExtBUSY	Front-panel BUSY input
1	ExtBUSYout	Bit 0 masked by EnExtBUSY
2	IntBUSY	Internal BUSY only
3	BUSYout	OR of all enabled BUSYs (output)
4	BurstBUSY	BURST sequence running
5	SeqBUSY	Sequencer running
6	SinkBUSY	Sink running
7	RODBUSYout	Masked OR of ROD BUSYs (output)
8	TTCClkON	TTC system clock running
9	SaClkON	Stand-alone clock running
10	RunMode	TTC system operation
11	SaMode	Stand-alone operation
12	-	reserved = 0
13	TIM_OK	Clock running etc
14	TestBUSY	Stops Int and Ext triggers (if enabled)
15	LaserInterlock	Laser Interlock on

7. FIFO Register

Register 7	FIFO Status
VME Address: 0E	R

bits	Field	Function
0- 5	IDcount	Event ID FIFO count
6	IDEF	Event ID Empty Flag
7	IDFF	Event ID Full Flag
8-13	TTcount	Trigger Type FIFO count
14	TTEF	Trigger Type Empty Flag
15	TTFF	Trigger Type Full Flag

Register is reset to 4040 hex by TIM RESET

8. Trigger IDlo Register

Register 8	Trigger Number lo word
VME Address: 10	R(/W)

bits	R/W	Field	Function
0-15	R	L1IDlo	Last trigger number (bits 0-15)
0-15	(R/W)	L1IDlo	Load last trigger number (next-1)

Write access in VME mode (stand-alone) only

Register is reset to FFFF hex by TIM RESET

9. Trigger IDhi Register

Register 9	Trigger Number hi word
VME Address: 12	R(/W)

bits	R/W	Field	Function
0- 7	R	L1IDhi	Last trigger number (bits 16-23)
0- 7	(R/W)	L1IDhi	Load last trigger number (next-1)
8-15	R	ECRID	ECR counter

Write access in VME mode (stand-alone) only
Register is reset to 00FF hex by TIM RESET

10. Trigger Bunch Register

Register 10	Trigger Bunch Crossing
VME Address: 14	R(/W)

bits	R/W	Field	Function
0-11	R	BCID	Bunch Crossing number of last trigger
12-15	R/W	Offset	BCID offset

Register is reset to 0 by TIM RESET

11. Trigger Type Register

Register 11	Trigger Type
VME Address: 16	R(/W)

bits	Field	Function
0- 7	TTID1	TTC Trigger Type
8- 9	TTID2	TIM Trigger Type
10-15	-	undefined

Write access in VME mode (stand-alone) only
Register is reset to 0 by TIM RESET

12. Run Enables Register

Register 12	TTC and Other Enables
VME Address: 18	R/W

bit	Field	Function
0	EnCLK	Enable TTC clock
1	EnL1A	Enable TTC L1Accept trigger
2	EnECR	Enable TTC ECReset
3	EnBCR	Enable TTC BCReset
4	EnCAL	Enable TTC Calibrate strobe
5	EnFER	Enable TTC FEReset
6	EnSpare	Enable TTC Spare command
7	EnRODBUSY	Enable ROD BUSY into BUSYout
8	EnExtRODBUSY	Enable external ROD BUSY input
9	EnID	Enable trigger & bunch ID numbers
10	EnTYPE	Enable trigger type
11	-	reserved
12	-	reserved
13	-	reserved
14	EnSaECR	Enable counter ECR
15	EnSaBCR	Enable counter BCR

Register is reset to 0 by TIM RESET

13. Sequencer Register

Register 13	Sequencer Control
VME Address: 1A	R/W

bit	Mode	Field	Function
0	level	EnSeqTRIG	Enable L1Accept trigger
1	level	EnSeqECR	Enable ECReset
2	level	EnSeqBCR	Enable BCReset
3	level	EnSeqCAL	Enable Calibrate strobe
4	level	EnSeqID	Enable SerialID
5	level	EnSeqTT	Enable SerialTT
6	level	EnSeqFER	Enable FEReset
7	level	EnSeqSpare	Enable Spare command
8	-	-	reserved
9	level	SeqRESET	Reset Sequencer
10	edge	SeqGO	Start Sequencer
11	level	EnCyclic	Enable cyclic operation
12	-	-	reserved
13	level	SinkRESET	Reset Sink
14	edge	SinkGO	Start Sink (and Source)
15	level	EnStartSink	Enable Sink trigger

Register is reset to 0 by TIM RESET

Note: a sequencer control bit has one of two modes of operation:

1. level : command or enable is asserted while the bit is set (to 1)
2. edge : command is generated by setting the bit (from 0 to 1, ie the bit must be cleared to re-enable operation)

14. Sequencer End Register

Register 14	Sequencer End
VME Address: 1C	R/W

bits	Field	Function
0-13	EndAddr	End/Recycle address
14-15	-	reserved

Register is reset to 0 by TIM RESET

15. ROD Mask Register

Register 15	ROD Mask
VME Address: 1E	R/W

bits	Field	Function
0-15	RODmask	ROD BUSY mask (16 slots: 5-12, 14-21)

Register is reset to 0 by TIM RESET

Note: the ROD bits are in the order of ROD slot number, eg bit 0 is slot 5 in the ROD crate, bit 7 is slot 12, bit 8 is slot 14, etc.

16. ROD BUSY Register

Register 16	ROD BUSY Status
VME Address: 20	R

bits	Field	Function
0-15	RODBUSY	ROD BUSY status (16 slots: 5-12, 14-21)

Note: the ROD bits are in the order of ROD slot number, eg bit 0 is slot 5 in the ROD crate.

17. ROD Latch Register

Register 17	ROD BUSY Latch
VME Address: 22	R

bits	Field	Function
0-15	RODlatch	ROD BUSY latch (16 slots: 5-12, 14-21)

Register is reset to 0 by TIM RESET or by a write

Note: the ROD bits are in the order of ROD slot number, eg bit 0 is slot 5 in the ROD crate.

18. ROD Monitor Register

Register 18	ROD BUSY Monitor
VME Address: 24	R

bits	Field	Function
0-15	RODmonitor	ROD BUSY monitor (16 slots: 5-12, 14-21)

Register is reset to 0 by TIM RESET or by a write

Note: the ROD bits are in the order of ROD slot number, eg bit 0 is slot 5 in the ROD crate.

19. TTC Data Register

Register 19	TTC Data
VME Address: 26	R

bits	Field	Function
0- 7	Dout	Long-format data
8-15	SubAddr	Sub-address

Register is reset to 0 by TIM RESET or by a write

20. TTC Select Register

Register 20	TTC Select
VME Address: 28	R/W

bits	Field	Function
0- 3	DQselect	Select long-format Data Qualifier
4-15	-	undefined

Register is reset to 0 by TIM RESET

21. TTC BCID Register

Register 21	TTC BCID
VME Address: 2A	R

bits	Field	Function
0-11	TTC_BCID	TTC bunch number
12-15	-	undefined

Register is reset to 0 by TIM RESET

22. TTCrx Access Register

Register 22	TTCrx Access
VME Address: 2C	R/W

bits	R/W	Field	Function
0- 7	R/W	Data	TTCrx data (read or write)
8-12	R/W	Pointer	TTCrx register number
13	R/W	Read	I2C Read (not Write)
14	R/W	Enable	I2C clock enable
15	W	Control	I2C Go
15	R	Control	I2C Busy handshake

Register is reset to 0 by TIM RESET

23. TTC Status Register

Register 23		TTC Status
VME Address: 2E		R
bit	**Field**	**Function**
0	BCntRes	BCReset
1	EvCntRes	ECReset
2	Brcst(2)	FEReset bit - system message
3	Brcst(3)	Broadcast bit - system message
4	Brcst(4)	Broadcast bit - system message
5	Brcst(5)	Broadcast bit - system message
6	Brcst(6)	Calibrate bit - user message
7	Brcst(7)	Broadcast bit - user message
8	L1Accept	Trigger
9	BrcstStr1	Broadcast strobe - system message
10	BrcstStr2	Broadcast strobe - user message
11	DoutStr	Long-format data strobe
12	DbErrStr	Double error or frame error occured
13	SinErrStr	Single error occured
14	TTCReady	TTCrx operating correctly
15	-	reserved = 0
Register is reset to 0 by TIM RESET or by a write		

24. TIM Output Register

Register 24		TIM Output
VME Address: 30		R
bit	**Field**	**Function**
0	TTCout0	L1Accept trigger
1	TTCout1	ECReset
2	TTCout2	BCReset
3	TTCout3	Calibrate strobe
4	TTCout4	SerialID
5	TTCout5	SerialTT
6	TTCout6	FEReset
7	TTCout7	Spare command
8-15	-	reserved = 0
Register is reset to 0 by TIM RESET or by a write		

25. TIM ID Register

Register 25		TIM ID
VME Address: 32		R
bits	**Field**	**Function**
0- 7	SerialNo	Serial number
8-15	Version	Version number

Sequencer RAM

Sequencer RAM Address Map	
Address	**Byte Field (D16 access only)**
8000	First byte of Source data
8001	First byte of Sink data
...	...
FFFE	Last byte of Source data
FFFF	Last byte of Sink data

Note: the source and sink memories are each 16K bytes long, interleaved with the source being the least significant byte of each 16-bit word, giving 32K bytes (16K words) of sequencer memory in total.

Note: the memories have no reset and have undefined values after a power-up cycle; to be safe they should be filled with zeros after each TIM RESET.

Sequencer RAM		
VME Address: 8000-FFFE		R/W
bit	**Field**	**Function**
0	SourceTRIG	Source L1Accept trigger
1	SourceECR	Source ECReset
2	SourceBCR	Source BCReset
3	SourceCAL	Source Calibrate strobe
4	SourceID	Source SerialID
5	SourceTT	Source SerialTT
6	SourceFER	Source FEReset
7	SourceSpare	Source Spare command
8	SinkTRIG	Sink L1Accept trigger
9	SinkECR	Sink ECReset
10	SinkBCR	Sink BCReset
11	SinkCAL	Sink Calibrate strobe
12	SinkID	Sink SerialID
13	SinkTT	Sink SerialTT
14	SinkFER	Sink FEReset
15	SinkSpare	Sink Spare command

References

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TIM_interface_RCC http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_interface_RCC.html
TIM_manual        http://www.hep.ucl.ac.uk/atlas/sct/tim/TIM_manual.html

History:

0.0  2Dec99  MP First draft
0.1  3Jul00 JBL First draft on the Web
0.2 21Jul00 JBL Minor update
0.3  9Nov00 JBL Minor update
0.4 24Nov00 JBL Add frequency tables, RAM bits
0.5 11Mar01 JBL Move TIM ID & Output, add ROD Latch & Monitor
0.6 21Mar02 JBL Redefine some bits
0.7 11Nov02 JBL Rearrange L1ID registers to add ECRID (firmware v9)
0.8 22Jun04 JBL L1ID registers reset to -1 (firmware v9)
```

Last update: 22 June 2004 by John Lane (UCL) email: jbl@hep.ucl.ac.uk

`http://www.hep.ucl.ac.uk/~jbl/SCT/TIM_registers.html`