

# THE ATLAS BINARY CHIP

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## ABSTRACT

This paper presents a general overview of the binary readout system for the proposed ATLAS Semiconductor Tracker (SCT), together with a detailed description of the "ABC" chip being developed for this system.

The SCT binary readout architecture is based on a bipolar amplifier/discriminator and CMOS pipeline circuits. In one configuration this is arranged as two chips, a bipolar amplifier/discriminator chip (CAFE-M) and a CMOS pipeline chip (ABC). The "ABC" chip reads out 128 channels of silicon strip data from a "CAFE-M" chip. The data are stored in a 128 location deep pipeline, for the duration of the level 1 trigger (L1) latency. For every L1 trigger received by the chip, only the data corresponding to hit strips are read out. Data is read out from the "ABC" chips via a token ring. This scheme enables several chips to be daisy chained together on a detector module.

## 1. INTRODUCTION

The ATLAS Semiconductor Tracker will consist of approximately 6 million channels of silicon strip detectors requiring the same number of electronic readout channels.. The SCT binary readout system detects hits generated in silicon strip detectors by particles passing through it. Only the presence of hits is recorded; no amplitude information is retained. The binary readout chain consists of a preamplifier, a shaper, a discriminator, and a digital pipeline. In one implementation, this is arranged as two chips, a bipolar amplifier/discriminator chip (CAFE-M) [1] and a CMOS pipeline chip (ABC). Data is held in the digital pipeline until receipt of a trigger signal, when the data is transmitted via data links to the off detector electronics for further processing. Both, data links based on opto-electronics devices and links based on twisted pairs are being investigated. A block diagram of the system is shown in figure 1.

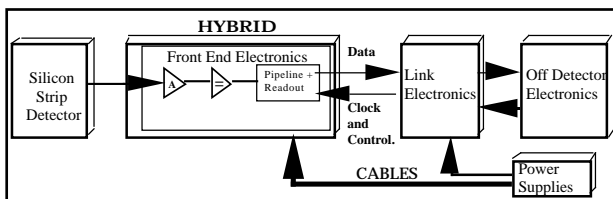


Fig 1 Block Diagram of the Atlas SCT.

## 2. ATLAS SEMI-CONDUCTOR TRACKER

The Atlas Semi-Conductor Tracker will be made of 4088 modules. Each module will consist of 1,536 silicon strips which will be read out by 12 pairs of readout chips mounted on a hybrid (see figure 2). Each chip pair processes the signals from 128 strips. Signals from the detector are first passed to an amplifier discriminator chip, CAFE-M, which amplifies the signal from the detector with a shaping time of 20ns. The amplifier has 1,500 electrons of input referred noise. The output of the amplifier is passed to a discriminator the threshold of which can be set in the range 0.5fC to 5fC by a DAC built into the ABC chip. The discriminator output is connected to the inputs of the ABC chip where it is sampled at the LHC bunch crossing rate of 40MHz. These samples are stored in a digital pipeline on the ABC chip for 3.2μs while a L1 trigger decision is made. On receipt of a L1 trigger data from each group of ABC chips is read out via a token ring with one of the ABC chips controlling the readout process. Each side of the hybrid is read out separately and has its own data link. Circuitry built into the ABC chip enables data to be read out from the hybrid in the event of a single chip or data link failure. In addition to receiving the LHC bunch crossing clock, all ABC chips also receive commands over a serial data link from the off-detector electronics. Three types of command can be received by the ABC; L1 triggers, fast commands, and slow commands. Fast commands are time critical commands such as the issuing of a reset command. Slow commands are used to alter the configuration of the ABC chip. A geographical addressing scheme is employed to enable individual chips to be addressed. Each hybrid has both a normal and backup set of clock and command inputs so that in the event of one of these sets of inputs failing the other one can be used.

## 3. ABC

A block diagram of the ABC chip is shown in figure 3. The signal flow in the ABC chip is as follows. Data at the inputs of the chip is first passed to an edge detection circuit which ensures that only a single '1' is written into the pipeline for every pulse detected by the discriminator irrespective of its duration. This feature may be disabled by sending the appropriate slow command to the chip. After passing through the edge detection circuitry the signal is passed through a mask register which enables data from bad or noisy channels to be suppressed. The mask register can also be used to inject test values into the chip when placed in test mode.

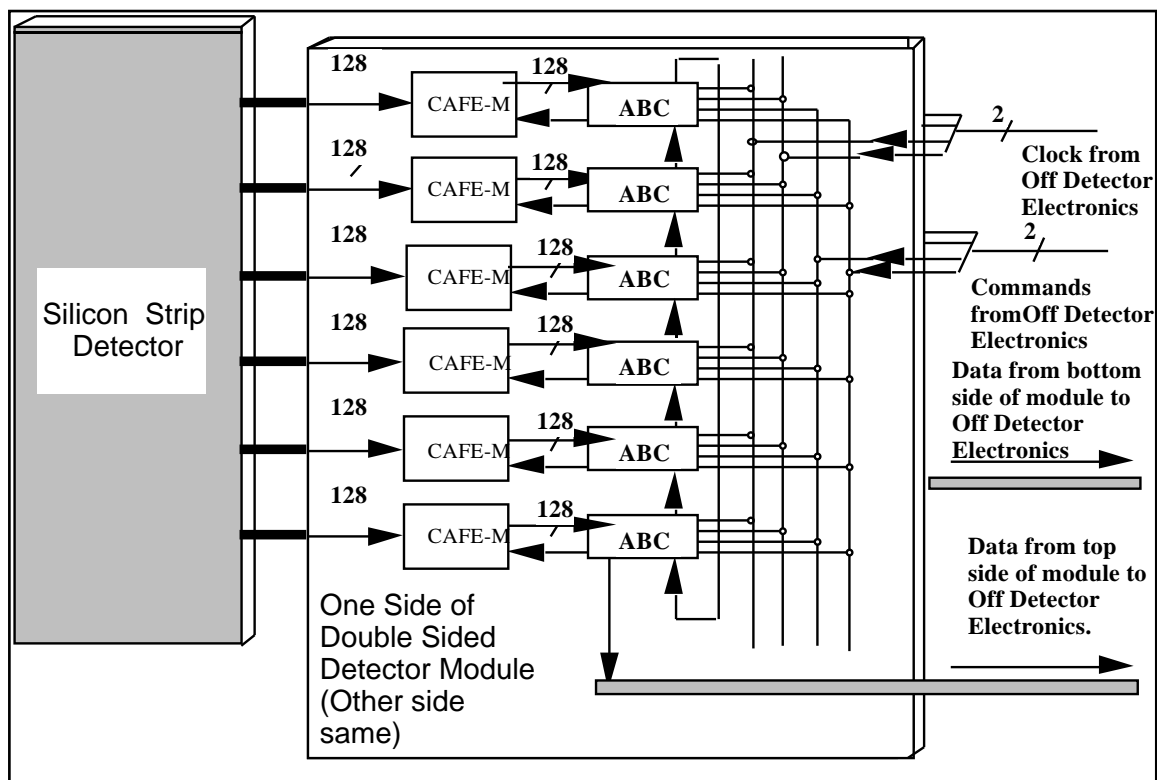


Figure 2 Diagram of a Hybrid Module

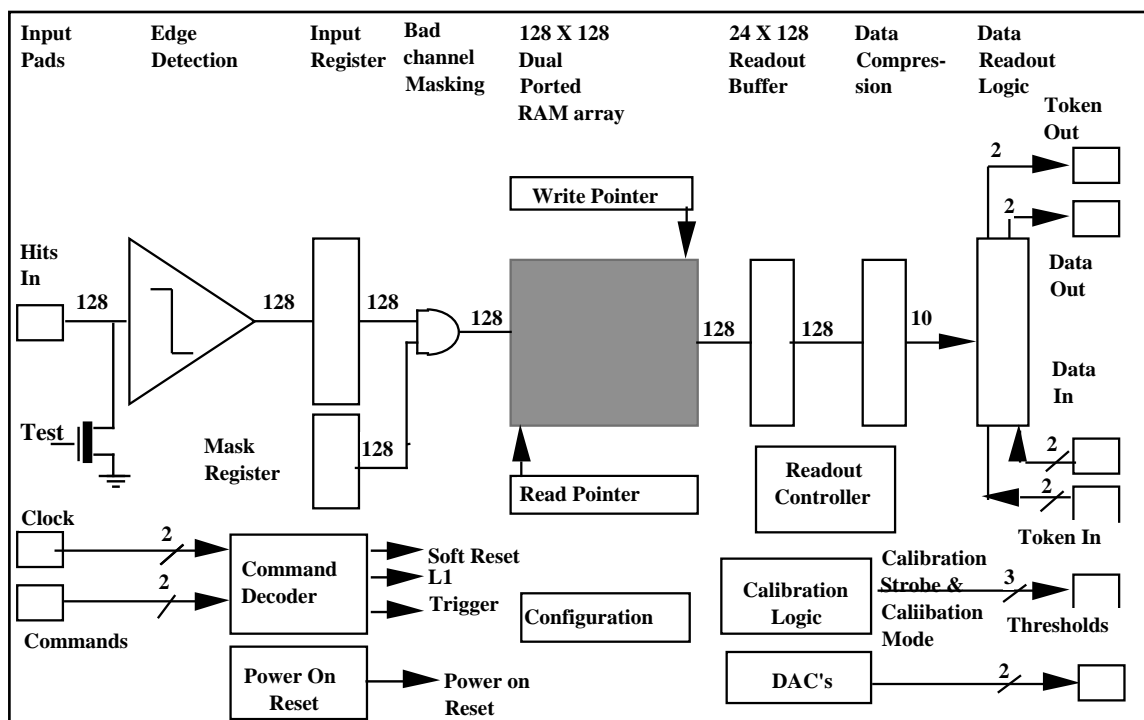


Figure 3 Block Diagram of the ABC Chip.

After the mask register, the resulting signal is sampled on every bunch crossing and stored in the pipeline. The pipeline consists of 128 locations of dual ported RAM. This block of RAM is addressed by 2 circular pointers, a read pointer and a write pointer. The write pointer is used to address the next location in the RAM into which data will be stored. The read pointer follows the write pointer by 128 locations or  $3.2\mu\text{s}$ . When a L1 trigger is received the sample being addressed by the read pointer together with the next 2 samples are copied into the readout buffer.

The readout buffer acts as a 24 location deep FIFO. It has sufficient capacity to hold the data from up to 8 events without data loss. Its purpose is to hold the data from events until they can be read out. If the capacity of the readout buffer is exceeded the oldest events in the buffer are overwritten by new ones. Logic built into the buffer tracks which events have been overwritten.

As soon as there is data in the readout buffer to be processed the 3 samples that constitute an event are transferred to the data compression logic. The function of the data compression logic is to find the data from channels which have been hit and only pass this data to readout logic for transmission off the chip. The data compression logic performs a sequential search, looking for channels which have the required hit pattern. A choice of 4 hit patterns are available. The hit pattern from every matching channel together with its address is passed to the readout logic upon request.

The readout logic on the chip has two functions to perform. Firstly, it must format the address and data into the protocol used for data transmission. This protocol adds extra bits to the data stream which enables synchronisation or framing errors to be detected. Secondly, the readout logic must send the data over the token ring connecting several chips together.

Each ABC chip contains the logic to control the readout of several chips together with the logic needed to read out the data from itself. For each group of chips one of these chips is enabled to co-ordinate the readout of data from a group of chips using a token based readout scheme.

#### 4. READOUT

In this scheme the one chip is connected to the data link and programmed to be a master. The remainder of the chips are programmed to become slaves. The last chip in the readout chain is designated as the end chip. On receipt of a L1 trigger the Master chip first outputs any data it has to send over the link. When it has completed sending its data it sends a token to the slave chip on its right. On receipt of the token the slave sends its data to the master which sends this data to the link. Once the slave has finished sending its data, it passes the token on to the next slave which then starts to send its data. This process continues until the last chip in the readout chain, the end chip, has sent its data. This chip appends a unique data packet to its data stream. When the master receives this packet it interprets it as the end of data. It is then free to initiate another readout cycle. This scheme minimises the number of connections needed on the hybrid.

The ABC chip also includes the support circuitry needed for the CAFE-M chip. This consists of two 8 bit DACs for setting a discriminator threshold and calibration value for the CAFE-M chip. It also has logic for generating and delaying a strobe pulse need by the CAFE-M chip during calibration.

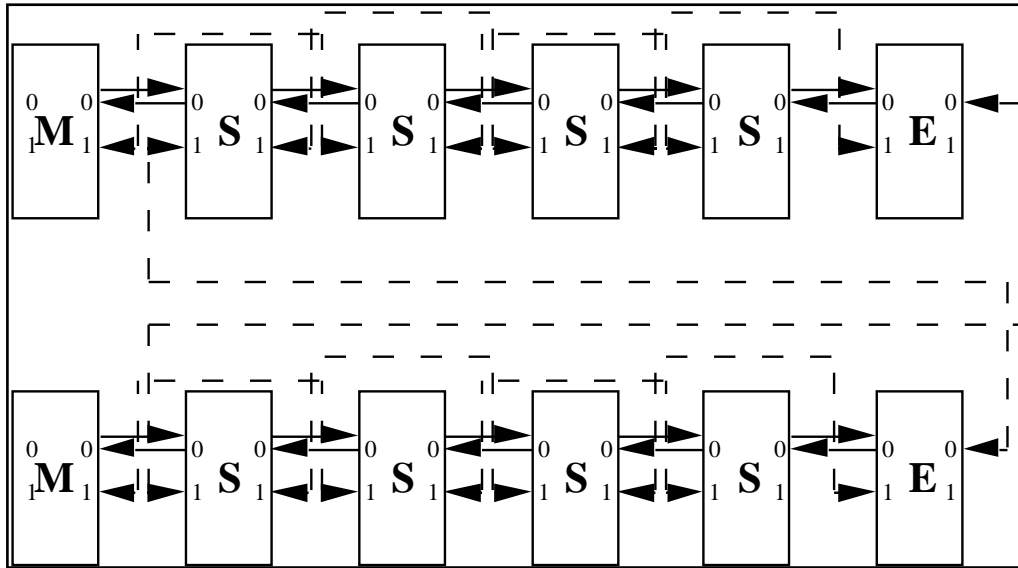


Figure 4 Token Based Readout Scheme.

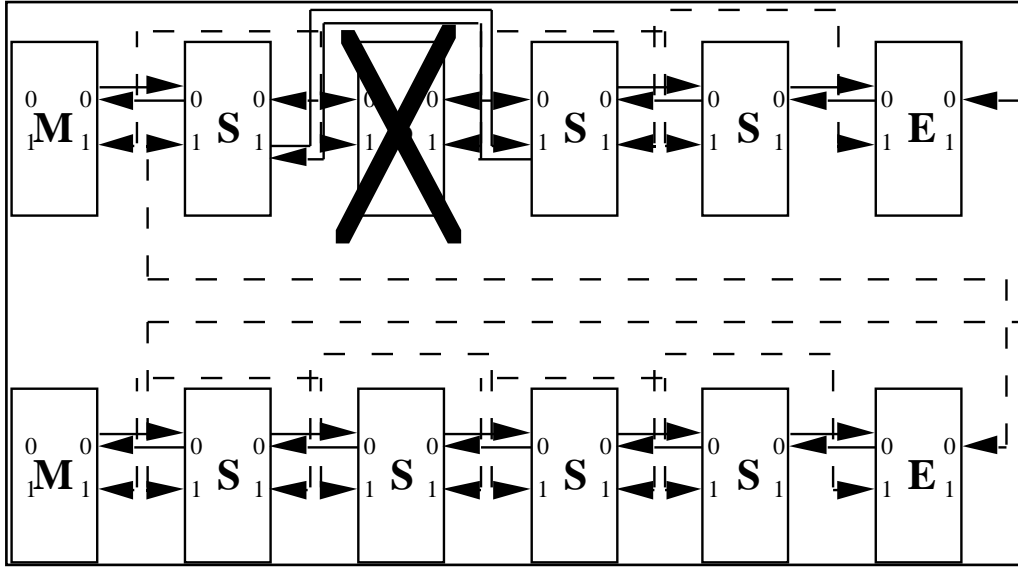


Figure 5. Readout in the case of a failed slave chip.

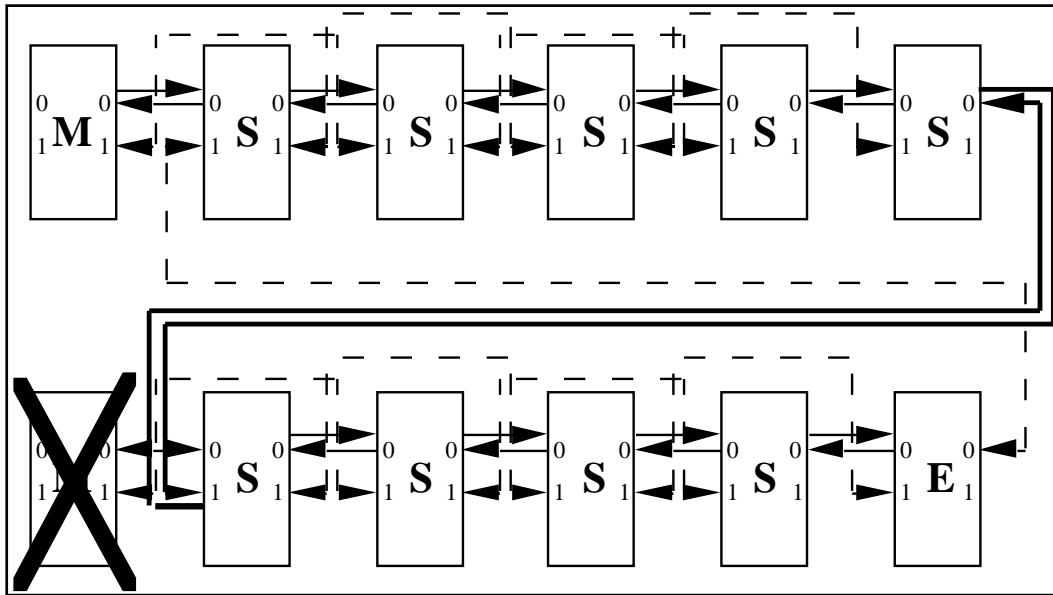


Figure 6 Readout in the case of a failed master chip.

## 5. REDUNDANCY

The ability of this system to tolerate a single point failure is one of its key features. Each chip incorporates a backup set of inputs and outputs which enable a module to continue operating in the event of a single point failure. In the case of the clock and command inputs selection between normal and backup inputs is made via a dedicated input to the chip. In the case of the token and data links these are configured by sending the appropriate slow commands to the chip.

## 6. IMPLEMENTATION

It is estimated that the CAFE-M chip will consume between 1.5 and 1.8mW per channel. The ABC chip is estimated to consume 0.5mW per channel. The CAFE-M chip will be fabricated in Maxim CB2 complementary Bipolar process [2], and the ABC chip will be fabricated in the Honeywell RICMOS4 Radiation Insensitive CMOS process. The work is being carried out on another version of the binary readout system incorporating both, the front-end and the pipeline in a single chip using the DMILL BiCMOS process [3,4].

## 7. CONCLUSIONS

A complete detailed design of the binary readout system for the ATLAS Semiconductor Tracker has been developed. The overall concept is based on the prototype chips which have been developed in the past and used successfully in the beam tests. The present development aims for a final SCT design coherent with the other SCT items like detectors, hybrids data links, readout protocol, and incorporating some tolerance to failures. The implementation work is continued along two lines employing two different technology choices, a bipolar and a rad-hard CMOS in one case and a rad-hard BiCMOS in the other one.

## REFERENCES

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