Project Specification
Project Name: **A**tlas **B**inary **C**hip (**ABC**)
Version: V3.04

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1.0 SCOPE

The aim of this project is to develop a chip suitable for the binary readout of the proposed LHC ATLAS semi-conductor tracker (SCT). This chip is to be based on the work already carried out for atlas in particular the ddr2 chip and CDP128 chip. The chip will be designed to interface to the CAFE[1] and the DORIC [2] chips in addition it must also be compatible with the protocols for receiving and sending data as defined for the atlas silicon micro-strip detector.[3]

[1] CAFE: A Complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT. Issy Kipsis
[2] DORIC. A Front End Clock and L1 Distribution Chip. J.R. Gorbold & P.Seller
[3] Proposed Protocols for Data Transmission and Control Functions for the ATLAS Silicon Micro-strip Detector

1.1 ATLAS Binary Front End Readout Architecture

The ATLAS binary front end readout architecture is based on amplifier/discriminator and CMOS pipeline chips. In one configuration this is arranged as two chips, a bipolar amplifier/discriminator chip (CAFE-B) and a CMOS pipeline chip (“ABC”). The “ABC” chip reads out 128 channels of silicon strip data from a CAFE-B chip. Data are stored for the duration of the level 1 trigger (L1) latency in a 128 deep 1 bit pipeline. In normal data taking, the data corresponding to hit strips are read out (“sparse” read out). Four modes of data read out are possible: in the level mode the decision is based on the data in the BC corresponding to the L1 trigger only but in the edge mode there must be a “0” in the channel for the bunch crossing preceding the trigger. The efficiency is highest for level mode but the occupancy may be up to a factor of two higher. The optimum mode to run will therefore depend on luminosity and therefore both modes of operation should be possible. A third mode named hit demands a "1" in any of three bunch crossings, of a given L1 trigger, the one preceding and the one following. The mode is used for beam tests and diagnostics. The final mode "read_all" places no requirements on the data. All channels are read out. This mode is used during chip testing.

In order to reduce dead time due to queuing losses all the data from an L1 trigger are transferred to an 8 deep de-randomising buffer. The dead time of the system should be less than 1% for a mean occupancy of 1% and a mean L1 rate of 100 Khz. The data from the 6 ABCs corresponding to one side of an SCT module are readout in a daisy chain via a token passing scheme. The bunch crossing clock, the L1 trigger and the other control information is sent to the chips from the DORIC chip.

In order for the system to run reliably for many years at the LHC it must be immune to single point failures. If a single ABC on a module fails then the module can be re-configured so that bypass lines are used to route data and tokens around the bad chip. If a fibre optic data transmission link fails then the data can be re-routed via the fibre optic link on the other side of the hybrid. If the clock and control link to a module fails then the clock and control can be taken from a neighbouring module. Soft errors caused by a loss of a bit in data transmission or clock & control are detected in many cases by consistency checks on the data. This is informational since the system will be reset frequently to clear such errors, rather than corrected on error detection. Errors caused by buffer overflows are detected and lost events are labelled as such in the output data stream. Although an excess data rate can cause loss of data it should never result in the data being read out for the wrong trigger.

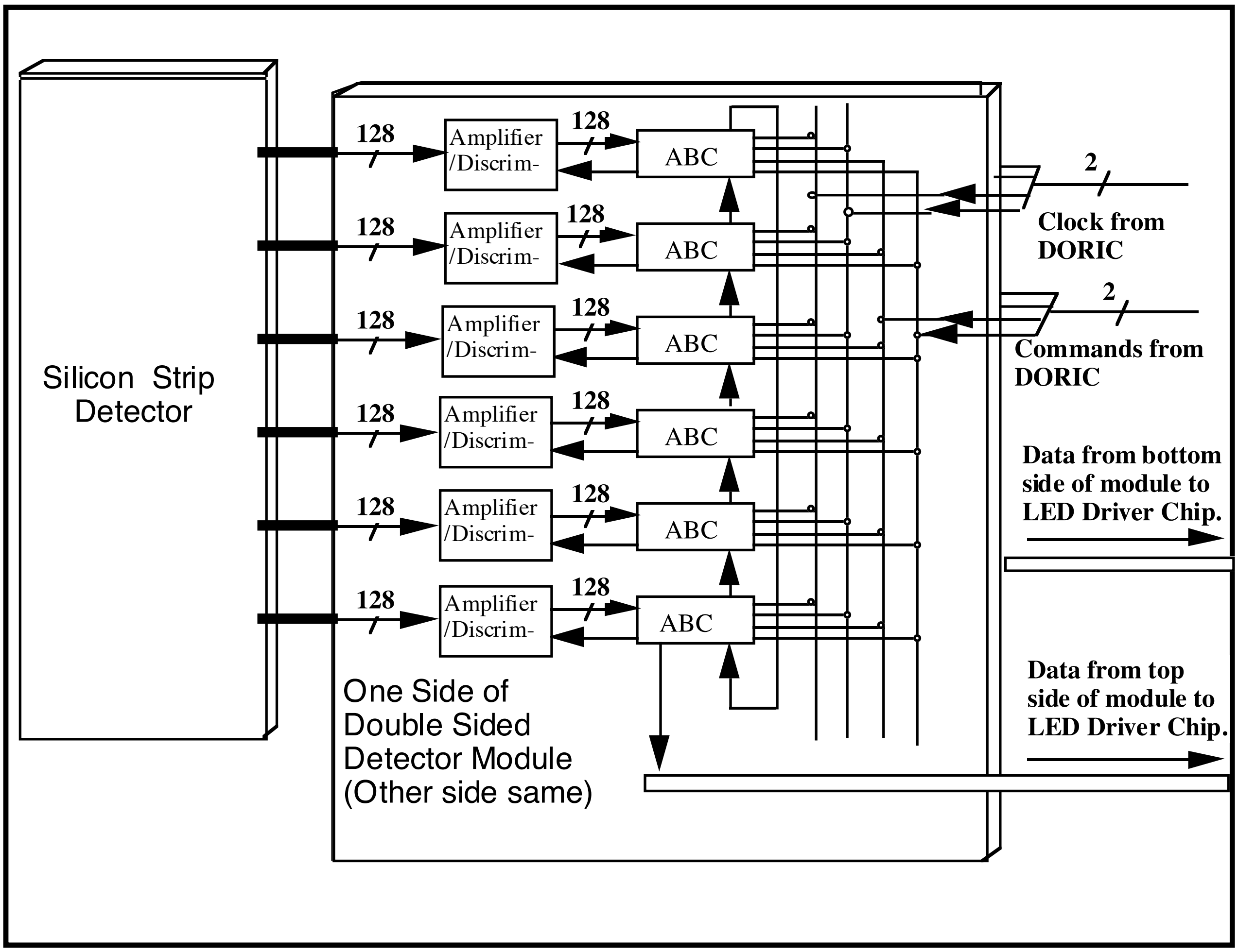

Figure 1.0 Block Diagram of the Binary Readout System

2.0 RELATED PROJECTS AND DOCUMENTS

1). DORIC. A Front End Clock and L1 Distribution Chip.
J.R. Gorbold and P.Seller.
2). Digital Read-out Chip for Silicon Strip Detectors at SDC
Kanex Shankar Nikhil Kundu et al
3) A 128-Channel Digital Pipeline Chip for Silicon Strip Detector Read-Out
Joel DeWitt
4). CAFE: A Complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT.
Issy Kipsis
5). DDR2RH Operating Manual
6). A Binary Readout System for Silicon Strip Detectors at the LHC
A.Ciocio, T.Collins
7).AROW Specification for Input Decoding v.11
J. Gorbold
8).Requirements for Wilkinson ADC Based Digitisation and Sparsification Circuits for ATLAS
Eric Evans
9).Proposed Protocols for Data Transmission and Control Functions for the ATLAS Silicon Micro-strip Detector
A.Grillo
10) Dead time calculations for SCT readout architectures. A.R. Weidberg ATLAS-INDET-124.

3.0 TECHNICAL ASPECTS

3.1 Requirements

1)The chip will be designed to accept the 128 output signals from the CAFE amplifier and comparator chip

2)At the start of each clock cycle the chip must sample the outputs from the CAFE and store these values in a pipeline until a decision can be made whether to keep the data.

3) Upon receipt of a Level 1 Trigger signal the corresponding set of values together with it's neighbours are to be copied into another buffer, the readout buffer.

4) The data written into the readout buffer is to be compressed before being transmitted off the chip.

5) Transmission of data from the chip will be by means of a token ring and must be compatible with the Atlas protocol.

6) The chip will be responsible for supplying the CAFE chips with their calibration pulses.

7) The chip is required to provide reporting of some of the errors that occur
   1) Attempt to readout data from the chip when no data available.
   2) Readout Buffer Overflow. The readout buffer is full and data from the oldest event/s has been overwritten.
   3) Readout Buffer Error. The readout buffer is no longer able to keep track of the data held in it. (Chip reset required)
   4) Configuration error (ChipID sent).

8) The chip will incorporate such features that will enable it to be tested both at the wafer level and in situ.
   Test include but are not restricted to :
   a) the functionality of input level translators
   b) transmission of programmable pattern through the pipeline and readout circuitry.

9) The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure.

10) It is a system requirement that the fraction of time during which data is lost due to the readout buffer on the chip being full is less than 1%. This assumes that on average only 1% of the silicon strip detectors are hit during any particular beam crossing.

11) DACs will be included on the chip to enable the thresholds of the comparators on the CAFE chip to be set.

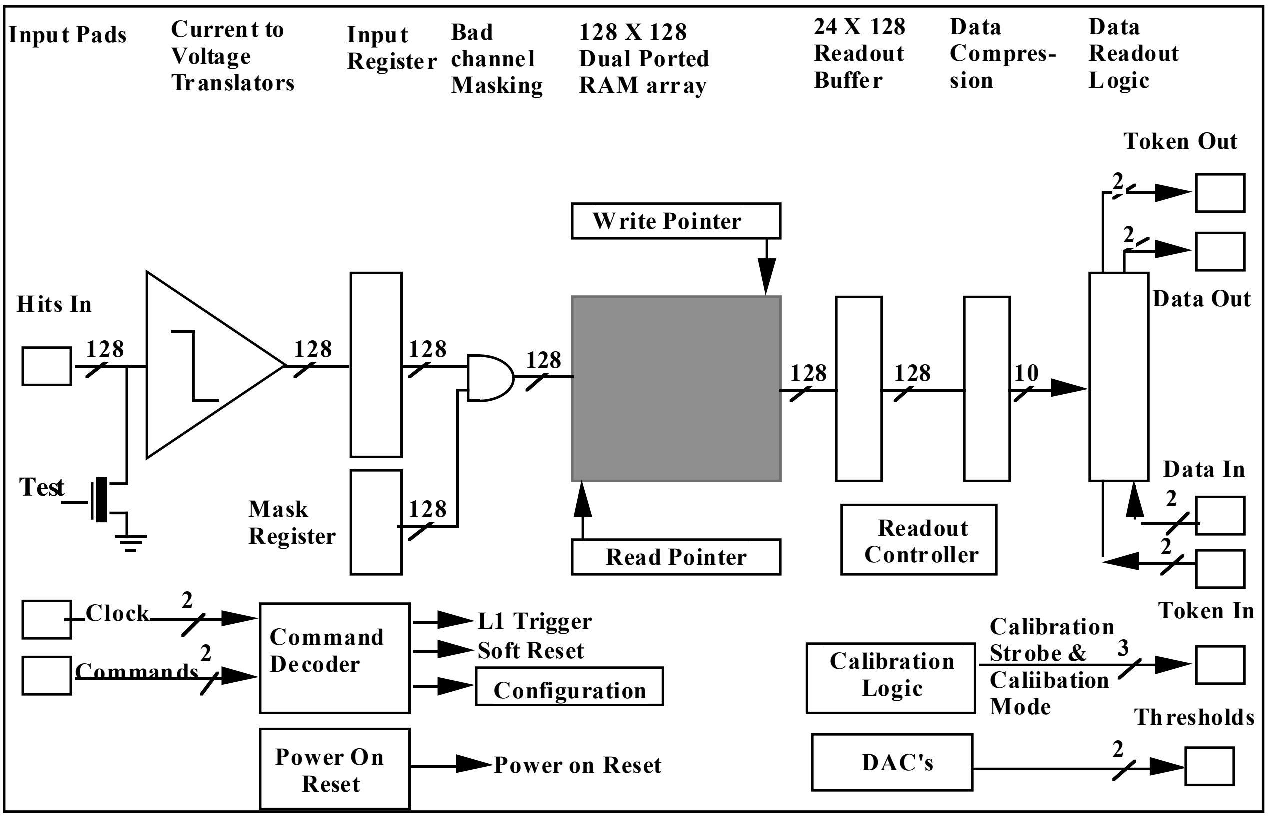

Figure 3.1 Block Diagram of the Binary Readout Chip

3.2 Specification of deliverables

3.2.1 Input Level Translators

The outputs from the CAFE chip, which are fed to the inputs of the Binary Readout Chip are open collector to enable a low voltage swing current mode interface to be formed between the two chips. The input level translators on the Binary Chip must provide a source of current which can be sunk by the outputs of the CAFE chip. These inputs must also be able to detect the amount of current sunk by the individual outputs of the CAFE chip and translate it into the logic levels used inside the Binary Readout Chip. The input impedance and circuit response time must ensure transition times <2nS on both the rising and falling edge. The effective threshold is set by a reference current provided by the CAFE chip. The design of these inputs is such that the chip is operational with inputs floating or shorted to ground. Built into the block will be the facility to selectively set a quarter of the input channels at a time to the level of a hit channel. This facility is required to enable the inputs to the chip to be tested without the need to probe all input pads.

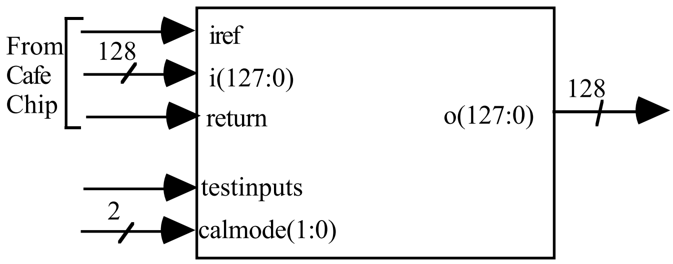

Fig 3. 2 Input Level translators Inputs/Outputs

Table 3.1 Input Level Translator I/O Signal Definitions

Signal Name	Active State/Edge	Function
iref		Current reference (from CAFE chip)
i(127:0)		Hit Inputs (from CAFE chip))
return		Signal Return (to CAFE Chip)
testinputs	High	Enables testing of inputs
calmode(1:0)		Selects group of channels to be tested
o(127:0)		Data Outputs (to input reg.)

Table 3.2 Test Modes

testinputs	calmode(1)	calmode0)	Channels of Chip Tested
0	X	X	Testing disabled
1	0	0	in0, in4 in8,...in124
1	0	1	in1, in5 in9,...in125
1	1	0	in2, in6 in10,...in126
1	1	1	in3, in7 in11,...in127

N.B. The calmode bits are also used for selecting the calibration mode of the CAFE chip (see section 3.2.10)

3.2.2 Input Register and Mask Register

The functions of the input register and mask register will be implemented in a single functional block. The input/output connections to this block are shown in Fig 3.3

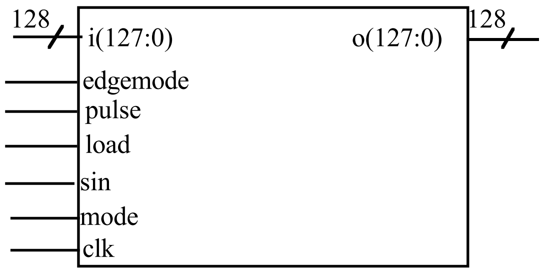

Fig 3.3 Input Register Inputs/Outputs

Table 3.3 Input Register I/O Signal Definitions

Signal Name	Active State/Edge	Function
i(127:0)		Hit Inputs (from input translators)
load	Active High	
sin		Configuration Data Inputs
mode	see table 3.4	
clk	Pos Edge	
o(127:0)		Data Outputs (to pipeline)
edgemode	High	Enables edge detection logic.
pulse	High	Forces Input register to output a test pattern while the pulse input asserted

3.2.2.1 Input Register

This register latches the incoming data, delivering a well defined pulse width to the pipeline.

3.2.2.2 Edge Detection Circuitry

The function of this block is to detect a low to high transition in the data entering the chip, and for each of such transition found the block outputs a pulse of duration 1 clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single '1' is written into the pipeline for every hit detected regardless of the response time of the CAFE chip. This circuitry can be turned on or of by setting the appropriate bit in the configuration register.

3.2.2.3 Channel Masking Register

This register serves a dual purpose. Firstly the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate to a level which would create dead-time from errors. Secondly it can be used during chip testing to apply a set of test patterns to the pipeline. The contents of this register can be changed by sending the appropriate control command to the chip.

Table 3.4 Masking Register Modes of Operation

mode	Mode of Operation
0	Normal Data Taking (Contents of register used to "Mask Inputs")
1	Test Mode (Contents of mask register are used to supply test values to pipeline)

3.2.2.4 Input Register Pulsing

The pulse input forces all the outputs of the Input register to go to a high level when asserted. The pulse input will is asserted for a duration of 1 clock cycle in response to the appropriate slow command being received by the chip. The purpose of this function is to facilitate the testing of the pipeline (see next section)

3.2.3 Pipeline

This consists of a block of dual ported RAM 128-bits wide by 128 locations deep. This must run at 40MHz. The RAM block is addressed by an address pointer. During data taking the chip is instructed to write into the RAM and increment the address pointer every clock cycle. When the address register reaches a count of 127, it automatically resets itself on the following clock cycle. When a level one trigger arrives, the hit-pattern from the appropriate time bin is copied into the readout buffer together with the hit pattern from the previous and next clock cycle. Incorporated into the pipeline is the accumulator register. This function can be enabled and disabled by setting a bit in the configuration register.

3.2.3.1 Accumulator Register

This is a 128-bit wide register used for accumulating hits in the pipeline. This register marks all channels that have been hit since it was last cleared. If the Accumulator Mode is selected in the configuration register, a L1 trigger results in the transfer of the contents of this accumulator into the readout buffer instead of the appropriate time bin of the pipeline. This accumulator column is cleared by a power-up or soft reset command.

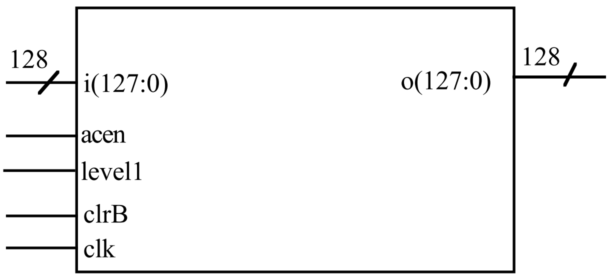

Fig 3.4 Pipeline Input/Outputs

Table 3.5 Pipeline Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
i(127:0)		Data Input
acen	High	Enables Accumulator Register
level1	High	Reads Value out of pipeline
clrB	Low	Initialises pipeline pointers and clears accumulator register
clk	Pos edge	Clock input
o(127:0)		Data Output

3.2.4 Readout Buffer

Data corresponding to each L1 trigger will be held in a Readout buffer pending readout. This data buffering is needed to remove the statistical fluctuations in the arrival time of L1 triggers. Data compression and read out will be started only when this buffer is not empty. Three bits of data will be stored in this buffer for each channel per L1 trigger. These bits represents the three beam crossings centred on the L1 trigger time and are set if the input was above threshold during the corresponding crossings. In the case when the Accumulator Register has been enabled, the contents of this register will be copied into the buffer 3 times resulting in the same amount of data being written into the readout buffer regardless of the operating mode. This buffer will be 128 bits wide by 24 locations deep. This is sufficient to hold the data from eight L1 triggers. This satisfies the ATLAS specification of maintaining <=1% data loss at a L1 trigger rate of 100 KHz and a strip occupancy of up to 1% [10].

RAM and Pointers
This buffer will be implemented as a "barrel store" i.e. it will be addressed by 2 cyclic pointers, a write pointer and a read pointer. Once a pointer has reached the end of the block of RAM , the next time it is incremented it will return to the beginning of the block of RAM.

The write pointer will be allowed to go past the read pointer and over-write data that has not yet been read out. However if this happens the Overflow flag will be set to indicate that data has been over-written. The read pointer will not be allowed to pass the write pointer and if the read pointer should catch up with the write pointer the EMPTY flag will be set. This is to prevent attempts to readout the buffer when there is no data in it.

Overflow Counter
A counter will be used to track the number of events that have been over-written in the buffer. This counter will be incremented for every time an event is written into the buffer while the buffer is full. The outputs from this counter represents the number of events from which data has been lost. This counter is decremented for every event that is readout of the buffer, until it's value reaches zero. Once it's value has reached zero it is no longer decremented. This is because in this state all the events from which data has been lost will have been cleared and none of the data in the buffer will have been overwritten. Should this counter overflow the ERROR flag will be set This will occur after 21 events have been overwritten. This flag will remain set until either a software reset, or power-up resets has been issued to the readout buffer and associated logic.

Flag Logic
Three signals EMPTY, OVERFLOW and ERROR are produced by the readout buffer. Empty indicates when there is no data in the buffer to be readout. This signal is used by the Data Compression logic to determine when to start a readout cycle. OVERFLOW indicates when data in the buffer has been overwritten and hence data lost. This signal is sent to the readout logic which results in the readout logic sending an error message to say that data from the current event being readout has been lost. Finally the ERROR signals is generated when the buffer has overflowed and it has also lost track of the number of events from which data has been lost. This flag can only be cleared by issuing a reset to the chip.

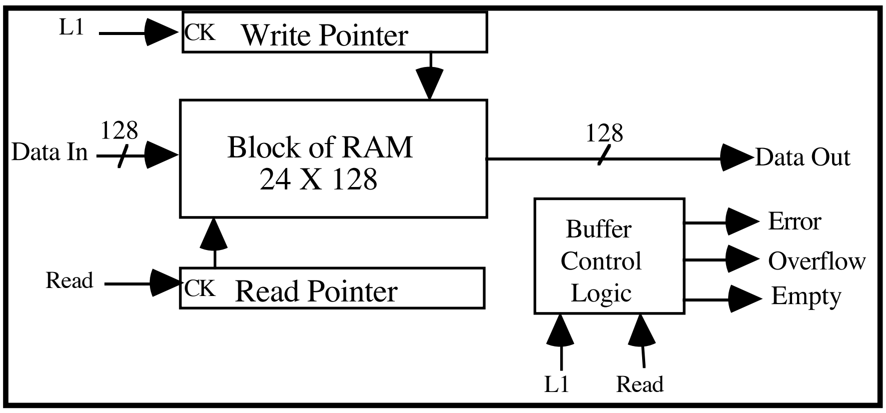

Fig 3.5 Block Diagram of the Readout Buffer

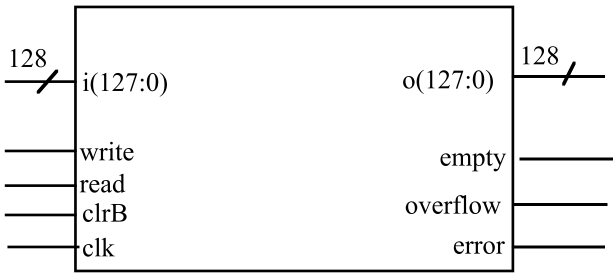

Fig 3.6 Readout Buffer Input/Outputs

Table 3.6 Readout Buffer Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
i(127:0)		Data Input
write	High	Write value into readout buffer
read	High	Reads value from readout buffer
clrB	Low	Resets buffers pointers and counter
clk	Pos edge	Clock input
o(127:0)		Data Output
empty	High	Buffer Empty
overflow	High	Buffer Overflow
error	High	Buffer Error

3.2.5 Data compression logic

It is anticipated that on any event very few channels will contain hits. This fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each group of 3 bits is compared against one of 4 selectable criteria. If the pattern meets the criteria then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This process is repeated until the hit patterns from all 128 channels have been examined. The following table shows the 4 selection criteria, (currently there are only plans to use 3 the 4th is for chip testing only)

Table 3.7 Data Compression Criteria

mode(1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Test	XXX	Test Mode

N.B. X = Don't care state.

This block operates as follows.

As soon as the chip receives a L1 trigger the three 128-bit words that make up an event are written into the read out buffer. This results in the empty flag on the readout buffer being negated, indicating that there is data to be processed. The data compression logic monitors the state of this flag until it finds that there is data available. Providing that it is not already processing data it then proceeds to read in the three 128-bit words that make up an event from the readout buffer.

The next thing that happens is that the data compression logic re-arranges the order of the data from being 3 128-bit words into 128 3-bit words. The reason for this is that the data compression algorithm requires all 3 samples of an event to be examined in parallel.

The data compression logic then starts to scan through all the channels in turn until it finds one which has a pattern of hits which matches the data selection criteria. If it finds such a pattern of hits it asserts the "datavalid" signal and places the pattern of hit bits on the "hit<2:0> " outputs and places the address of the hit channel on the address outputs "ch<6:0>". The logic then waits until the readout logic signals it to proceed by asserting the "next" input. The data compressin logic responds to next by presenting the address and data for the next hit found if any. If the next hit found is on the next adjacent channel the "adj" is asserted with the data from the previous channel.. If no more hits are found ,the "end" signal is asserted.

In certain situations e.g. in the case of a overflow of the readout buffer, it is not necessary for the Data compression logic to process the data from the readout buffer but it is still necessary for it to read the 3 values from the buffer in order tot flush them from the readout buffer. There are 3 cases when this happens

1) When the Readout Buffer overflow flag has been set.

2) When the Readout Buffer error flag has been set.

3) When the chip is chip is in its SEND_ID mode of operation.

The following table shows how the datavalid, end and overflowout outputs are used to indicate the status of the Data compression logic

Table 3.7a Data Compresion Logic Output States

datavalid	end	overflowout	condition
low	low	low	no events available to be read out i.e readout buffer empty.
high	low	low	data from hit channel waiting to be read out. (not last channel)
high	high	low	data from last hit channel waiting to be read out.
low	high	low	all hits read out or no hits found
low	low	high	data for event lost due to readout buffer overflow

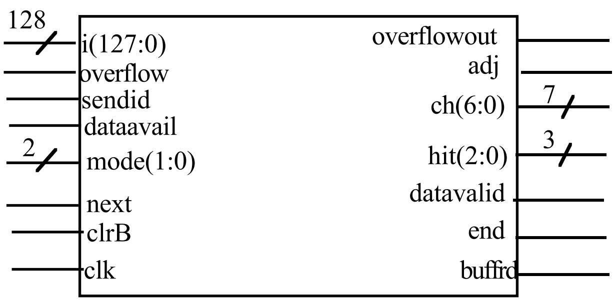

Fig 3.7 Data Compression Logic Input/Outputs

Table 3.8 Data Compression Logic Input/Output Signal Definitions

Signal Name	Input/Output	Active State/Edge	Function
i(127:0)	input		Data Input
overflow	input		Overflow output from readout buffer
sendid	input		indicates chips mode of operation
dataavail	input	High	Data available to be readout
mode1:0)	input		Selects data compression mode
next	input	High	Find next hit channel.
clrB	input	Low	Resets logic
clk	input	Pos Edge	Clock Input
overflowout	output	High	Overflow output to readout circuitry
adj	output	High	Next Hit found on adjacent channel
ch(6:0)	output		Channel address of Hits
hit(2:0)	output		Hit Data pattern
datavalid	output	High	Hit Data outputs valid
end	output	High	Last Channel scanned
buffrd	output	High	Reads Value out of Readout Buffer

3.2.6 Readout Circuitry

The readout circuitry will be responsible for capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives. On arrival of the token it checks if any hits have been found by the data compression logic. If so, it then outputs the appropriate header information. It then proceeds to output the address of the hit channel together with the data from that channel. Once the readout circuitry has finished sending the data from one channel it proceeds to output the data from then next channel. In the situation were one or more neighbouring channels are to be read out, only the address of the first channel is output., but the data from all hit channels is sent. This process continues until the data compression logic indicates that all channels have been examined by asserting "end". Once all the data corresponding to a single event has been read out, a token is sent out to the next chip in the readout chain. This token will be sent out ahead of the last bit of data sent out. If the chip has no data to be readout circuitry sends out a "No hit data " packet and passes the token on to the next chip in the chain.

If the chip is in "send-id" mode or the readout buffer has overflowed or generated an error condition, the readout circuitry sends the appropriate error packet or configuration data packet. In these cases the readout circuitry is still required to signal to the data compression logic that it has processed an event by asserting the "next" signal. This operation is needed so that a correct count of the number of events waiting to be read out can be maintained.

In the case of an error condition occurring e.g. attempt to readout data and no data available, the appropriate error code will be sent by the readout logic. If the chip is in the "send_id" mode of operation, no data or error codes are output from the chip but instead a special packet of data containing information about the chips current configuration is sent..

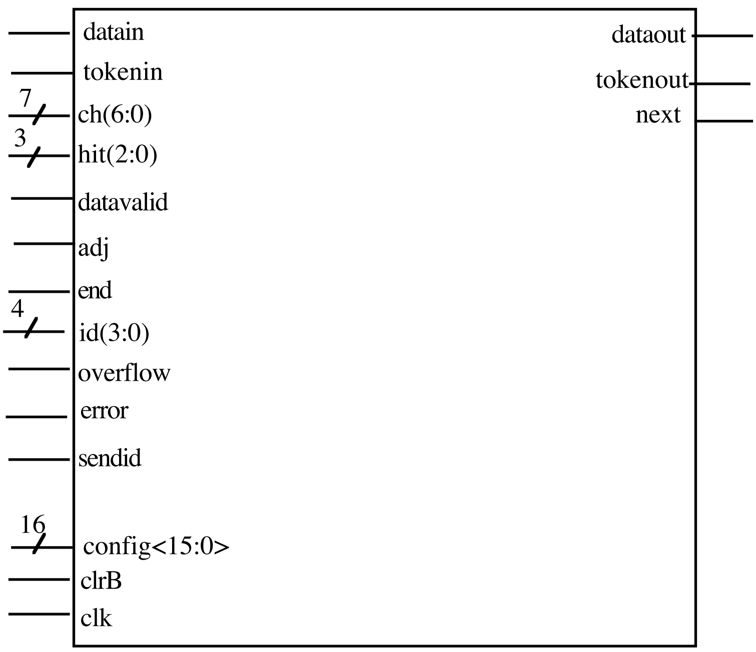

Fig 3.8 Connections to Readout Circuitry

Table 3.9 Readout Logic Input/Output Signal Definitions

Signal Name	Input/Output	Active State/Edge	Function
datain	input		Data Input
tokenin	input	High	Token Input
ch(6:0)	input		Address of Hit Channel
hit(2:0)	input		Hit data pattern
datavalid	input	High	Data available for sending
adj	input	High	Hit found on adjacent channel
end	input	High	End of data to be sent
id(3:0)	input		LS 4 bits of chip address
overflow	input	High	Readout buffer Overflow
error	input	High	Readout Buffer Error
sendid	input		Chip mode of operation
config<15:0>	input		Data from config-reg
clrB	input	Low	Resets circuit
clk	input	Pos Edge	Clock input
dataout	output		Data output
tokenout	output		Token Output
next	output	High	Scan Next Channel

3.2.7 Readout Controller Block

This block is to control the readout of data several ABC chips connected together in a token ring. This block is enabled by placing the chip in "Master Mode". This block has to detect when a L1 trigger has been received. Issue a token to all the ABC chips connected to it Collect all the data from these chips and tag the data with the Beam crossing number from which it came and the number of Level 1 Trigger. This block then has to transmit this data serially to the LED driver chip.

3.2.7.1 L1 Counter

This a 4-bit binary counter which is incremented every time the chip receives a level 1 trigger. The counter is zeroed by either a hardware reset or a software reset.

3.2.7.2 Beam Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either a hardware reset, a software reset., or a special BC Reset Command

3.2.7.3 Event FIFO

This is a 29 location deep 12-bit wide FIFO. Each time the chip receives a L1 trigger the output of the L1-Counter and the Beam crossing counter are loaded into the FIFO prior to the counters being incremented. These values are read from the FIFO every time an Event is readout and are used to tag the data with 12-bits of information about which trigger number and beam crossing number the data came from.

3.2.7.4 Token Generation Logic

The purpose of the token generation logic is to detect when the chip has received an L1 trigger and to generate a token to initiate the read out of data from that L1 trigger. This logic waits until the Event FIFO become not empty and it then issues a token . It then waits until the token has come back before checking to see if the Event FIFO empty. If the Event FIFO is still not empty it repeats the cycle.

3.2.7.5 Data Formatting Logic

The purpose of this logic is to attach the header information to the packets of data output from the chip on the Serial Data Output.

3.2.7.6 Serial Data Output Driver

This is the output from the chip outputs its data to the DAQ system.

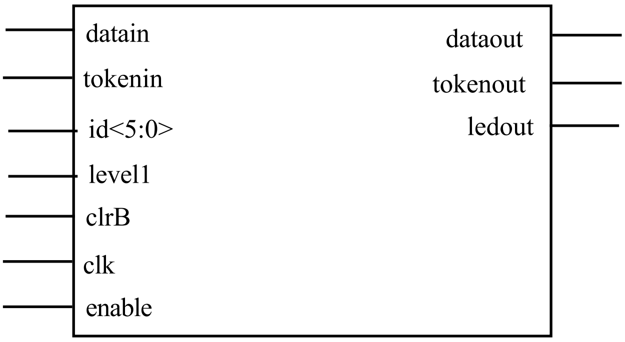

Fig 3.9 Connections to Readout Controller Circuitry

Table 3.10 Readout Controller Input/Output Signal Definitions

Signal Name	**Active State/Edge**	**Function**
datain		Serial Data Input
tokenin	High	Token Input
id<5:0>		Address of chip
level1	High	Level 1 Trigger
enable	High	Enables Controller block
clrB	Low	Resets block
clk	Pos Edge	Clock input
dataout		Serial data output
tokenout	High	Token Output
ledout		Serial data out to LED driver

33.2.8 Command Decoding

The command and control information all comes into the chip on the control input pin. There are two main classes of information which arrive here, which must be separated. Depending on which class arrives further information may follow. This will also need decoding, formatting and sending to the appropriate functional blocks of the chip. These two classes of information are:

Level 1 Trigger Command

If this command is received the control logic writes 3 samples from the pipeline or the accumulator register, into the Readout Buffer.

Fast Command

If this command is received, the second field of 4 bits is decoded and the appropriate command is executed. No address or data fields are included in these commands..

Slow Control Command

In this case the contents of the 5th Data field in the instruction is decoded, and the data value contained in the 6th data field is loaded into the appropriate register

The command decoder block is required to decode the command and sends the relevant instruction and data to other parts of the chip. The input/output connections to this block are shown in fig 3.10.

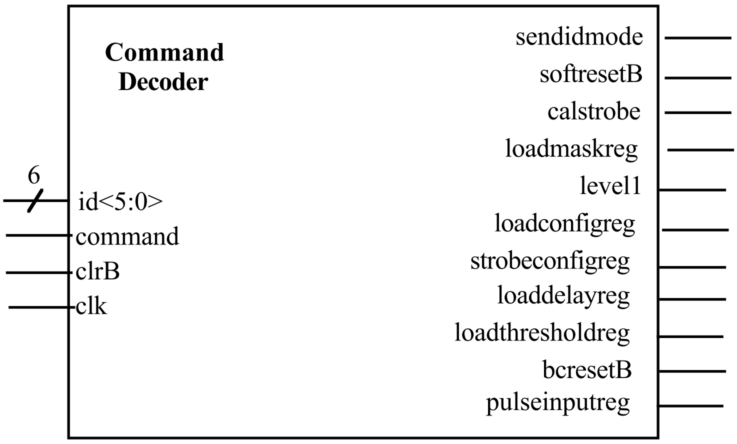

Fig 3.10 Command Decoder Inputs/Outputs:

Table 3.11 Command Decoder Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
id<5:0>		Chip ID
command		Command Data Input
clrB	Low	Reset Block
clk	Pos Edge	Clock Input
sendidmode		Sets chips mode of operation
softresetB	Low	Software controlled reset
calstrobe	High	Send Calibration pulse to CAFE
loadmaskreg	High	Load Mask Register
level1	High	Level_1 Trigger received
loadconfigreg	High	Loads Configuration reg.
strobeconfigreg	High	Strobes data into configuration reg
loaddelayreg	Highe	Load Strobe Delay Register
loadthresholdreg	High	Load Threshold Register
bcresetB	Low	Beam crossing reset

3.2.9 Configuration Register

This is a 16-bit register which is used to hold information about the chip's current configuration. The following table defines the usage of the bits in this register. The power up value of this register will be zero. The input/output connections to this block are shown in fig 3.11

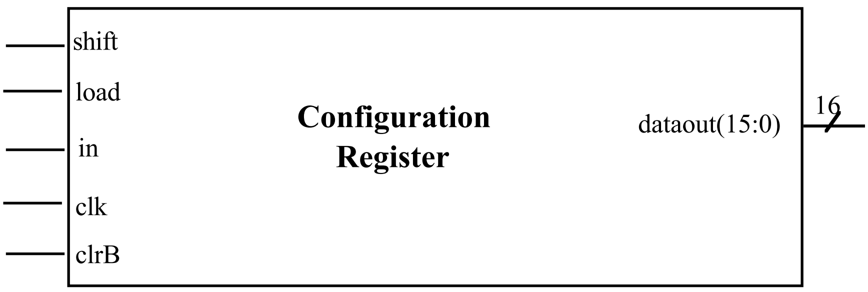

Fig 3.11 Configuration Register Inputs/Outputs

Table 3.12 Configuration Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
load	Pos Edge	Transfers data to register outputs
in		Serial Data input
shift	High	Enables data to be shifted into reg
clrB	Low	Resets register to default values
dataout(15:0)		Data Outputs See section 3.2.5

Table 3.13

Bit	Name	Function
0-1	Readout Mode	Selects the data compression Criteria (see table 3.7)
2-3	Cal_Mode(1:0)	Selects the Calibration code for the CAFE chip (see table 3.14). The state of these two bits also determines which channels are tested when Test Mode is enabled. (see table 3.2).
4	Cal_Enable	When this bit is set the calibration strobe output to the CAFE chip is enabled
5	Test_Mode	When this bit is set test values are applied to the channels defined by bits 2 & 3 of this register.
6	Edge_Detect	When this bit is Set the edge detection circuitry in the input stage is enabled.
7	Mask	When this bit is set the input register is disabled and the contents of the mask register are routed into the L1 pipeline.
8	Accumulate	When this bit is set the Accumulate function is enabled. (see section nnn)
9	Input_Bypass	This bit determines which set of token/data inputs are active.(see section nnnn)
10	Output Bypass	This bit determines which set of token/data outputs are active.(see section nnnn)
11	Master	Enables Readout Controller Logic on Chip*
12	End	When the chip is acting as a slave this bit configures the chip as the end of a chain.
13	Feed_Through	Enables Clock Feed Through Mode if the chip has been configured as a Master
14		reserved
15		reserved

* This bit is "x-ored" with the value on the "masterB" input. If the resutl is "0" the chip is placed into slave mode otherwise it is placed into master mode.

3.2.10 Calibration Logic

The calibration logic produces a calibration strobe signal for the CAFE chip This strobe is produced in response to a control command when the "Cal Enable" bit is also set in the configuration Register. A two-bit calibration code is also sent to the CAFE chip which selects one of the four possible patterns in the CAFE chip. The two-bit calibration code outputs are single-ended CMOS levels. The calibration Strobe is a differential current output. The calibration Strobe signal must be sent to the CAFE chip a fixed number of clock pulses after receipt of the control command. The phase of the strobe signal relative to the clock edge will be adjustable via an 8-bit register which can be loaded via another control command. The precision of the delay is not critical as long as it spans the period of one clock period.

Table 3.14 Calibration Codes

Cal enable Bit	Cal Mode Bit 1	Cal Mode Bit 0	Channels of Cafe Chip Pulsed
0	X	X	Calibration disabled
1	0	0	in3, in7 in11,...in127
1	0	1	in2, in6 in10,...in126
1	1	0	in1, in5 in9,...in125
1	1	1	in0, in4 in8,...in124

3.2.11 Strobe Delay Register

The Strobe Delay Register is an 3 bit register which enables the rising edge of the Calibration Strobe output to the CAFE chip to be delayed in eight, 4nS steps relative to the rising edge of the clock input.

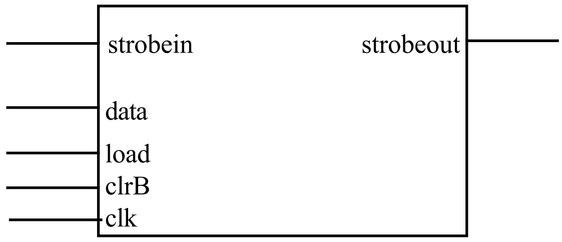

Fig 3.12 Strobe Delay Register Inputs/Outputs

Table 3.15 Strobe Delay Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
strobein		Strobe input
data		Data input to register
clrB	Low	Resets register
clk	Pos Edge	Clock input
load	High	Loads delay value into register
strobeout		Delayed version of STROBE_IN

Table 3.15a Strobe Delay Values

Delay Register Setting	Strobe Delay (Relative to Pos edge of clock)
000	0nS
001	4nS
010	8nS
011	12nS
100	16nS
101	20nS
110	24nS
111	28nS

3.2.12 Threshold Register

The threshold register is a 16 bit register which holds 2 8-bit values. A high threshold value is held in the MS byte of this register and the low threshold value is held in the LS byte of this register. The outputs of this register are used to control 2 separate 8-bit DACs. The outputs from these DACS supply 2 independent threshold levels to the CAFE chip.

Fig 3.13 Threshold Register Inputs/Outputs

Table 3.16 Threshold Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
load	Pos Edge	Load Values into register
data		Data input to register
clrB	Low	Resets register
clk		clock input to register
highthreshold		High Threshold Output from 1st DAC
lowthreshold		Low Threshold Output from 2nd DAC

3.2.12a Low and High Threshold DACs

Theses are two 8-bit DACs which are used to set high a low threshold values supplied by the ABC chip to the CAFE chip. These DACs will receive an input reference current "iref" from the CAFE chip. This reference current will be scaled at the output of the DAC by a value of 0 to 255 depending on the setting of the threshold register.

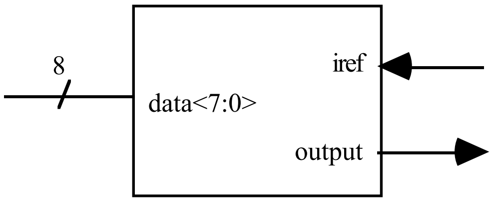

Fig n I/O connections to Threshold DACs

3.2.13 Clock and Command Inputs

Two sets of clock and command inputs will be provided in order to make the system in which the "ABCs' will be used fault tolerant and to provide an additional method of setting up the timing of the system. Each chip will be supplied with two independent sources of clock and commands. In the event of the fall out of one of these sources the alternative source can be used. An external input to the chip "clkselect" will be used to determine which pair of inputs will be used by the chip.

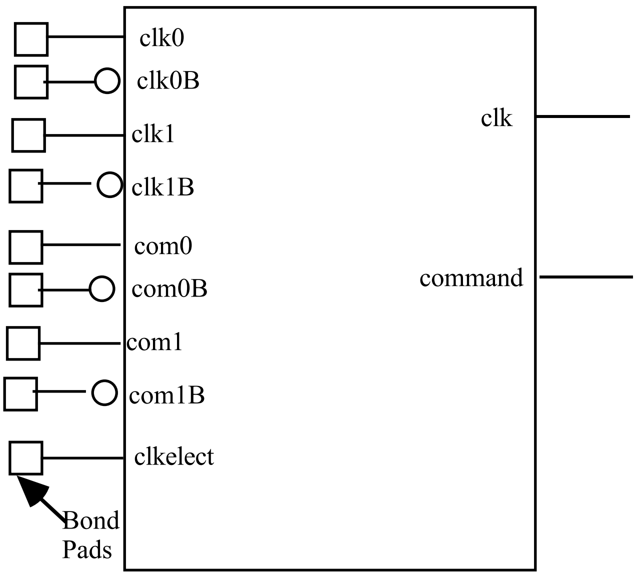

Fig 3.14 Clock & Command Data Inputs

Table 3.17 Clock Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
in0		1st Clock/Command Data Input
in0B		Complement of above
in1		2nd Clock/Command Data Input
in1B		Complement of above
clkselect		Selects which pair of inputs to use
clk		Clock output
command		Command Data Output

Table 3.18 Clock Input Modes of Operation

clkselect	clk	command
Low	clk0	com0
High	clk1	com1

3.2.14 Chip ID.

To enable a chip to be individually addressed six inputs (ID(5:0) will be used to implement a geographical addressing scheme. This is because there will be a total of 12 chips on each module (6 a side), and under certain conditions it may be necessary to address all the chips on 2 modules using the same control line. These inputs will be wire bonded to a unique set of logic levels on each chip mounted on the detector module. This set of logic levels will form a geographical address which will enable individual chips on the module to be addressed. The chips will be bonded according to the following scheme. For Historical reasons the geographical address using 6-bits even though not all these bits are essential. Internal pull ups on these inputs will force these inputs to go to a logic '1' level if left unconnected.

Table 3.19a Geographical Addresses (ID(5-0)

id(5:0)	Type of Chip Selected	Side of Module	Odd/Even Module
010aaa	ABC	Top	Even
011aaa	ABC	Bottom	Even
110aaa	ABC	Top	Odd
111aaa	ABC	Bottom	Odd
111111	All ABC chips	Top and Bottom	Both

N.B aaa is the 3 bit address of the ABC chip on any one side of a module see table 3.19b

Table 3.19b ABC Geographical Addresses (ID2-0)

Chip Position	ID(2)	ID(1)	ID(0)
1st	LOW	LOW	HIGH
2nd	LOW	HIGH	LOW
3rd	LOW	HIGH	HIGH
4th	HIGH	LOW	LOW
5th	HIGH	LOW	HIGH
6th	HIGH	HIGH	LOW
7th	HIGH	HIGH	HIGH
8th	LOW	LOW	LOW

.3.2.15 Token Input/Output Circuit

In order to provide some measure of fault tolerance in the system, a token and data bypass circuit will be built into each chip. The purpose of this circuit is to enable a chip to source or send it's token and data to another chip other then it's direct neighbours. Each chip will have 2 token and data inputs. It will also have two token or data outputs. Pairs of inputs and pairs of outputs will be connected to different chips enabling it to send or receive data from one of two chips. In this way should one of chips neighbours fail an alternative chip can take its place. Commands are used to direct each chip to use its normal or bypass inputs and outputs.

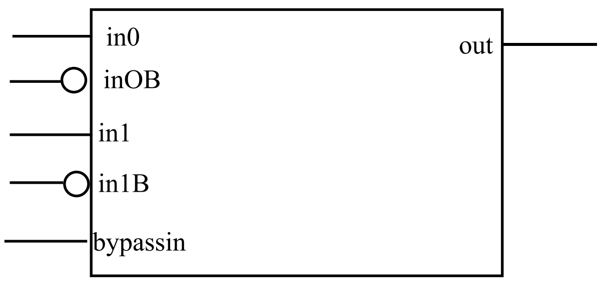

Fig 3.15 Token and Data Inputs circuit

Table 3.20 Token and Data Input Signal Definitions

Signal Name	Active State/Edge	Function
in0		1st Data/Token Input
in0B		Complement of above
in1		2nd Data/Token Input
in1B		Complement of above
bypassin		When High in1 is selected else in0
out		Token /Data Output

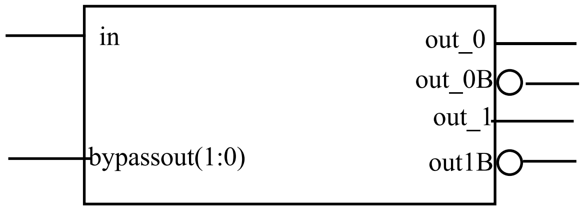

Fig 3.16 Token and Data Outputs circuit

Table 3.21 Token and Data Output Signal Definitions

Signal Name	Active State/Edge	Function
in		Token/Data in
bypassout(		When High out1 is enabled else out0
out0		1st Data/Token Output
out0B		Complement of above
out1		2nd Data/Token Output
outB		Complement of above

3.2.16 Test Circuitry

To simplify the testing of the chip during production and module assembly, it is proposed that additional test pads be included on the chip to enable selected parts of the chip to be tested easily

3.2.17 Readout Protocols

Output data from the ABC can be grouped into one of four classes.:

1) Physics Data

This is the compressed hit data from the detector. The format of this data is as follows:

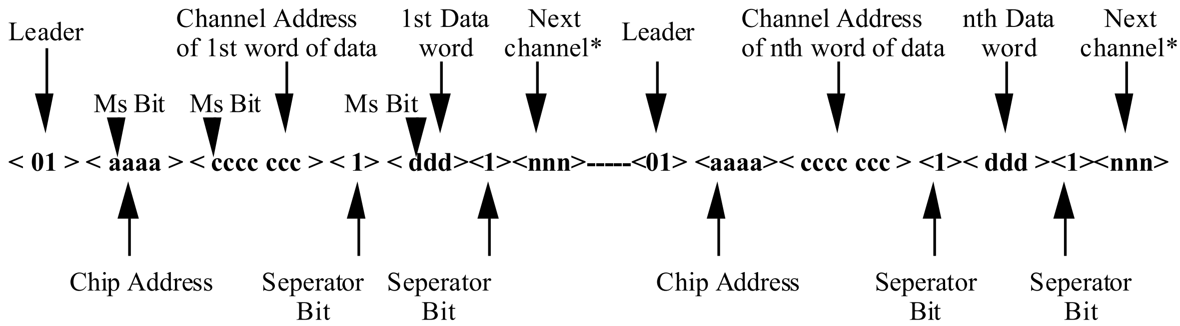

Fig 3.17 Readout Data Format

where

aaaa	LS 4 bits of the chips geographical address
ccc,cccc	7-bit address of the channel on which the hit or 1st channel in a groups of hits was found
ddd	Is the 3 bit hit pattern read out from the hit channel.
nnn*	Is the 3-bit hit pattern read out from the next channel.

*N.B. This field is only sent if a hit is found on the channel which is next to the one which has previously been read out.
This field will be sent n-1 times for all the channels is a contiguous groups of n channels that have been hit.
e.g. If all the channel on the chip have been hit, then the address of the 1st channel would be output followed by the data from that channel. This would then we followed by a string of 127 values from the other channels.
If the next channel is not next to the previous channel , then the leader, chip address and channel address of this hit must be sent before the data can be sent.

2) No Hit Data

If a chip has received the event currently being read out but has not found any hit channels, it outputs a No Hit Data Packet.

Leader

< 00 ><1>

Fig n No Hit Data Packet

3) Configuration Data

Configuration data is sent by the chip in response to a L1 trigger when the chip is in its Send_ID mode of operation, i.e. the chip is not sending data. A packet of data is sent from the chip which contains the chips address and the contents of the chips configuration register.

Leader Control code MS Byte of Config Reg LS Byte of Config Reg

Ms Bit

< 00 ><1> < aaaa > < 111> < 1><cccc,cccc><1><cccc,cccc><1>

Chip Address Seperator Bit Ms Bit Seperator Bit Ms Bit Seperator Bit

4) Error Data

.
Error data is only sent if the chip detects an error e.g. Buffer overflow,. In this cases a data packet of the following format is sent :

Leader Error code

Ms Bit

< 00 ><0> < aaaa > < eee> < 1>

Chip Address Seperator Bit

Fig 3.18 Error Data Format

Error Codes:

At present only 3 codes have been defined :

eee = 001	No Data Available
eee = 010	Buffer Full
eee = 100	Buffer Overflow (Soft Reset needed)

N.B. Error messages are only sent if the chip is Data_Taking Mode. (see section 3.2.19)

4) Module Data

This type of data packet is only output from chips which have been configured as masters. The packet consists of 2 elements, a 13-bit header generated by the Master ABC chip and string of physics data packets, from the other ABC chips daisy-chained to the Master ABC chip.

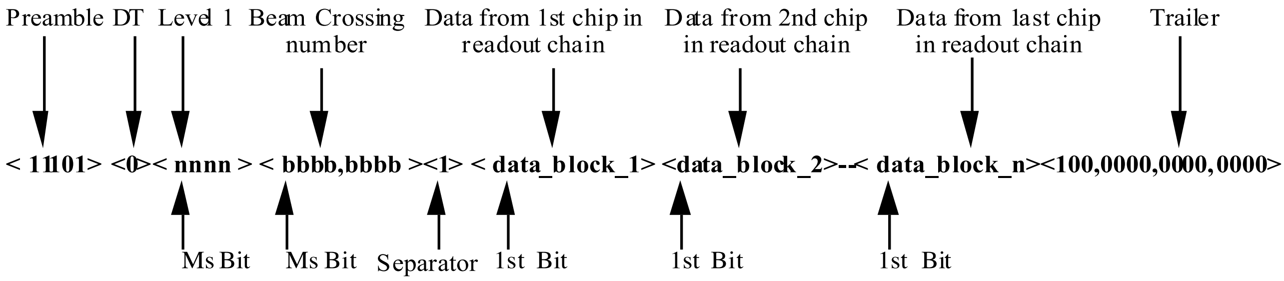

Fig 3.18a Module Data Format

DT(Data Type
The value of this bit determines the type of data which follows. This can either be Level 1 Trigger Data (DT=0) or Information Data (DT=1). In the case of the ABC chip only Level 1 trigger Data is Sent and hence this field is always set to '0'.

Level 1
Current count of Level1 Trigger modulo 16 since the last system reset. This field can be used for event building by the DAQ and also to monitor for lost data.

Beam Crossing Number
Current count of Beam Crossing modulo 256 since the last system reset. This field is not really to tag Beam Crossing numbers since it wraps around so quickly. It is intended to monitor for clock pulses lost by the on-detector electronics.

3.2.18 Control Protocol

There are 3 groups of control commands; Level One Triggers, Fast Commands and Control Commands that can be issued during data taking

Table 3.22 Control Commands

Type	Field 1	Field 2	Field 3	Description
Level 1	110	---	---	Level one Trigger
Fast	101	0101 or 0010		Soft Resets BC Reset
Slow	101	0100	Command	Control Command see table 3.23

3.2.18.1 Level One trigger

This is the most frequently issued packet and hence the smallest. All ABC chips that receive this packet act on it. There is no addressing. If this command is received 3 samples are readout out of the pipeline and written into the readout buffer.

Fast Command
This type of command is sent when a command has to be issued to the chip more quickly than can be achieved by sending a slow command to the chip. In the case of the ABC chip only two commands of this type has been defined i.e. the soft reset , and BC reset commands. It is expected that these commands will be sent to the chip at regular intervals, during periods of time when no Level 1 triggers will be sent to the chip. The purpose of these commands is perform a limited reset of the chip. (see section 3.2.19 for details)

3.2.18.2 Control commands

These are long packets that enable the operation of the chip to be controlled. While they are being sent it is not possible to send a first level trigger. Only the addressed ABCs will act on the packet, unless the address sent equals '111111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed ABCs erroneously decoding parts of the data field as the start of packets. To ensure that the chip does not respond to erroneous commands the chip will be placed out of taking mode for any command it receives which effects the configuration of the chip. i.e. all commands in which the 1st bit of field 5 is '0'. Hence it will be necessary to issues a command to the chip to Enable data taking after issuing a command to change its configuration. When the chip is not in data taking mode it will send its ID. This is the power on default state.

Table 3.23 Control Commands

Field 3	Field 4	Field 5	Field 6	Description
0001,1100	aaaaaa	000 000	dddd,dddd,dddd,dddd	Write to Configuration Register
1000,1100	aaaaaa	001 000	d---,----,----,---d	Write to Mask Register
0001,1100	aaaaaa	010 000	dddd,dddd,dddd,dddd	Write to Strobe Delay Register
0001,1100	aaaaaa	011 000	dddd,dddd,dddd,dddd	Write to Threshold Registers
0000,1100	aaaaaa	100 000	-------------------	Pulse Input_Reg
0000,1100	aaaaaa	101 000	-------------------	Enable Data taking Mode
0000,1100	aaaaaa	110 000	-------------------	Issue Calibration Pulse
0000,1100	aaaaaa	111 000	-------------------	Reserved

N.B
xxx = don't care state.
aaaaaa = 6 bit chip address(MS bit first)
dddd = data value for register (MS bit first)

Field 3
This is an 8 bit count of the number of bits in the following instruction.

Field 4
This is the 6-bit address of the chip for which the command is intended (see Section on Geographical Address)

Field 5
This 6 bit field is used to determine into which register on the chip the data contained in the following field will be written.

Field 6
This field holds the data that is to be written into the selected register. With the exception of instruction which load the mask register, this field will be 16-bits long.

Field 7
This field contains a single bit which enables a parity check to be performed on the bits contained in fields 4, 5 and 6.

3.2..19 Chip Initialisation and Configuration

3.2.19.1 Operating Modes

The chip has 2 modes of operation, "Send_ID mode and "Data_Taking Mode". After a Power-up reset the chip is placed into Send_ID mode.

Send_ID Mode

In this mode of operation the chip sends its ID and Configuration data in response to a L1 trigger. There is no command which explicitly places the chip in this mode of operation, however any attempt to alter the contents of the contents of the chips various registers automatically results in the chip being placed into Send_ID mode.

Data_Taking Mode.

When the chip is not in Send_ID mode it is in Data_Taking Mode and visa-versa. In this mode of operation the chip sends out any physics data that it has The chip may be placed in this mode of operation by sending a command to the chip to enable data taking. The chip may be taken out of this mode of operation and placed into Send_ID mode by either a Power_up reset or any attempt to change the contents of the chips registers. In addition, if parity checking is enabled on the chip any command received by the chip which fails its parity check will also have the same effect.

Clock Feed Through

If the clock feed through bit in the configuration register has been cleared and the chip has been configured as a Master , the chip outputs the chips system clock divided down by 2 from it's data output pins. This feature has been included to simplify system testing.

3.2.19.2 Resets

There are three kinds of reset in the system.

Power up reset

The power-up reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips command register to zero, it's default value, and clears all the buffers in the chip. Thus placing the chip into a well defined state. This type of reset is issued automatically when power is first applied to the chip. Provision will be made to enable this signal to be supplied externally to the chip.

Soft Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset will be issued to the chip periodically during data taking to eliminate synchronisation errors.

1) Upon receipt of the reset command, the ABC chip resets all internal counters, clears tokens and sets itself to the no-data state. If it was transmitting data, it terminates this immediately.

2) The external system must wait a time consistent with any data in the serial ring at the reset clock cycle to flush round the ring. This is one clock cycle per chip in the read-out ring, or 0.3μs for a 12 chip ring.

N.B. It should be noted that the off-detector system must then be able to determine the last complete event transmitted before the reset and discard it (Complete in the sense that all read-out rings supply a header and trailer). With either reset it must also be able to recognise and discard partial events since there is no guarantee that different read-out rings will be reading the same event when the periodic reset arrives. This section will define how the chip behaves on power up, i.e. default state of registers etc. latch-up prevention measures needed , and any special power cycling or power ramping required.

BC Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to zero the Beam Crossing counter. It has no effect the operation of any other part of the chip.

3.2.19.3 Data Readout and Redundancy

The figure below shows the data and token interconnections on a typical silicon detector module. The module has 6-ABC chips on each side. The LED outputs of 2 of these chips are connected to an fibre-optic interface and are configured to act as Masters in controlling the readout of data from each side of the module. On the diagrams the Master chips are denoted by a “M” and all the other chips are configured to act as slaves as denoted by a “S” or "E' on the diagram.

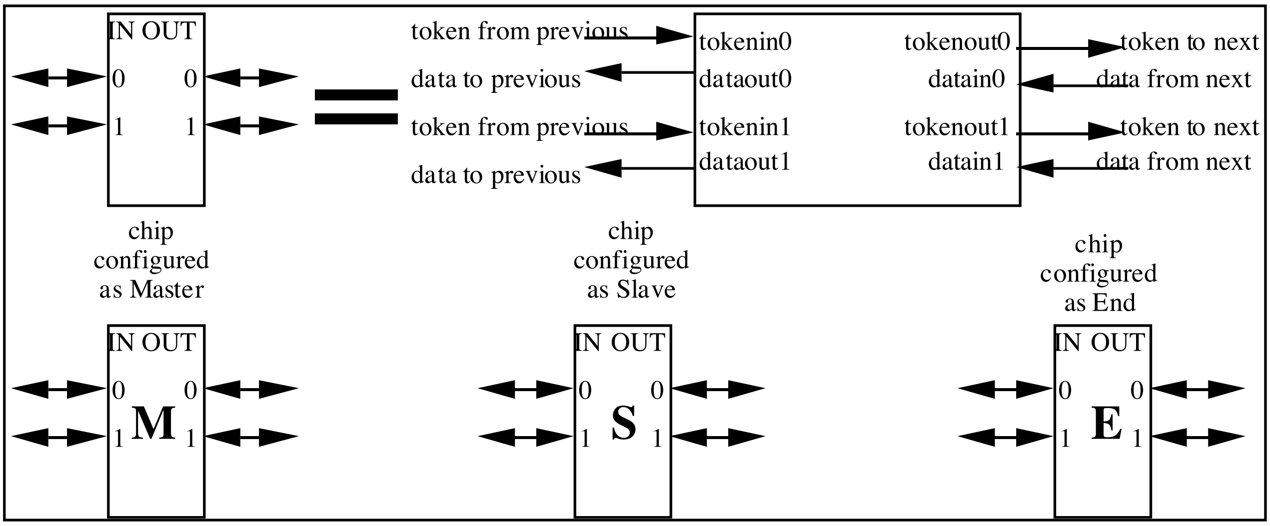

Fig. 1 Key to symbols used in following Diagrams

After the receipt of a Level 1 Trigger the Master chip initiates a readout cycle by sending the pre-amble bits at the start of each data block to the LED driver. A few clock cycles before the last bit of the pre-amble has been sent it sends a token to the slave chip on it's right. The slave chip on the right responds by sending its data packet to the Master which in turn it appends it to the pre-amble and sends it to the LED driver.

N.B. each chip always sends at least 3 bits of data even if it hasn't found any hit channels in the event being read out.

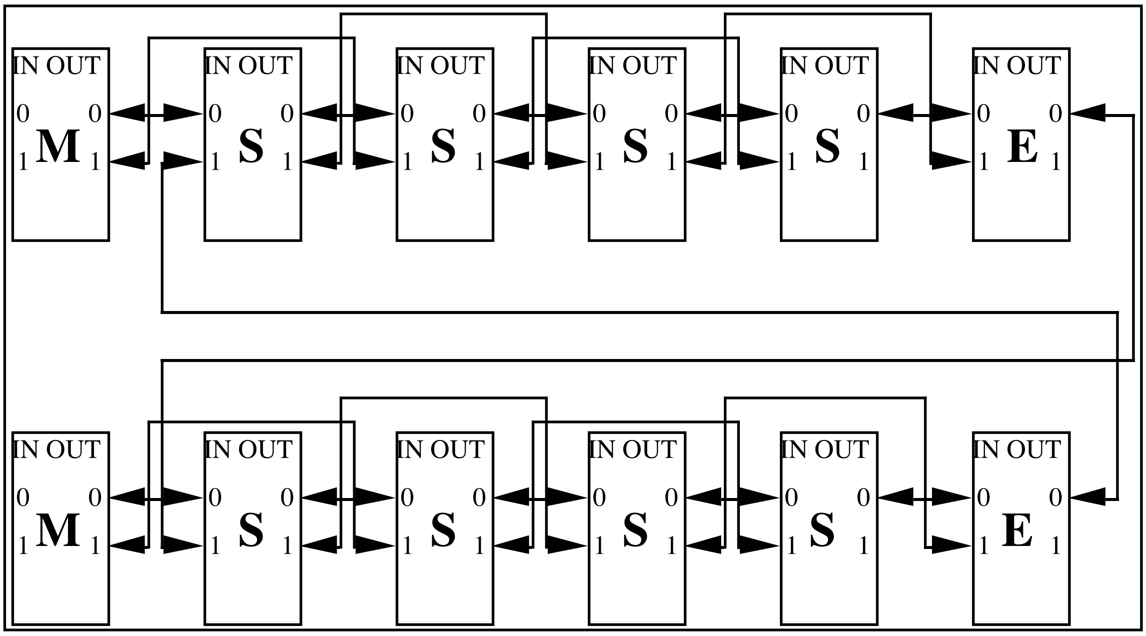

Fig 2 Diagram Showing the Interconnection of ABC chips on a Silicon Detector Module.

Once this slave chip has finished sending it's data it also passes on the token to the next chip on the right. The next chip on the right passes its data onto the previous chip on the left which in turn passes it back to the Master chip for transmission to the LED driver. This process continues until the last chip in the chain has sent it's data.

A bit is set in the last chip in the chain to inform it that it is the last chip (these chips are shown as 'E' on the diagrams). When this chip has sent it's data it appends a trailer to the end of the data stream. While the Master chip is outputting data it is constantly looking for the trailer pattern which has been carefully chosen to be distinct from the data. Once it finds the trailer patter it knows that all the data from the event has been sent and can start processing the next event.

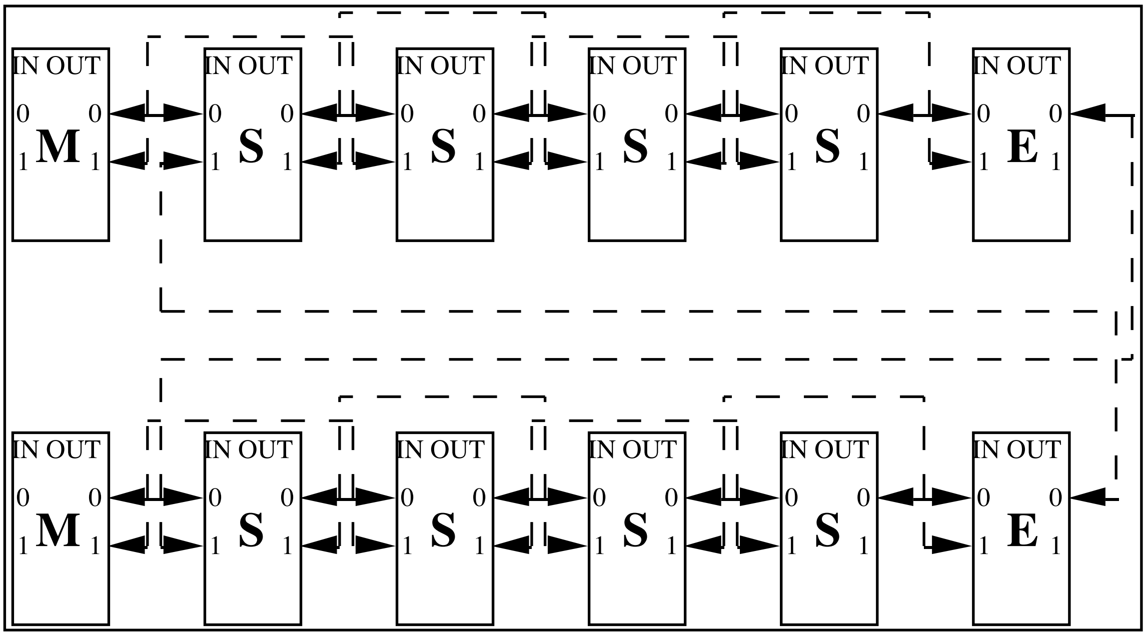

Fig 3 Diagram Showing the normal flow of Data and Tokens between chips. (Active links are Highlighted)

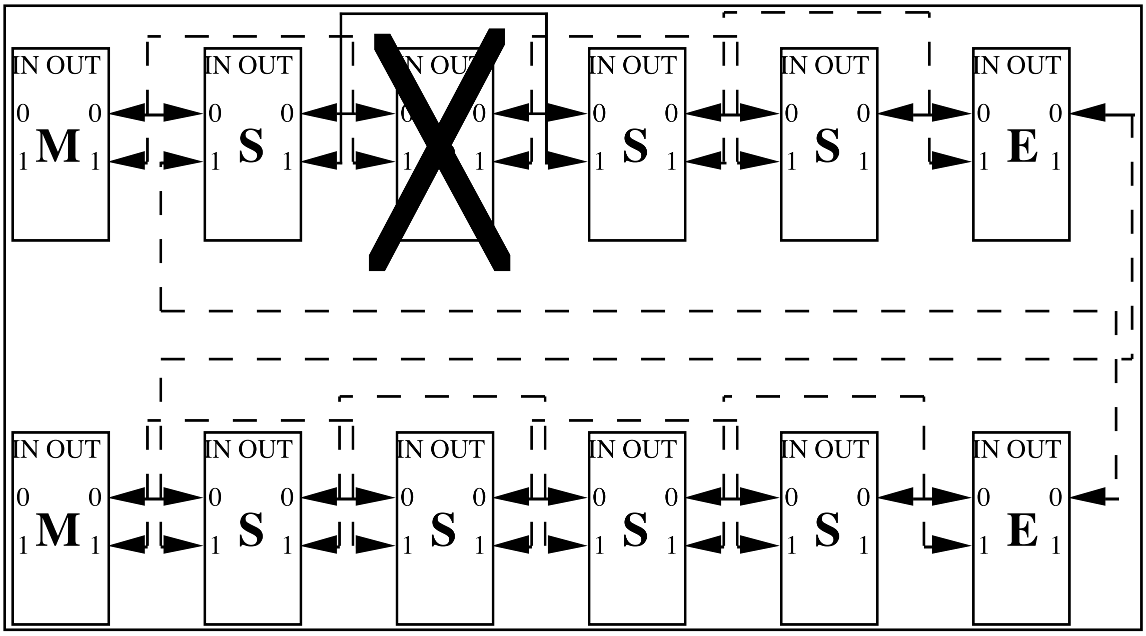

Fig 4 Diagram Showing the flow of Tokens and Data in the event of the failure of a Slave ABC chip

In the event of the failure of one of the Slave chips the previous and next slave chips in the chain are programmed to route their data and tokens around the failed chip. If the last chip in the chain should fail, then the penultimate chip in the chain is programmed to perform the operation of the "End chip".

In the event of the failure of a Master chip in the chain, the data and tokens from the chain with the failed Master chip are routed to the working master chip as shown in the next diagram .

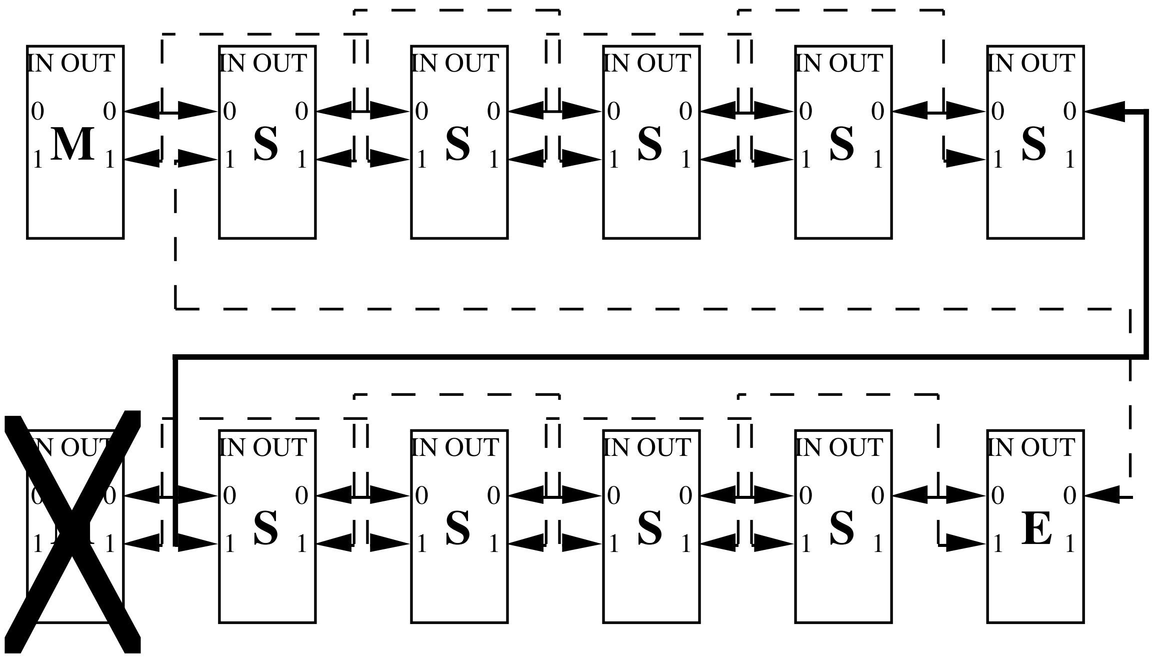

Fig 5 Diagram Showing the flow of Tokens and Data in the Event of the failure of a Master ABC chip

3.2.20 Default Register Values

On power up the contents of the configuration register will be set to zero. This results in the following configuration.

Read Out Mode is set to Detector alignment mode
Calibration Mode is disabled
Send_ID mode is enabled.
tokin0 and din0 inputs are enabled
tokout0 and doutO outputs are enabled.
Input test mode is disabled.
Edge Detection Mode disabled
Clock Feed Through Mode is Enabled if the chip is acting as a Master.
Chip will not be configured as the end of a readout chain.
The chip will be configured as a Master if masterB is asserted else it will be configured as a slave.

3.2.20.1 Master/Slave Selection

The default state of the chip on power up is determined by the state on the masterB input pin. If this pin has been left unconnected or tied high the chip will power-up as a Slave. If this pin has been tied to ground the chip will power up as a Master. The masterB signal is "x-ored" with bit 11 of the configuration register and the resulting signal determines the operational state of the chip. This enables the power-up state of the chip to be pre-determined and also enables the mode of operation of the chip to be changed via a Slow Control Command if required.

3.2.21 Input/Output Connections

The following diagram shows all the external connections to the chip. These connections are listed and described in the following tables.

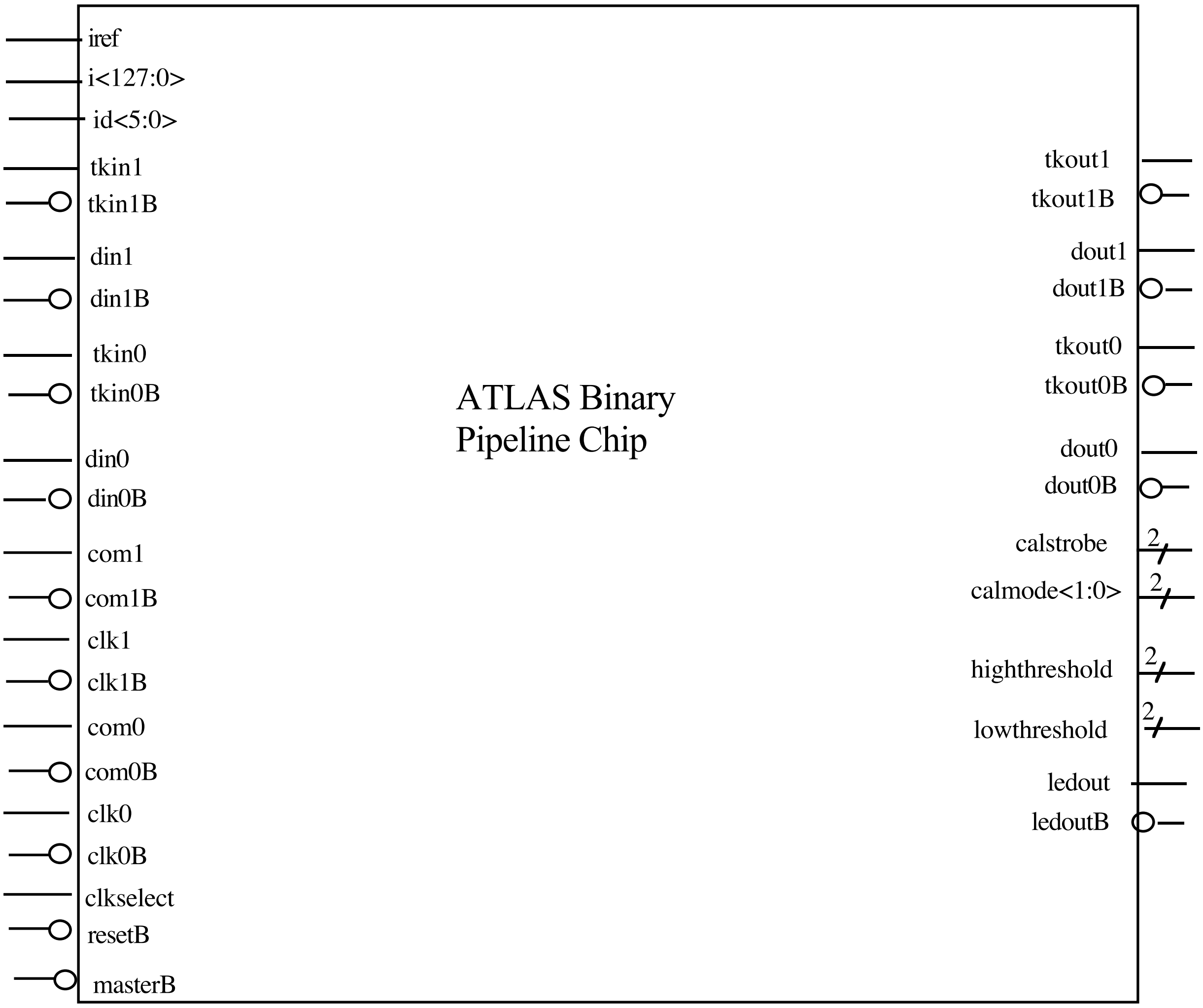

Fig 3.19 External Connections to the Chip

Table 3.24 Input Signals

Name	**Function**	**Type**
in<0:127>	Signal Inputs	Current Mode
clk0 & clk1	Clock input	LVDS
clk0B & clk1B	Complement of above signal	LVDS
com0 & com1	Command Input	LVDS
com0B & com1B	Complement of above signal	LVDS
tokin0 & tokin1	Token Input	Current Mode
tokin0B & tokin1B	Complement of above signal	Current Mode
din0 & din1	Data Input	Current Mode
din0B & din1B	Complement of above signal	Current Mode
id<5:0>	Geographical address of chip	CMOS
masterB	Sets chip default to master	CMOS
clksel	Selects clock/command inputs	CMOS
resetB	Resets Chip	CMOS

Table 3.25 Output Signals

Name	Function	Type
tkout0 tkout1	Token Output	Current Mode
tkout0B tkout1B	Complement of above	Current Mode
dout0 dout1	Data Output	Current Mode
dout0B dout1B	Complement of above	Current Mode
ledout	Data Output to LED driver	LVDS
ledoutB	Complement of above	LVDS
calmode<0:1>	Calibration Mode Output to pre-amp chip.	CMOS
calstrobe	Calibration Strobe Output to pre-amp chip	Current Mode
highthreshold	High threshold output to CAFE chip	Analogue
lowthreshold	Low Threshold output to CAFE chip	Analogue

3.2.22 Electrical Specifications

3.2.22.1 Supply Voltage

4.0 volts ± 5%.
The ramp up times and ramp down requirements of the power supply will be specified as soon as known.

3.2.22.2 Power Consumption

Less than or equal to 64mW when operating at a 1% occupancy and 100Khz Level 1 trigger rate.

3.2.22.3 Input /Output Levels

Table 3.21 Input Levels for Hit Inputs.

Parameter	Minimum	Typical	Maximum
Low Level Input Current I_{IL}	4µ	6µ	9µ
High Level Input Current I_{IH}	128µ	160µ	192µ

Table 3.22 Output Levels for Calibration Code Outputs

Parameter	Minimum	Typical	Maximum
Low Level Input Voltage V_{OL}		30µ	
High Level Input Voltage V_{OH}		60µ	

Table 3.23 Output Levels for Calibration Strobe Output

Parameter	Minimum	Typical	Maximum
Low Level Input Current I_{OL}		30µ	
High Level Input Current I_{OH}		60µ	

Table 3.24 Input Levels for Voltage Mode Inputs (Clock, Control)

Parameter	Conditions	Minimum	Maximum	Units
Input Voltage Range V_i	$V_{gpd} \leq 950mV$	0	2400	mV
InputVoltage Common mode V_{icm}	$V_{gpd} \leq 950mV$	50	2350	mV
Differential high input threshold $+V_{idth}$	$V_{gpd} \leq 950mV$		100	mV
Differential high input threshold $-V_{idth}$	R_{load} =100Ω±1%	-100		mV
Threshold hysteresis	(+Vid) - (Vid)	**25**		mV
Receiver input impedance		90	110	Ω

Table 3.26 Input Levels for Current Mode Inputs (Token_in, Data_in)

Parameter	Minimum	Typical	Maximum
Low Level Input Current I_{IL}			
High Level Input Current I_{IH}			

Table 3.27 Output Levels for Current Mode Outputs (Token_Out, Data_out)

Parameter	Minimum	Typical	Maximum	Conditions
Low Level Output Current I_{OL}		15µ		C_L=40pf
High Level Output Current I_{OH}		30µ		C_L=40pf

Table 3.27a Output Levels for LED Outputs

Parameter	Conditions	Minimum	Maximum	Units
Output Voltage low V_{IL}	R_{load} =100Ω±1%	1000		mV
Output Voltage High V_{IH}	R_{load} =100Ω±1%		1400	mV
Output offset Voltage	R_{load} =100Ω±1%	1125	1275	mV
Output Differential Voltage	R_{load} =100Ω±1%	250	400	mV
Output impedance	I_{load} =2mA to 3mA	40	280	Ω

a timing diagram for inputs and outputs will be included here when available. together with a set of timing parameters

an example of a test circuit will be included for these inputs and outputs when available

3.2.24Timing Requirements

3.2.24.1 Clock and Command Input Timing

to be specified

Fig 3.20 Clock & Command Timing

Table 3.28 Clock and Command Timing Parameters

Symbol	Parameter	Min	Typical	Max.	Condition
					CL=xxpf
					CL=xxpf
					CL=xxpf
					Cl=xxpf

3.2.24.2 Readout Timing

he timing for the readout circuitry is shown in Fig 3.10

Fig 3.21 Readout Timing

Table 3.29 Readout Timing Parameters

Symbol	Parameter	Min	Typical	Max.	Condition
	Token In set-up time				
	Token In Hold Time				
	Data In set-up time				
	Data In hold time				
	Clock High to Token out High				CL=xxpf
	Clock High to Token Out Low				CL=xxpf
	Token High to Data Out Valid				CL=xxpf
	Token Low to Data out invalid				Cl=xxpf

3.2.24.3 Input Signal Timing

To be defined

Fig 3.22 Input Signal Timing

Table 3.30 Input Signal Timing Parameters

Symbol	Parameter	Min	Typical	Max.	Condition
					CL=xxpf
					CL=xxpf
					CL=xxpf
					Cl=xxpf

3.2.24.4 Calibration Timing

To be defined

Fig 3.23 Calibration Signal Timing

Table 3.31 Calibration Timing Parameters

Symbol	Parameter	Min	Typical	Max.	Condition
					CL=xxpf
					CL=xxpf
					CL=xxpf
					Cl=xxpf

the following parameters will be specified

Voltage level of 2 bit patter outputs (the 2 CMOS levels)
Current levels of the strobe
rise time of strobe (mas strobe duration i=16 clocks

3.2.25 Physical Requirements

The die size will be 6.2mm x less than 5mm. Assuming a 0.8µm 3-metal process.

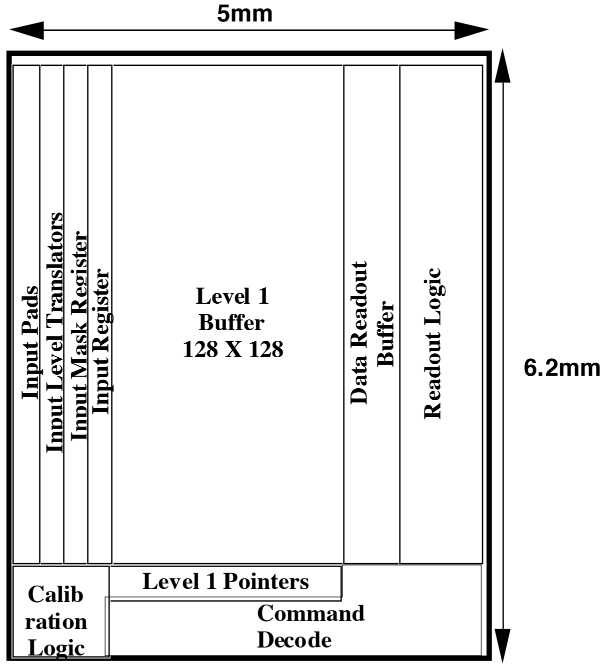

Figure 3.24 Chip Layout (not to scale)

The input pads to the chip must be arranged on a pitch so as to enable the Binary Readout Chip to be wire bonded to the CAFE chip. The input pads on the CAFE chip are arranged as 2 rows of 64 pads. Each pad has an area 130µ x 60µ and the pads have been laid out on a pitch of 44.0µ.

3.2.25.1 Bond Pad Arrangement

The arrangement of the bond pads will be defined in conjunction with the people involved in the design of the Detector Modules All service pads should be large enough to allow double bonds if possible.

a diagram of the chips bond pads will be inserted here when defined

Table 3.32 Bond Pad Connections

Pad No	Connection	Pad No	Connection
1-128	IN<0-127>		TOK_IN
129	CAL_MODE<0>		TOK_OUT
	CAL_MODE<1>		DATA_IN
	CAL_STROBE		DATA_OUT
	CLK		BIAS
	CLK		VSS
	COM		VSS
	COM_B		VSS
	ID<0>		VSS
	ID<1>		VDD
	ID<2>		VDD
	ID<3>		VDD
	ID<4>		VDD

3.3.26 Manufacturing

Initial manufacture of the chip will be subcontracted to Honeywell, who will fabricate the chip on their 0.8µ RICMOS IV radiation hardened bulk CMOS process. After initial development of the chip other suitable vendors will be evaluated.

3.4 Testing and product control

A plan for the testing of these devices will be drawn up as soon as it is known who will be involved. This plan will be produced no later than the intermediate design review to ensure that the chip is testable.

3.5 Installation

Not applicable.

3.6 Maintenance and further orders

To be determined at the concluding review stage.