Project Specification
Project Name: CAFE-M
Version: V2.02

1. Scope:

Establish the requirements and the target design specifications for the Front-end Bipolar Amplifier/Discriminator Integrated Circuit to be used as part of the Binary Readout of the ATLAS Semi-Conductor Tracker (SCT). This design is based upon previous work, in particular TekZ IC used in the DESY ZEUS experiment, the FABRIC IC used in the CERN NA50 experiment and the LBIC and CAFE prototype ICs.

2. Reference Documents:

1) Specification for the Atlas Binary Chip (ABC), 1996.
2) I. Kipnis, "CAFE: A complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT", 1995.
3) E. Spencer, et al., "A Fast Shaping Low Power Amplifier-Comparator Integrated for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1994, (SCIPP 94/32)
4) W. Dabrowski, et al., "Fast Bipolar Front-end for Binary Readout of Silicon Strip Detectors", Nuclear Instruments and Methods A 350 (1994), 548
5) I. Kipnis, et al., "An Analog Front-end Bipolar-transistor Integrated Circuit for the SDC Silicon Tracker," IEEE Transactions on Nuclear Science, vol. 41, no. 4, (1994), 1095-1103.
6) E. Barberis, et al., "A Fast Shaping Amplifier-Comparator Integrated Circuit for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1992, (SCIPP 92/40)
7) "Silicon Tracker Conceptual Design Report", SCIPP 92/04.
8) H. Spieler, "Electronics Baseline Specification - Recap and Postscript", Minutes of SDC Silicon Tracker Meeting at LBL, 16-Dec-92.
9) J. Leslie, A. Seiden, Y. Unno, "Signal Simulations for Double-sided Silicon Strip Detectors", SCIPP 92/20.
10) H. Spieler, "Rate of Noise Hits in Threshold Discriminator Systems", unpublished note.
11) H. Spieler, "Some Comments on Specifications for Front-End Electronics in the SDC Silicon Tracker", unpublished note.

3. Technical Aspects:

3.1 Requirements

3.1.1 An Integrated Circuit (IC) to process signals from 128 n-type strips of a Silicon Micro-strip Detector. An outline schematic of the IC is shown in Figure 1.

3.1.2 Signal Processing (See block diagram in Figure 2):

The IC must contain the following functions:

Charge integration
Pulse shaping
Threshold/timing discrimination

The result of the discrimination function, indicating a "hit" or "no hit" for each strip, is output from this IC to another circuit for further digital processing. This IC will have one independent channel to process signals from each silicon strip of the detector. Signals from each detector strip will be received at single-ended Sensor

Input pads IN0..INn and results appear at single-ended Output pads OUT0..OUTn. Two reference current outputs OUTRH and OUTRL are provided as well as a ground return DRET for the output current.

A control input (VI1) is provided to set the operating current of the input transistor.

The threshold value is provided either as a differential voltage from an external source (VTHP, VTHN) or as a programmable current from the adjoining digital processing IC (ITH) as selected by the pad VTSEL. See 3.2.3.7 for more details.

3.1.3 Compatibility:

The design of this IC and that of the digital processing IC, ABC, must be compatible so that they can work together as a chip set. This compatibility of design includes the interface circuits (128 data signals with references, the calibration and threshold controls and the DAC reference) and the corresponding bonding pad locations.

3.1.4 Calibration Circuitry (See block diagram in Figure 3):

Each channel will have an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors will be charged by a chopper circuit which is triggered by an independent differential input Calibration Strobe (CALSP, CALSN). Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). These strobe and selection signals are expected to originate in the accompanying digital processing IC which is acting on commands from the experiments control system. The voltage applied to the Calibration Capacitors by the chopper is determined by a single differential DC Calibration Level input voltage (CALVP, CALVN) or as a single programmable current from the adjoining digital processing IC (CALI). See 3.2.3.9 for more details. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads on each side of the IC (CBUS0, CBUS1, CBUS2, CBUS3) which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing.

3.1.5 DAC Reference Circuit (See block diagram in Figure 4):

The adjoining digital processing IC will contain digital-to-analogue converters (DACs) to supply programming currents for the Comparator Threshold and the Calibration Level. It is assumed that these DACs will scale down a reference current supplied by this bipolar IC according to values programmed via commands from off-detector. One reference current will be generated via a band-gap reference circuit. The derived reference current and the voltages derived from the returned currents programmed by the DACs will depend upon resistors on this bipolar chip in order to maintain process independent scaling.

3.2. Specification of Deliverables:

3.2.1 Physical Requirements:

Number of amp/comparator channels per IC: 128

Physical Layout: See Figure 5.

Pad Layout:

Sensor Inputs on front edge.
Comparator Outputs on back edge
Service (power, ground, references) on side edge (reflected on both sides)
Threshold Inputs on back edge (current mode, including reference current)
and also on side edge (differential voltage mode, reflected on both sides)
Calibration Strobe & Address Inputs on back edge near corners
Calibration Amplitude Inputs on back edge (current mode)
and also on side edge (differential voltage mode, reflected on both sides)
Output logic high and low reference current on back edge

Sensor Input Pad Pitch: = 48 μm, 2 rows @ 96 μm pitch each offset at 48 μm to each other

Output Pad Pitch: = 44 μm, 2 rows @ 88 μm pitch each offset at 44 μm
Note that an alternative output pad arrangement is under consideration in order to allow the ABC chip to be kept to its minimum width. This arrangement would use 3 rows of pads @ roughly 96 μm pitch each.

Pad Size (nominal):

Sensor Inputs:	140 x 60 μm
Outputs:	140 x 60 μm
Service: (VCC, GND)	190 x 92 μm
(Other Service on side edge)	92 x 92 μm
Service on front and back edge:	140 x 60 μm

Total Chip Width: $\geq$ 6.4 mm, $\leq$ 6.6 mm after sawing and including all bond pads.

Total Chip Length: $\geq$ 3.8 mm, $\leq$ 4.5 after sawing and including all bond pads. (Minimize total area to improve cost.)

Channels must be laid out in parallel to meet electrical requirements.

Services like power, ground and voltage references must be bussed across chip with pads on both sides to allow bonding on either side. The SSGND pads must be bonded on both sides of the IC to equalize voltage drop across the IC. It would ease the IC layout if the services were required to be bonded on both sides rather than on either side. This should be studied further with the hybrid designers.

Critical service pads (e.g. VCC, GND) are made double width to allow double wire bond for improved reliability.

3.2.2 Assumed Detector Electrical Characteristics at Input to this IC from n-type 12 cm long strips:

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbor strips	1.22 pF/cm	0.92 pF/cm
Capacitance of strip to backplane	0.28 pF/cm	0.28 pF/cm
Metal strip resistance	20 Ω/cm	20 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise {estimated}	2.0 nA	2.0 μA

AC characteristics for the detector signal are shown in Figure 6 and Table 3 for an irradiated n-strip detector. For an unirradiated detector, the pulse shape will be slightly narrower.

3.2.3 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.2.3.1 Sensor Input Characteristics:

Input Signal Polarity: Negative signals from n strips.

Crosstalk: < 5% (with detector)

Input Protection: Must sustain voltage step of 300 V of either polarity with a cumulative charge of 5 nC in 15 ns.

Open Inputs: Any signal input can be open without affecting performance of other channels.

Max Parasitic Leakage Current: 100 nA DC per channel with < 10 % change in gain at 1 fC input charge.

3.2.3.2 Calibration Input Characteristics:

The digital signal processing IC, ABC, must provide the following inputs for the Calibration Circuit. See 3.2.3.9 for functional specifications of the Calibration Circuit.

Two single ended logic inputs CALD1, CALD0 to select one of four groups of channels to test.

	Min	Nominal	Max
"1" State Level	2.9 V	4 V	4.2 V
"0" State Level	0 V	0 V	0.5 V
Current			100 µA
Rise Time			10 ns
Duration		DC	

One pair of Calibration Strobe inputs CALSP, CALSN which form one signal to activate the Calibration circuitry. The CALSP input is normally in the "Off" state and the CALSN input is normally in the "On" state when the Calibration Strobe is idle. During an active Calibration Strobe, CALSP goes to the "On" state and CALSN goes to the "Off" state. It is expected that these inputs are driven by a complementary driver:

	Min	Nominal	Max
"On" State Current at 0.7 V Nom (each input)	- 180 µA	- 240 µA	- 300 µA
"Off" State Current	- 15 µA		- 30 µA
Voltage Range (either state)	0.7 V		1.0 V
Rise Time			2 ns
Duration	125 ns		
Delay after transition of CALD1,CALD0	250 ns		
Off interval between consecutive pulses	250 ns		

Calibration Level: See DC Supply and Control Characteristics

3.2.3.3 DC Supply and Control Characteristics:

The following DC inputs are required for 128 channels with voltage specifications listed on this page and current specifications on the following page. Differential pairs are grouped together.

		Operational Values			Absolute
	Pad Name	Min	Nominal	Max	Max
Circuit Supply	VCC	3.325 V	3.5 V	3.675 V	0 to 6 V
Preamp Current Control	VI1	0 V	1 V	2 V (off)	Vcc
Small Signal Ground	SSGND		0 V		
Circuit Ground	GND		0 V		
Digital Ground Return	DRET	-100 mV	0 V	100 mV	-500 mV
Comparator (voltage) Threshold	VTHP	2.4 V	2.5 V	2.6 V	VCC
	VTHN		2.4 V		VCC
(Vthp - Vthn)			0.19 V	0.9 V	0 to 2 V
Comparator (current) Threshold	ITH	VCC - 1.2 V			VCC
Threshold Select (for voltage mode)	VTSEL	VCC - 0.5 V		VCC	VCC
Calibration (voltage) Level (diff. pair)	CALVP	1.2 V		2.8 V	VCC
	CALVN	1.2 V		2.8 V	VCC
(CALVP - CALVN)		50 mV		1 V	2.0 V
(Equiv. Charge)		(.5 fC)		(10 fC)	
Calibration (current) Level	CALI	1.0 V		2.4 V	VCC
DAC Reference Current	IDAR	1.8 V			VCC

Special Requirements:

Gain Sensitivity to VCC for 1 fC signal		TBD
Power Supply Rejection Ratio at:	10 Hz - 100 Hz	TBD
	100 kHz - 300 kHz	TBD
	10 MHz - 60 MHz	TBD

The current draw at each DC input is as follows. Maximums assume -20 % resistor production skew.

		Min	Nominal	Max
Circuit Supply	VCC			
For I(Vi1)=150 µA			45 mA	51 mA
For I(Vi1)=300 µA			67 mA	73 mA
Preamp Current Control	VI1		.15 to .3 mA	.5 mA
Small Signal Ground	SSGND			
For I(Vi1)=150 µA			23 mA	23 mA
For I(Vi1)=300 µA			45 mA	45 mA
Circuit Ground	GND		22 mA	27 mA
Digital Ground Return	DRET		1 mA	
Comparator (voltage) Threshold	VTHP		12 µA	15 µA
	VTHN		12 µA	15 µA
Current Balance	|I of VTHP - I of VTHN|			
Comparator (current) Threshold	ITH	- 3 µA		- IDAR
Threshold Select	VTSEL		50 µA	60 µA
Calibration (voltage) Level	CALVP			1 µA
	CALVN			1 µA
Current Balance	|I of CALVP - I of CALVN|			10 %
Calibration (current) Level	CALI	+ 15 µA		IDAR
(Equiv. Charge)		(.5 fC)		(10 fC)
DAC Reference Current	IDAR		+ 324 µA	+ 363 µA

3.2.3.4 Signal Output Characteristics:

Assumed type of logic of receiving stage: edge triggered

Output configuration: open collector output of npn transistor as a current source.

	Min	Nominal	Max
"Off" State Current	0 μA		10 μA
"On" State Current	130 μA	200 μA	300 μA
Pulse Duration			
for 1.25 fC	8 ns		
for 3.50 fC			44 ns

Open Outputs: Any signal output can be open without affecting performance of other channels.

Output Reference pad named OUTRH: DC current equal to that of "On" state of normal outputs.

Output Reference pad named OUTRL: DC current equal to that of "Off" state of normal outputs.

3.2.3.5 Power Dissipation:

Power use will be minimized for this design.

Average Power: <= 1.8 mW for one bipolar channel, for VI1 at 300 μA and nominal fabrication processing parameters.

Total Average Power: <= 275 mW for VI1 at 300 μA and -20 % resistor production skew. {This is an over estimate which will be adjusted later.}

3.2.3.6 Noise:

Maximum rms. noise for nominal components including contributions from:
a) All detector parameters listed in 3.2.2
b) Two neighboring channels (one on each side): 3 channel simulation will be: <= 1400 electrons for unirradiated module
<= 1500 electrons for irradiated module

Noise analysis predicated on worst case n-strip signal (WNS) as shown from simulation of depleted detector n-strip signal in Figure 6 and Table 3 assuming the front-end ICs are wire bonded at the center of the 12 cm detector strips.

3.2.3.7 Comparator Stage:

A threshold is applied as a voltage offset to the comparator stage.

Threshold setting range: 0.5 fC to 5 fC, nominal 1 fC

This threshold voltage is applied externally either as a differential voltage or as a current. The unused inputs must be left floating. A pad VTSEL on the side of the chip must be bonded to VCC to use the voltage mode or left floating to use the current mode.

For voltage mode, typical externally applied differential threshold voltage to establish nominal threshold of 1 fC: ~ 190 mV (150 mV/fC + offset)

For current mode, a reference current (IDAR) is sunk as output expecting a programmable scaled current supplied as a threshold input (ITH). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Resulting step size near 1 fC threshold should correspond to ~0.025 fC of input charge. Typical externally supplied current to establish nominal threshold of 1 fC: ~ 60 µA.

Threshold variation at 1 fC:
4% (1 sigma) channel to channel matching within one chip
20% (1 sigma) including all process variations

3.2.3.8 Timing Requirements:

Timewalk: <= 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.

Timewalk defined: The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC according to 3.2.3.7.

Double Pulse Resolution: <= 50 ns for a 3.5 fC signal followed by a 3.5 fC signal, including a 6 ns off state of Output between pulses.

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 µs

3.2.3.9 Calibration Circuit Characteristics:

Calibration Capacitors: 100 fF +- 20% (3 sigma) over full production skew
+- 2% (3 sigma) within one chip

Absolute accuracy of voltage step applied to capacitors: 5% (full process skew)

Relative accuracy of voltage step: < 2 %
(for known values of calibration capacitors, amplitude range 0.8 to 4 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Relative accuracy of voltage step: < 10 %
(for known values of calibration capacitors, amplitude range 0.8 to 8 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Calibration circuit must be laid out such that Calibration Strobe signal pickup at comparator will be less than 0.3 fC equivalent sensor input.

The calibration amplitude is established externally either as a differential voltage or as a current. The unused inputs can be left floating or grounded

For voltage mode, typical externally applied differential voltage will correspond linearly to roughly 100 mV/fC of equivalent input charge up to 1 V

For current mode, the same reference current (IDAR) used for threshold control will be available expecting a programmable scaled current supplied as a calibration level input (CALI). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Typical externally supplied current will correspond linearly to roughly 30 µA/fC of equivalent input charge up to 300 µA. Linearity will be < 1 % in the range 0.5 fC to 2 fC and < 4 % in the range 2 fC to 10 fC.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CBUS0, CBUS1, CBUS2, CBUS3). Such an external voltage step must be AC coupled. When not used, these four pads must be left floating.

4. Quality Assurance:

4.1 Specification Review:

This specification and all revisions will be approved by the selected Review Committee for appropriateness to meet the goals of the detector and integratability with the rest of the subsystem.

4.2 Circuit Simulations:

The design will be simulated to test fulfillment of these requirements before submission to fabrication.

Transient analyses will be performed in which all DC supplies are cycled in random order to verify that no latch up occurs in the circuit.

Behavior will be simulated for variations in supply voltages 25 mV beyond that specified in section 3.2.3.3. Simulations will be done at temperatures of -10 and 25 degrees centigrade.

DC and AC analysis will be performed for 25% of the channels activated using actual metal busses and expected on-chip and off-chip bus impedances.

Sensitivity analysis will be done for all relative process parameters over 3 standard deviations of the expected fabrication distributions to the satisfaction of the review committee listed in 4.3. Circuit parameters will also be varied to simulate circuit

performance at initial commissioning and after irradiation of $10^{14}/cm^2$ particles including the respective sets of unirradiated and irradiated detector parameters given in section 3.2.2.

In the sensitivity analysis, < 1% of all channels may deviate from the specification.

4.3 Preliminary Design Review:

The design will be checked and simulations reviewed in detail by at least one engineer other than the circuit designer.

A Data Sheet specific to each prototype design must be submitted and include typical operating values, operating limits and absolute maximum values of supply voltages and currents.

The specific data sheet and simulation results will be reviewed by the Selected Review Committee of this specification before submission to fabrication.

4.4 Intermediate Design Review:

Results of prototype circuits including test data will be reviewed by the Review Committee to verify compliance with these requirements.

4.5 Final Design Review:

Before this circuit is submitted for Production Fabrication, a Final Design Review will be held by the Review Committee. The following data will be reviewed including comparisons between different vendors:

Electrical component tests

Electrical tests in assembled modules

Comparisons of tests vs. simulations

Expected yield and performance over process variations from each potential vendor

Reliability data

Irradiation effects

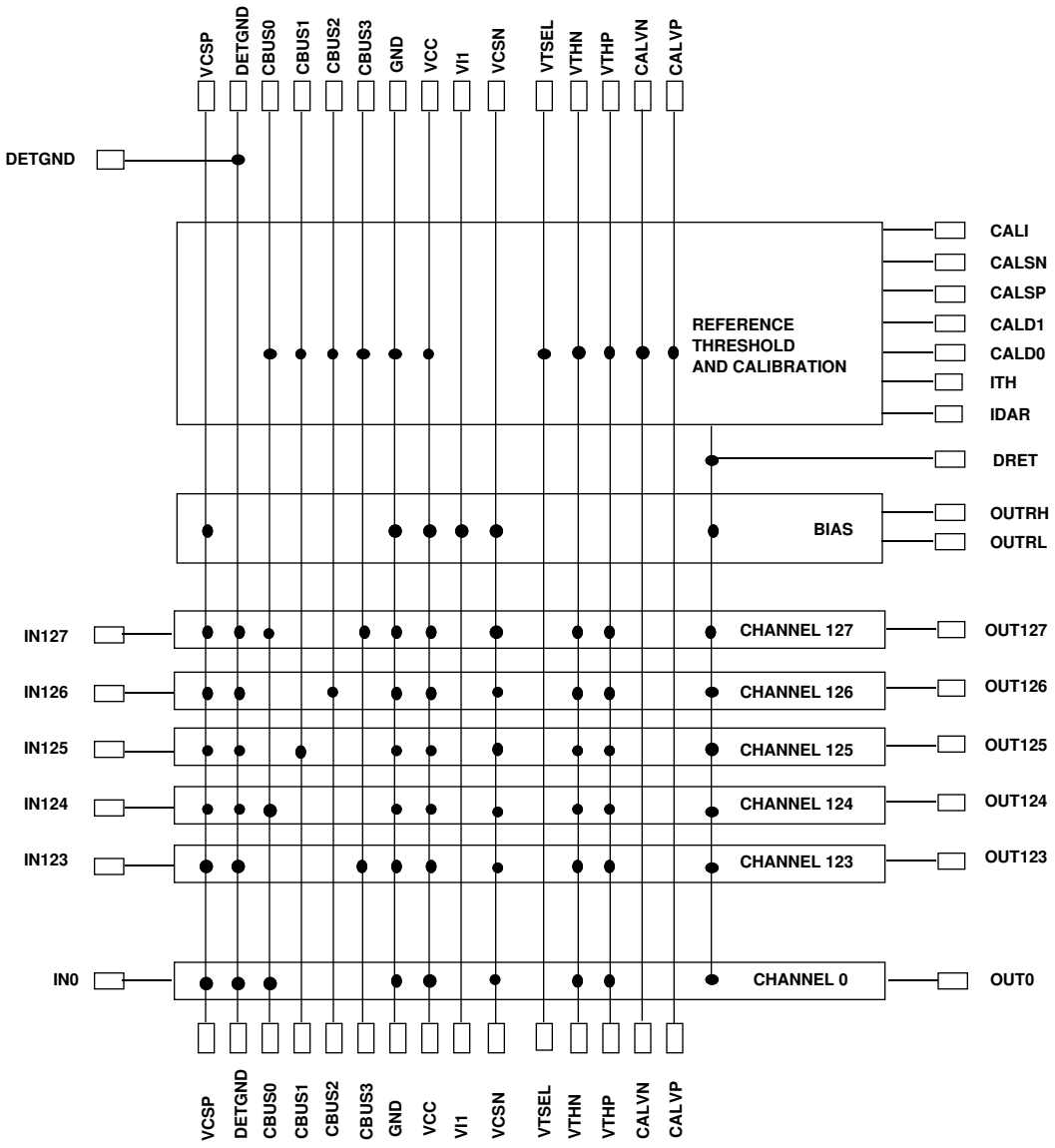

Figure 1: Chip Outline Schematic
Note: This figure shows relationships of input/output signals to circuit blocks and not relative pad positions of the chip layout.

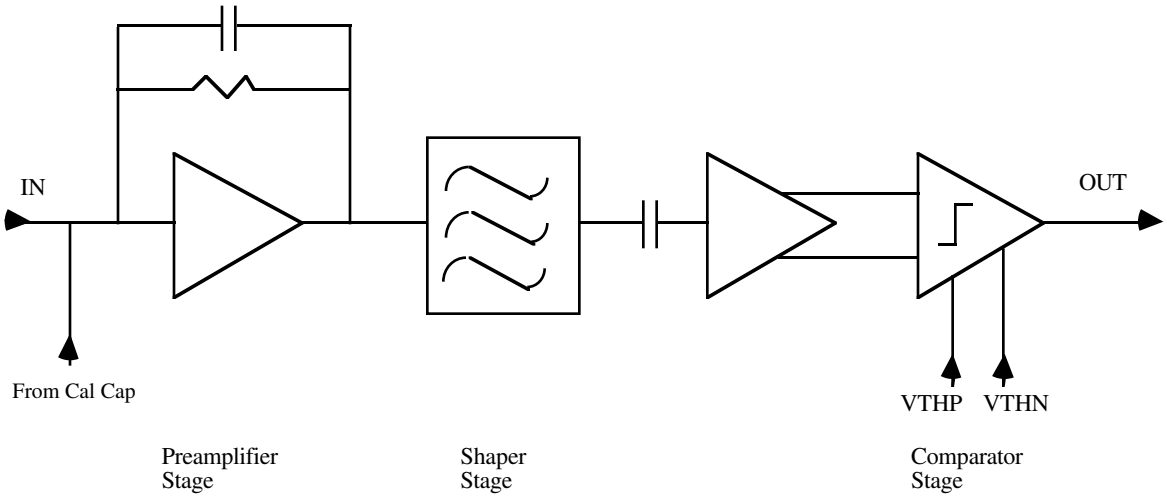

Figure 2: Block Diagram of One Signal Processing Channel

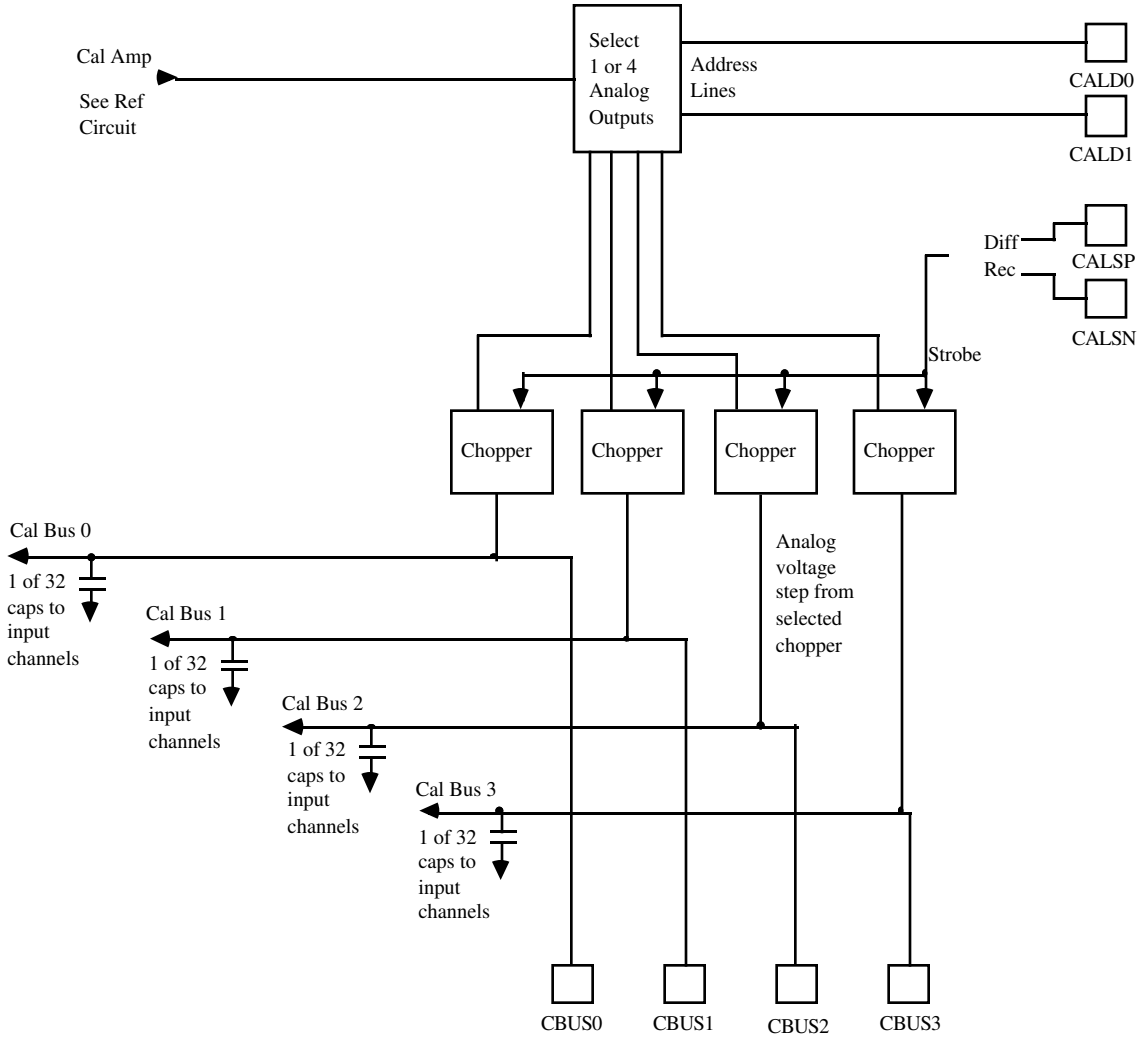

Figure 3: Block Diagram of Calibration Circuitry

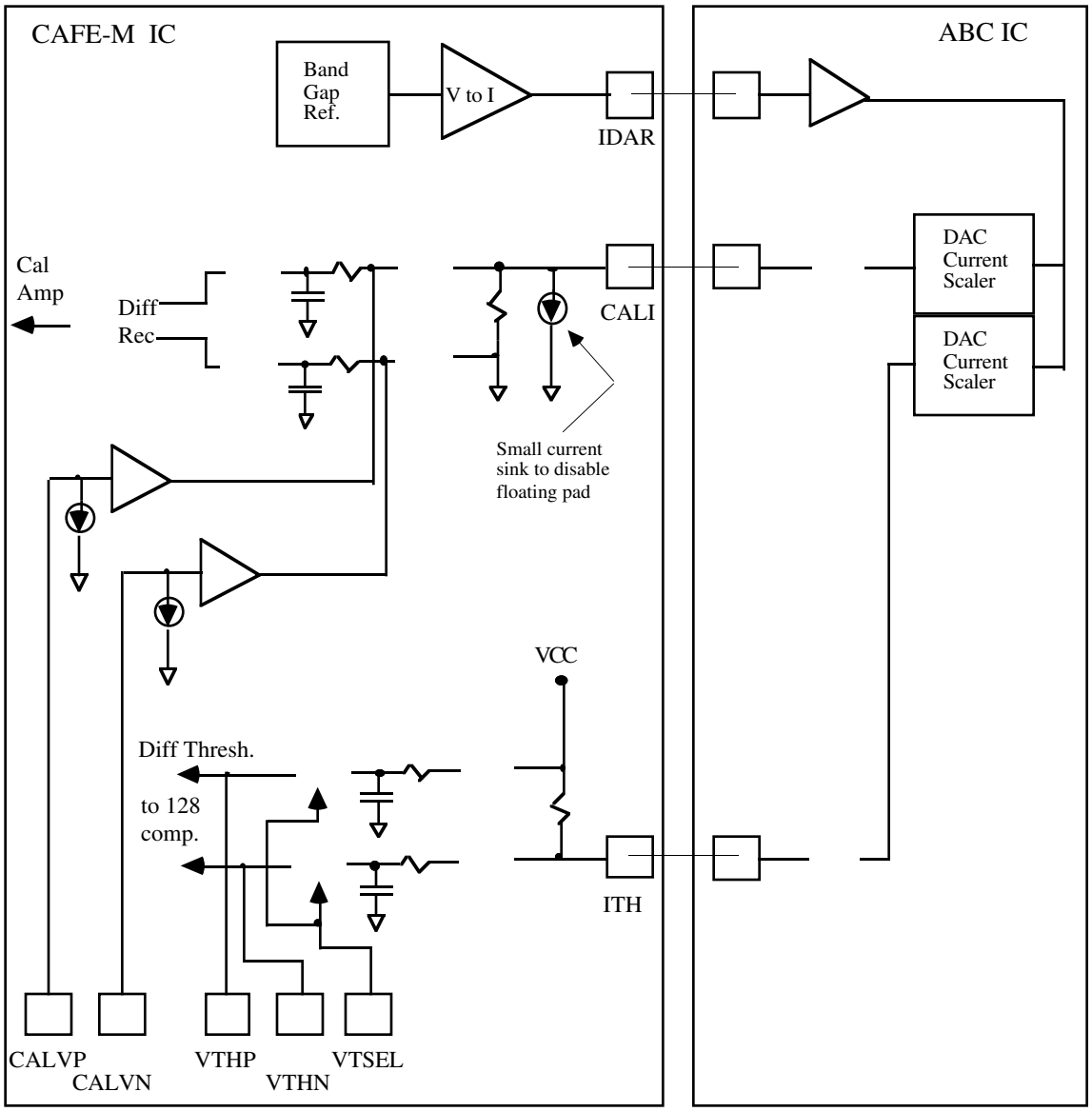

Figure 4: Block Diagram of DAC Reference Circuit

Table 1: Pad List

IN0 .. IN127	128 input data channels
SSGND	Ground of Strip Detector
OUT0 .. OUT127	128 output data channels
OUTRL	Low output reference current
OUTRH	High output reference current
DRET	Ground return to digital processing IC
VCC	Chip power
GND	Chip ground
VI1	Bias for front-end transistor
VCSP	Internal bias bus for diagnositcs
VCSN	Internal bias bus for diagnostics
IDAR	Reference current for DACs on digital processing IC
ITH	Current mode threshold control
VTHP	High side of differential voltage threshold control
VTHN	Low side of differential voltage threshold control
VTSEL	Threshold control mode selection
CALI	Current mode calibration amplitude control
CALVP	High side of differential voltage calibration amplitude control
CALVN	Low side of differential voltage calibration amplitude control
CALD0	Address 0 for calibration channels
CALD1	Address 1 for calibration channels
CALSP	High side of calibration strobe
CALSN	Low side of calbiration strobe
CBUS0	Calibration Bus #0 for channels 0, 4, .. 124
CBUS1	Calibration Bus #1 for channels 1, 5, .. 125
CBUS2	Calibration Bus #2 for channels 2, 6, .. 126
CBUS3	Calibration Bus #3 for channels 3, 7, .. 127

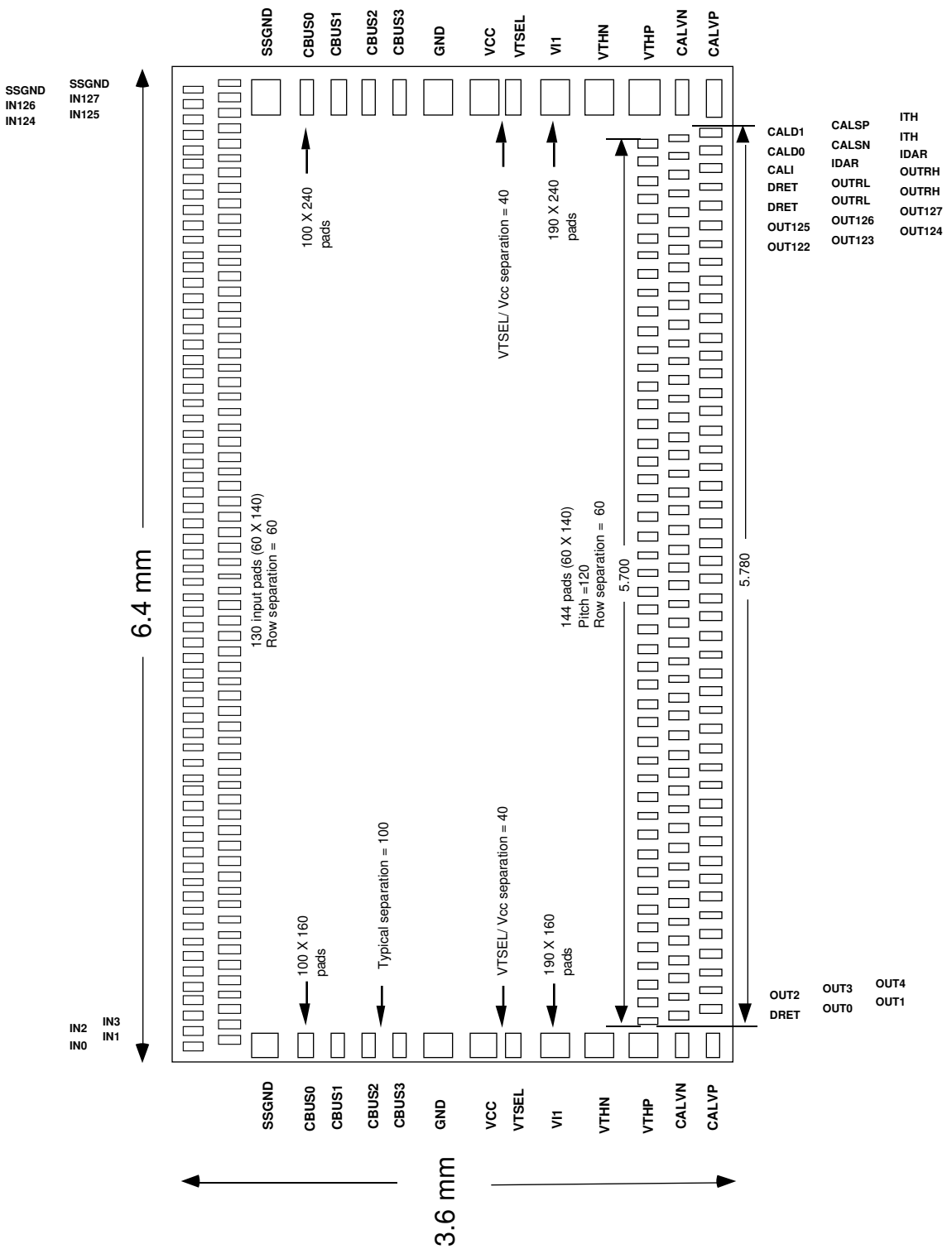

Figure 5: Pad Layout

This diagram will be redrawn accurately after pad coordinates are established. Relative pad positions are as shown. Overall chip size is current estimate. Opening for diagnostic probe points are not yet shown.

Table 2: Pad Coordinates and Sizes

X, Y Coordinates refer to layout of Figure 5 with X measuring to the right and Y measuring up. The orgin is at lower left corner at center of scribe line.
Pad sizes are for metal with opening ?? µm smaller.

Pad Name	XCoord	YCoord	XSize	YSize
SSGND'0		5734	190	160
CBUS0'0			100	160
CBUS1'0			100	160
CBUS2'0			100	160
CBUS3'0			100	160
GND'0			190	160
VCC'0			190	160
VTSEL'0			100	160
VI1'0			190	160
VTHN'0			190	160
VTHP'0			190	160
CALVN'0			100	160
CALVP'0			100	160
DRET'0			140	60
OUT0			140	60
OUT1			140	60
OUT2			140	60
OUT3			140	60
OUT4			140	60
OUT5			140	60
OUT6			140	60
OUT7			140	60
OUT8			140	60
OUT9			140	60
OUT10			140	60
OUT11			140	60
OUT12			140	60
OUT13			140	60
OUT14			140	60
OUT15			140	60
OUT16			140	60
OUT17			140	60
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OUT66			140	60
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OUT68			140	60
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OUT70			140	60
OUT71			140	60
OUT72			140	60
OUT73			140	60
OUT74			140	60

OUT75	140	60	OUT124	140	60
OUT76	140	60	OUT125	140	60
OUT77	140	60	OUT126	140	60
OUT78	140	60	OUT127	140	60
OUT79	140	60	DRET'1	140	60
OUT80	140	60	OUTRL'0	140	60
OUT81	140	60	OUTRH'0	140	60
OUT82	140	60	DRET'2	140	60
OUT83	140	60	OUTRL'1	140	60
OUT84	140	60	OUTRH'1	140	60
OUT85	140	60	CALI	140	60
OUT86	140	60	IDAR'0	140	60
OUT87	140	60	IDAR'1	140	60
OUT88	140	60	CALD0	140	60
OUT89	140	60	CALSN	140	60
OUT90	140	60	ITH'0	140	60
OUT91	140	60	CALD1	140	60
OUT92	140	60	CALSP	140	60
OUT93	140	60	ITH'1	140	60
OUT94	140	60	CALVP'1	100	240
OUT95	140	60	CALVN'1	100	240
OUT96	140	60	VTHP'1	190	240
OUT97	140	60	VTHN'1	190	240
OUT98	140	60	VI1'1	190	240
OUT99	140	60	VTSEL'1	100	240
OUT100	140	60	VCC'1	190	240
OUT101	140	60	GND'1	190	240
OUT102	140	60	CBUS3'1	100	240
OUT103	140	60	CBUS2'1	100	240
OUT104	140	60	CBUS1'1	100	240
OUT105	140	60	CBUS0'1	100	240
OUT106	140	60	SSGND'1	190	240
OUT107	140	60	SSGND'2	140	60
OUT108	140	60	SSGND'3	140	60
OUT109	140	60	IN127	140	60
OUT110	140	60	IN126	140	60
OUT111	140	60	IN125	140	60
OUT112	140	60	IN124	140	60
OUT113	140	60	IN123	140	60
OUT114	140	60	IN122	140	60
OUT115	140	60	IN121	140	60
OUT116	140	60	IN120	140	60
OUT117	140	60	IN119	140	60
OUT118	140	60	IN118	140	60
OUT119	140	60	IN117	140	60
OUT120	140	60	IN116	140	60
OUT121	140	60	IN115	140	60
OUT122	140	60	IN114	140	60
OUT123	140	60	IN113	140	60

IN112	140	60	IN63	140	60
IN111	140	60	IN62	140	60
IN110	140	60	IN61	140	60
IN109	140	60	IN60	140	60
IN108	140	60	IN59	140	60
IN107	140	60	IN58	140	60
IN106	140	60	IN57	140	60
IN105	140	60	IN56	140	60
IN104	140	60	IN55	140	60
IN103	140	60	IN54	140	60
IN102	140	60	IN53	140	60
IN101	140	60	IN52	140	60
IN100	140	60	IN51	140	60
IN99	140	60	IN50	140	60
IN98	140	60	IN49	140	60
IN97	140	60	IN48	140	60
IN96	140	60	IN47	140	60
IN95	140	60	IN46	140	60
IN94	140	60	IN45	140	60
IN93	140	60	IN44	140	60
IN92	140	60	IN43	140	60
IN91	140	60	IN42	140	60
IN90	140	60	IN41	140	60
IN89	140	60	IN40	140	60
IN88	140	60	IN39	140	60
IN87	140	60	IN38	140	60
IN86	140	60	IN37	140	60
IN85	140	60	IN36	140	60
IN84	140	60	IN35	140	60
IN83	140	60	IN34	140	60
IN82	140	60	IN33	140	60
IN81	140	60	IN32	140	60
IN80	140	60	IN31	140	60
IN79	140	60	IN30	140	60
IN78	140	60	IN29	140	60
IN77	140	60	IN28	140	60
IN76	140	60	IN27	140	60
IN75	140	60	IN26	140	60
IN74	140	60	IN25	140	60
IN73	140	60	IN24	140	60
IN72	140	60	IN23	140	60
IN71	140	60	IN22	140	60
IN70	140	60	IN21	140	60
IN69	140	60	IN20	140	60
IN68	140	60	IN19	140	60
IN67	140	60	IN18	140	60
IN66	140	60	IN17	140	60
IN65	140	60	IN16	140	60
IN64	140	60	IN15	140	60

IN14	140	60	IN6	140	60
IN13	140	60	IN5	140	60
IN12	140	60	IN4	140	60
IN11	140	60	IN3	140	60
IN10	140	60	IN2	140	60
IN9	140	60	IN1	140	60
IN8	140	60	IN0	140	60
IN7	140	60			

Table 3: Tabulation of Simulated Detector Signal

Time [ns]	Current [μA]	8.5	0.4317	18.5	0.0068
-1.0	0.0000	9.0	0.3383	19.0	0.0064
-0.5	0.0000	9.5	0.1628	19.5	0.0060
0.0	0.0000	10.0	0.0253	20.0	0.0056
0.5	0.1850	10.5	0.0195	20.5	0.0052
1.0	0.3931	11.0	0.0183	21.0	0.0048
1.5	0.4027	11.5	0.0172	21.5	0.0044
2.0	0.4025	12.0	0.0161	22.0	0.0040
2.5	0.4055	12.5	0.0151	22.5	0.0037
3.0	0.4124	13.0	0.0142	23.0	0.0033
3.5	0.4242	13.5	0.0133	23.5	0.0030
4.0	0.4373	14.0	0.0125	24.0	0.0027
4.5	0.4489	14.5	0.0117	24.5	0.0024
5.0	0.4615	15.0	0.0110	25.0	0.0021
5.5	0.4675	15.5	0.0103	25.5	0.0017
6.0	0.4709	16.0	0.0096	26.0	0.0013
6.5	0.4718	16.5	0.0090	26.5	0.0008
7.0	0.4725	17.0	0.0084	27.0	0.0002
7.5	0.4665	17.5	0.0078	27.5	0.0000
8.0	0.4588	18.0	0.0073		

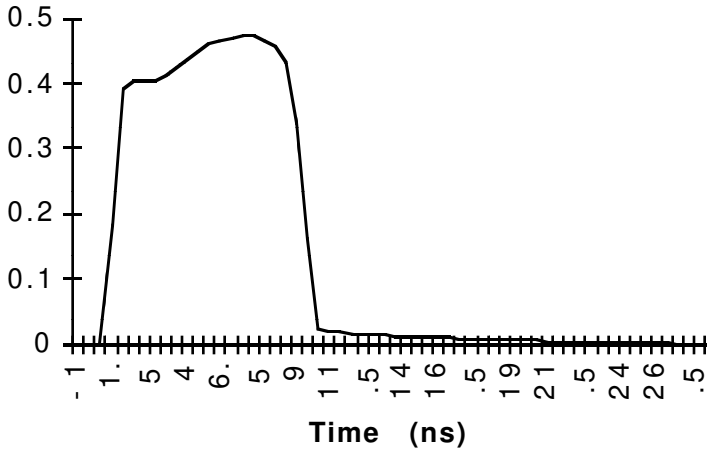

Figure 6: Simulated Depleted Detector n-Strip Signal
Signal is for an irradiated n-strip detector. For an unirradiated detector, the time scale should be scaled shorter by the ratio 0.60.
[See reference (9) J. Leslie, et al.]