

Project Specification

Project Name: DORIC3

Version: 1.01

Approval:

	name	signature	date
Project Manager	D. J. White		

Distribution for all updates:

Project Manager: D. J. White

Customer: A. R. Weidberg

Group Leader responsible for Project: M. J. French

Project Managers of related projects: D. A. Campbell, R. L. Wastie

Additional distribution at PDR and FDR:

Electronics System Design Group Leader:

Micro Electronics System Design Group Leader:

Design Support Group Leader:

Management Support Services Group Leader:

Electrical and Control Design Group Leader:

1.0 Scope

To design a further iteration of the DORIC optical receiver. This will be performed using a new process as the previous bipolar process is no longer available to external users. A new decoding scheme will be designed to suit the revised transmission protocol. Output signals will be made compatible with LVDS voltage levels.

The job began as a minor redesign to correct slow digital circuitry. The new process and major changes to requirements make this a completely new design.

The first version of DORIC had LED driver test structures on it. A dual LED driver circuit will be designed as a separate device. See LDC Project Specification.

2.0 Related projects and documents

DORIC, A Front End Clock and L1 Distribution Chip, J. R. Gorbald and P. Seller.

ABC (Atlas Binary Chip) Project Specification, D. A. Campbell, RAL.

Biphase Mark Encoder and LED Drive Control Chip, R. L. Wastie, Oxford Nuclear Physics.

LDC (LED Driver Circuit) Project Specification, D. J. White, RAL.

Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI). Draft 1.3 IEEE P1596.3-1995.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

DORIC will be a single channel device. It will receive and decode the biphase mark encoded bunch crossing clock and first level trigger plus slow control signals (data). The biphase mark encoding scheme is shown as figure 1.

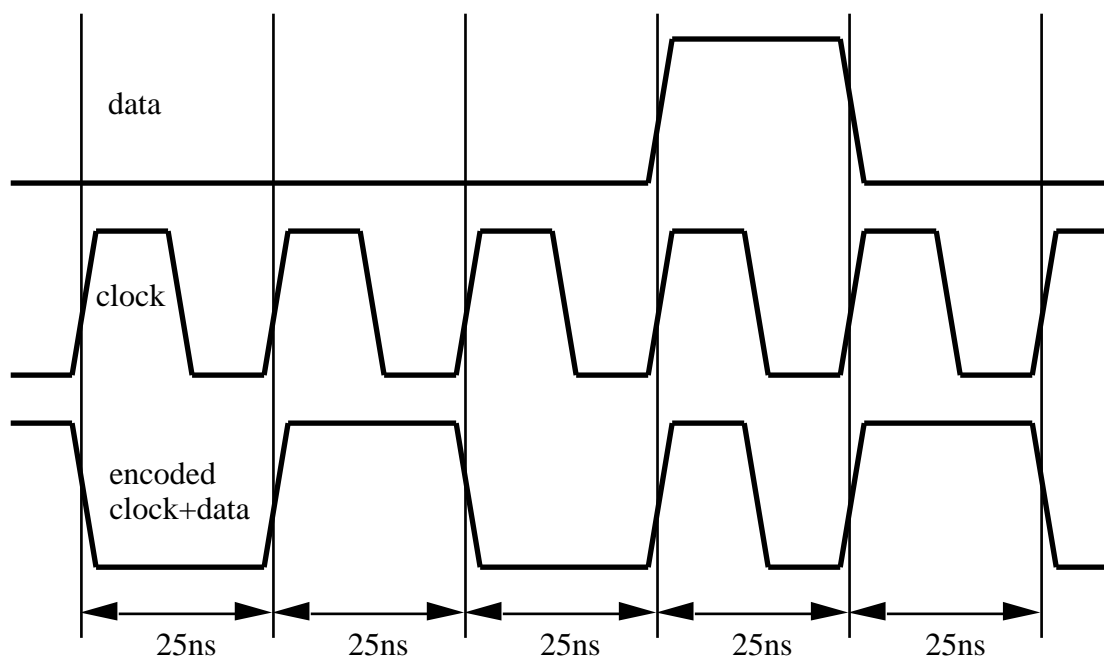


Figure 1. Biphase mark encoded clock and data signals.

Biphase mark encoding sends transitions corresponding to clock leading edges only with extra transitions at clock trailing edges to indicate data 1's. Clock has to be regenerated from leading edge transitions and data from trailing edge transitions.

3.1.2 Input Signal Level Requirements

The LED producing the optical signal will be current biased to improve its switching speed. The optical output will switch between a low level defined by the bias current to a high level defined by bias plus signal current. This optical signal will be received by a PiN photodiode which will produce an output current proportional to its optical input power. The low level signal defined by LED bias will produce an output current from the photodiode, the photodiode will also have leakage current which will increase with irradiation. The sum of these two currents is not expected to exceed $1\mu\text{A}$. Signal current step amplitude is expected to be $8\mu\text{A}$. The photodiode output current will feed into DORIC input. DORIC must function correctly with low level input current range from 0 to $2\mu\text{A}$, and with signal current step amplitude range from less than $6\mu\text{A}$ to greater than $12\mu\text{A}$, figure 2. The dc and signal current operating ranges must be made as large as possible during circuit design. Ideally DORIC should work for either polarity of current to suit either polarity of PiN photodiode.

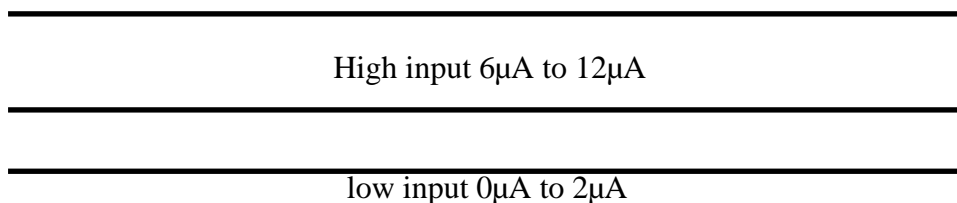


Figure 2. Input signal level definition, either polarity.

The PiN photodiode capacitance is not well characterised so DORIC must be designed to function correctly with a range of photodiode capacitances from 0 to 2pF . In addition to photodiode capacitance the opto-hybrid has approximately 2pF capacitance to substrate from each of the photodiode terminals. This extra capacitance will increase the noise of DORIC input stage and cause feedback problems through ground loops. These effects are to be minimised by design.

3.1.3 Noise Requirements

Total circuit noise must be low enough to guarantee a bit error rate (BER) of 10^{-11} or better, at end of life, after irradiation. This requires a signal-to-noise ratio (signal:rms noise) at the comparator input of 14:1 or higher (from formulae by Rice, 1944 and Personick, 1973). Clock output jitter must be less than $\pm 1\text{ns}$ maximum, or approximately 250ps rms, if signals at the comparator have $\sim 4\text{ns}$ rise and fall times, this requires a signal-to-noise ratio of 16:1 or higher. DORIC must be designed so that its internal noise will give a signal-to-noise ratio better than 20:1 to allow for further degradation caused by the shot noise of detector current, supply noise and interference. Rejection of supply noise and interference will be optimised during design but there will be a limit to the amount of supply noise and interference which can be tolerated.

Clock jitter will be affected by asymmetry or jitter of the input signal. If the encoded clock signal received from the PiN photodiode is not accurate due to the encoding, the transmission system, or both, DORIC will not correct it. If the signal is very asymmetric or jittery the decoding may fail and DORIC may produce bad data.

At start-up the asymmetry of the encoded clock waveform must not exceed $\pm 3\text{ns}$. Any asymmetry of the signal can be measured by reading it back through the ABC in clock feedthrough mode and sending single data bits at a low rate to flip the phase. The asymmetry may then be corrected by adjustment of encoded signals.

3.1.4 Output Requirements

DORIC must decode and produce differential outputs for clock and data. The biphas mark encoded input signal and true outputs are shown as figure 3.

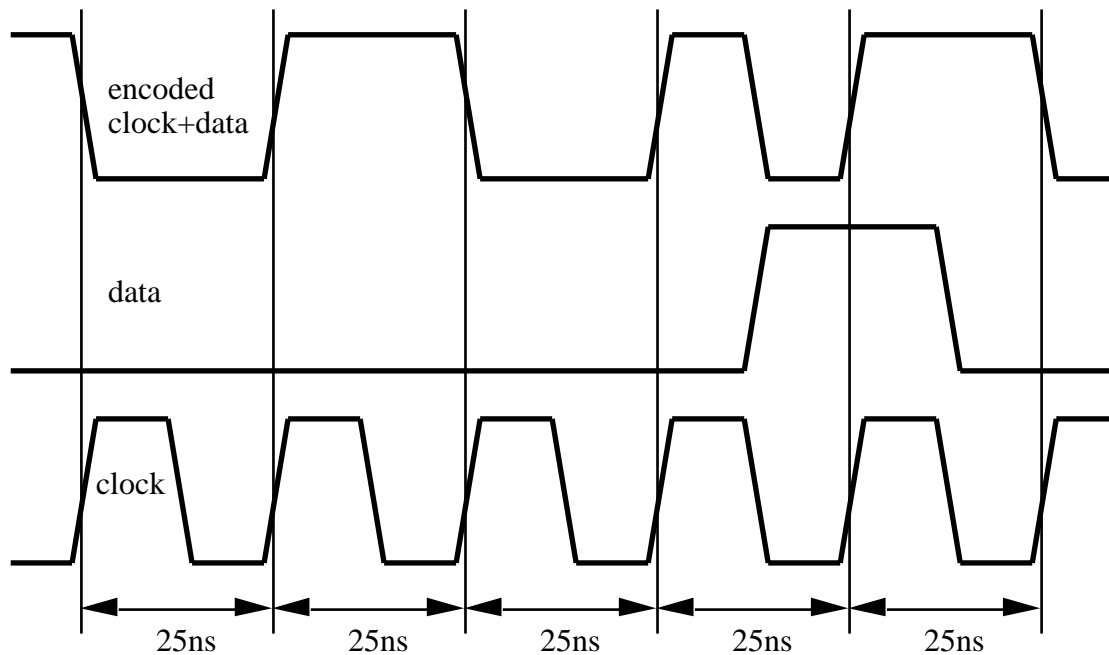


Figure 3. Ideal decoded clock and data outputs.

Clock leading edges (indicated on figure 3) are produced by transitions of the input, trailing edges are produced internally. Clock output duty cycle must be close to 50%; mark and space must each be $12.5\text{ns} \pm 1\text{ns}$, or better. Data output must be approximately one full clock cycle wide and suitably phased with respect to clock leading edges to guarantee minimum setup and hold times of 8ns for the ABC. Data outputs will be non-return-to-zero (NRZ). Input to output propagation delay of clock leading edges (not shown on figure 3 for clarity) approximately 3ns.

Two sets of clock and data outputs are required; clk0 and data0, clk1 and data1. Two control inputs must be provided to enable or disable each set of outputs. Control levels for clk0 and data0 will be nominally $\text{Lo} = 0\text{V} \pm 1\text{V} = \text{enable}$, $\text{Hi} = +4\text{V} \pm 1\text{V} = \text{disable}$. Control levels for clk1 and data1 will be nominally $\text{Lo} = 0\text{V} \pm 1\text{V} = \text{disable}$, $\text{Hi} = +4\text{V} \pm 1\text{V} = \text{enable}$. These levels make it possible for the control signal of each module to operate the reserve/redundant output of the previous module, thus saving one wire. Control inputs will be pulled down with a $10\text{k}\Omega$ resistance so 0 outputs will be enabled and 1 outputs disabled if control signals are not connected.

Outputs will be designed to match the LVDS voltage specification. This is a balanced differential voltage output centred on $1200\text{mV} \pm 75\text{mV}$ with a minimum signal swing of 250mV , maximum of 400mV . DORIC may be made with slightly lower output impedance and slightly higher current capability than a standard LVDS output stage because the high capacitance loading of 12 ABCs plus hybrid tracking (estimated as 100pF) may produce very low impedance transmission lines. The rise and fall times will be made slightly slower than a standard LVDS output stage to minimise noise injection into sensitive front end electronics. Rise and fall times 20% to 80% nominally 800ps .

3.1.5 General Requirements

The customer requested that passive circuitry should be used for decoding, to avoid the problems which could occur with a phase locked loop system.

After DORIC has been powered up the decoder circuitry must be ready to accept data within 1µs of starting the clock.

DORIC will be required to operate at an ambient temperature up to 25°C during test and down to as low as -10°C when in use on the experiment.

Supply voltage nominally +4V±5%. DORIC must withstand an overvoltage of up to 2V without damage and function correctly with minimal decoupling or other external components over the specified temperature and nominal supply voltage ranges.

Power dissipation will be dominated by the output stage currents needed to drive low impedance or high capacitance loads. Estimate ~200mW for the four output drivers. The optical receiver and biphasic mark decoding circuitry should use less than 50mW.

Any bond pads which may be connected to long lines or to other modules by connectors should aim for electrostatic discharge (ESD) protection to IEC 801-2 compliance level 2, or higher. It may not be possible to achieve a high degree of protection on all bond pads for reasons of noise or capacitance loading. All bond pads to be made as well protected as possible without impairing function. Careful handling may be needed to prevent damage to sensitive pads during assembly.

3.1.6 Physical Requirements

Chip width 2.0mm, chip length 2.5mm, to fit into available space. Photodiode connections at one end, all other connections ideally at the other end. No preference for layout of connections. Pad layout was discussed at IDR. An extra bias input was requested in the lower right corner. An extra input return pad above input would allow reversal of the detector polarity without lead crossover, this option may give better dynamic range. Test structures may be added in unused areas at the designers discretion. The following scheme was approved, figure 4.

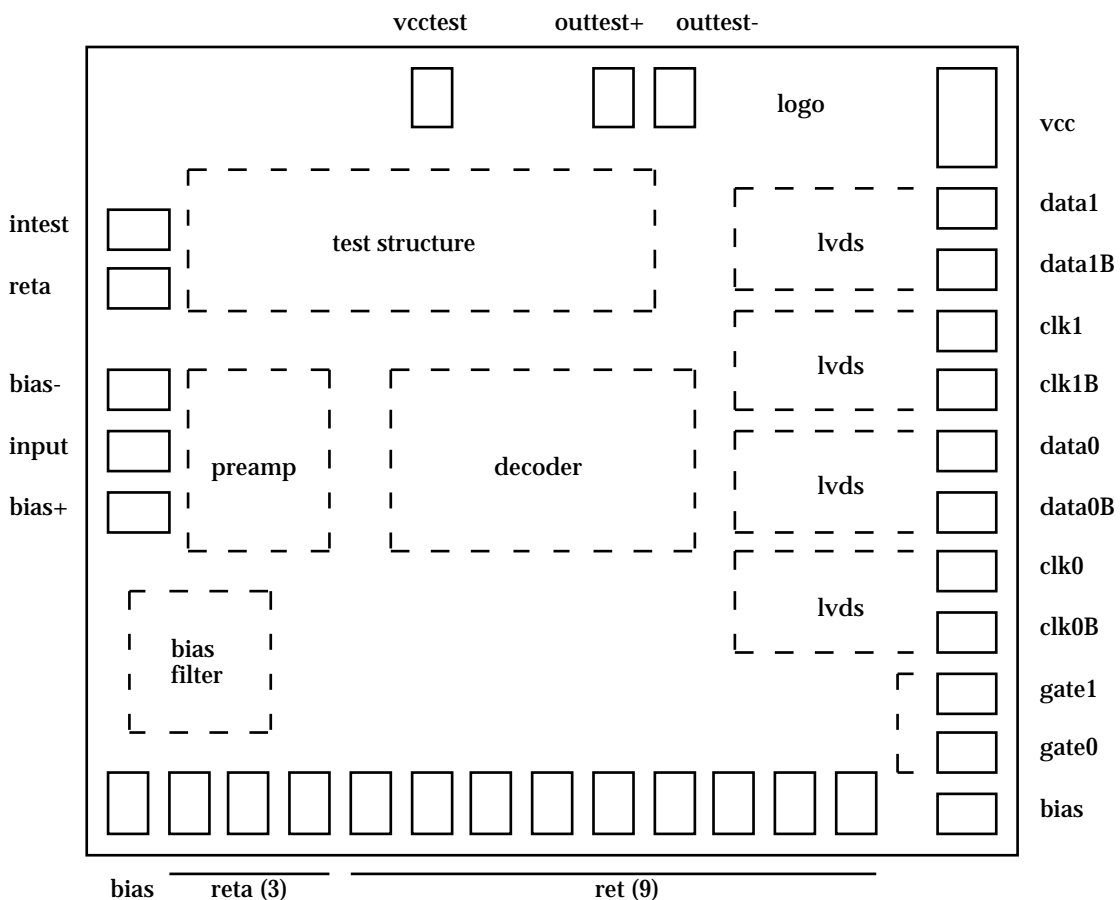


Figure 4. DORIC pad layout and naming.

3.1.7 Pad numbering and names

Pads are numbered in an anticlockwise direction starting at bias- for convenience.

Pad #	Pad Name	Function
1	bias-	PiN photodiode signal return for negative bias
2	input	PiN photodiode signal connection
3	bias+	PiN photodiode signal return for positive bias
4	bias	PiN photodiode bias supply, common with 17
5	reta	analogue supply return
6	reta	analogue supply return
7	reta	analogue supply return
8	ret	digital supply return
9	ret	digitalsupply return
10	ret	digital supply return
11	ret	digital supply return
12	ret	digital supply return
13	ret	digital supply return
14	ret	digital supply return
15	ret	digital supply return
16	ret	digital supply return
17	bias	PiN photodiode bias supply, common with 4
18	gate0	output0's enable, active low, 10k pulldown
19	gate1	output1's enable, active high, 10k pulldown
20	clk0B	LVDS clock output complement
21	clk0	LVDS clock output true
22	data0B	LVDS data output complement
23	data0	LVDS data output true
24	clk1B	LVDS clock output complement
25	clk1	LVDS clock output true
26	data1B	LVDS data output complement
27	data1	LVDS data output true
28	vcc	supply, +4V, large enough for several bond wires
29	outtestB	test structure output complement
30	outtest	test structure output true
31	vcctest	test structure supply, +4V
32	intest	test structure input
33	reta	analogue supply return (intest signal return)

29 - 33 only
used for test
purposes

The two connected pads bias- and bias+ are supplied to avoid crossing of input bond wires. For positive bias supply voltage, input and bias+ are connected to PiN photodiode anode (p) and cathode (n) respectively. For negative bias supply voltage, bias- and input are connected to PiN photodiode anode (p) and cathode (n) respectively. Positive bias is the preferred connection but greater signal dynamic range may be obtained by using negative bias.

Three analogue supply returns and nine digital supply returns have been provided. All may be used if necessary for stability and low noise but it is expected that the circuit will function correctly with less. A good starting point would be two analogue and three or four digital returns. The vcc pad is large enough to take several bond wires. A minimum of two are needed to handle the supply current, more may be used to minimise inductance.

3.2 Specification of deliverables

See Requirements.

3.3 Manufacturing

The circuitry will be designed using AMS 0.8µm BICMOS models and design rules for fabrication on an AMS MPW run. Submission date, 31st January 1997.

This process is not qualified as radiation hard but, if transistors are limited to npn bipolars only and if the circuitry is designed to minimise and to allow for degradation, it may produce sufficiently radiation tolerant devices.

3.4 Testing and product control

Test requirements were discussed at IDR by R. Nickerson, M. J. French, D. A. Campbell and D. J. White. A. R. Weidberg sent comments by e-mail, P. Seller was not available. A draft test plan has been written. Some of the devices will be tested for use, some will be tested, irradiated and tested again to see if they still function after a dose of 2×10^{14} n/cm², equivalent to more than 10 years running on LHC.

3.5 Shipping and Installation

No clear definition of requirements at present.

3.6 Maintenance and further orders

All documentation will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager:	D. J. White	david.white@rl.ac.uk
Engineer:	D. J. White	david.white@rl.ac.uk
Customer:	A. R. Weidberg	Anthony.Weidberg@cern.ch
Finance:	R. Nickerson	r.nickerson1@ph.ox.ac.uk

4.2 Deliverables

Project documentation. Test results. Application notes. Tested and untested die.

4.3 Project plan

Milestones, schedule, see also 4.4.

Design and layout started after PDR.

AMS 0.8µm BICMOS MPW submission, 31st January 1997.

Testing discussed at IDR, test fixtures to be built for May 1997.

Tested die required for use by June 1997.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm Project Specification, held on 8th August 1996.

Interim Design Review (IDR) to review project progress and test requirements, optimistically planned for September 1996, held on 12th December 1996.

Final Design Review (FDR) to confirm the devices as designed meet requirements of Project Specification, including any change orders. Planned for October 1996, to be held May/June 1997.

Concluding Review (CR) and Maintenance Review (MR) after delivery.

4.5 Training

Minimal training requirements, probably some familiarisation time for new software, device models and design rules.

4.6 CAE and test equipment

Workstation, software, support, to suit selected process.

Test equipment as defined in test plan. Test boards for die mounted in temporary, reusable packaging.

4.7 Costs and finance

Original estimate based on IMEC/Europractice MPW run using AMS, cost of 10 prototypes is ~£3k, possibly double to guarantee 20. By going direct to AMS, cost for 20 prototype chips is ~£2k. An extra 20 may be ordered for ~£400.

Test board and components are unlikely to cost more than £1k.

No financial authority given to project manager, all requisitions to be authorised by M. Tyndel, or by M. Edwards for items on which VAT may be recovered.

4.8 IPR and confidentiality

Technology Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this project.

4.10 Environmental impact

Very little from final product.

Small amounts of inert substance which may be safely disposed of as landfill.