Project Specification

Project Name: DORIC4

Version: 1.00

Approval:

	name	signature	date
Project Manager	**D. J. White**		

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1.0 Scope

To design a further iteration of the digital optical receiver integrated circuit (DORIC4). The input stage will be modified to receive the high level, high dynamic range signals produced by a vertical cavity surface emitting laser (VCSEL). The biphase mark decoding circuitry will be improved to assist clock and command recovery from encoded input signals with mark-space variation and jitter.

2.0 Related projects and documents

DORIC3 Project Specification, D. J. White, RAL.
ABC (Atlas Binary Chip) Project Specification, D. A. Campbell, RAL.
Biphase Mark Encoder and LED Drive Control Chip, R. L. Wastie, Oxford Nuclear Physics.
LDC (LED Driver Circuit) Project Specification, D. J. White, RAL.
Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI). Draft 1.3 IEEE P1596.3-1995.
VCSEL Tests, I. Mandic and A. Weidberg, Oxford University.

3.0 Technical Aspects

3.1 Requirements

3.1.1 General Description

DORIC4 will be a single channel device. It will receive and decode biphase mark encoded clock and command signals. The encoding scheme is shown as figure 1.

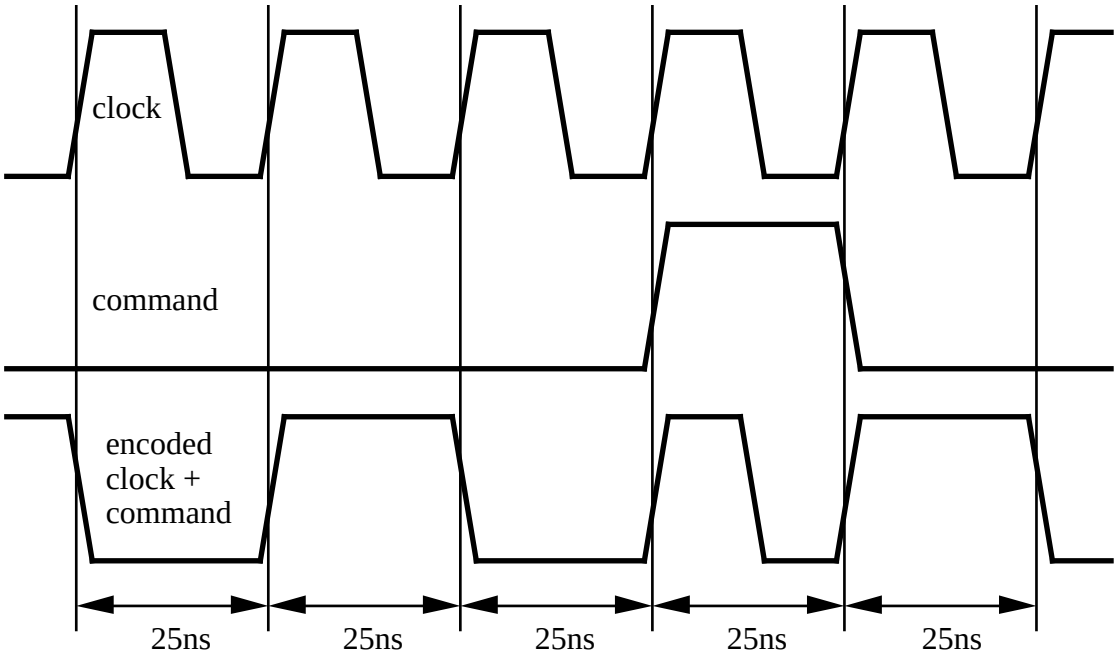

Figure 1. Biphase mark encoded clock and command signals.

Biphase mark encoding sends transitions corresponding to bunch crossing clock leading edges only. Extra transitions at clock trailing edges indicate command signals.

The bunch crossing clock has to be regenerated from leading edge transitions and command from the extra trailing edge transitions. Biphase mark encoded signals will be used to drive a VCSEL to produce an optical output.

The high level optical signal produced by a VCSEL will depend on its drive current, lasing threshold and efficiency, the low level optical signal may be zero or some residual value. This optical signal will be received by a PiN photodiode which will produce an output current proportional to its optical input power. The received signal waveform and edge timing will be considerably less perfect than the idealised version shown in figure 1, see VCSEL Tests document for more details.

3.1.2 Input Signal Level Requirements

The high level signal received by a PiN photodiode should lie between 200µW and 2mW. Assuming a responsivity of 0.3A/W, the high level signal current will lie between 60µA and 600µA. The low level signal may be a significant percentage of the high level signal. Assuming a maximum of 33% for design purposes, the low level signal will lie between 0µA and 20µA or 200µA. The photodiode will also have leakage current which will increase with irradiation but this should be less than 1µA. DORIC4 must function correctly over this range of inputs, shown as figure 2.

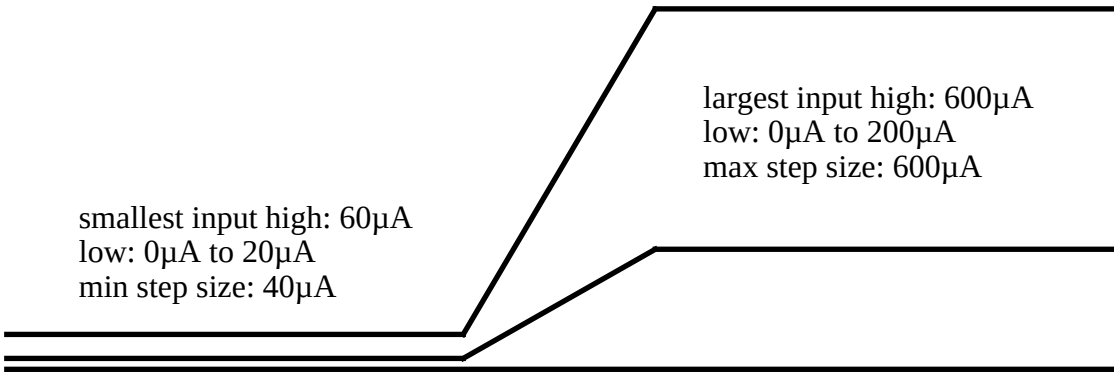

Figure 2. Input signal current amplitude range.

The smallest to largest signal operating range should be made as large as possible during circuit design. Ideally DORIC4 should work for either polarity of current to suit either polarity of PiN photodiode and/or bias voltage. The PiN photodiode and its packaging are not well characterised so DORIC4 must be designed to function correctly with a range of photodiode capacitances from 0 to 2pF and with stray capacitance of up to 4pF from each photodiode terminal to ground.

3.1.3 Noise Requirements

Total circuit noise must be low enough to guarantee a bit error rate (BER) of 10^{-11} or better, at end of life, after irradiation. This requires a signal-to-noise ratio (signal:rms noise) of 14:1 or higher (calculated from formulae by Rice, 1944 and Personick, 1973). DORIC4 must be designed to give a signal-to-noise ratio (SNR) of better than 25:1 (ratio of smallest input signal step size to internal rms noise) to allow for further degradation caused by supply noise and interference. For the large signals produced by VCSELs a high SNR is easy to achieve. Rejection of supply noise and interference will be optimised during design but there will be a practical limit to the amount of supply noise and interference which can be tolerated.
Crosstalk from data link VCSEL driver output to PiN may be cause large BER. VCSEL drivers may be run at low output to minimise crosstalk. The minimum input

signal level may need to be raised to overcome this problem. Suggested minimum is 450µW optical giving 100µA minimum step size electrical signal.

3.1.4 Output Requirements

DORIC4 must decode and produce differential outputs for clock and command signals. A biphase mark encoded input signal with jitter and/or pulse length distortion with respect to a reference clock and the decoded true outputs are shown as figure 3.

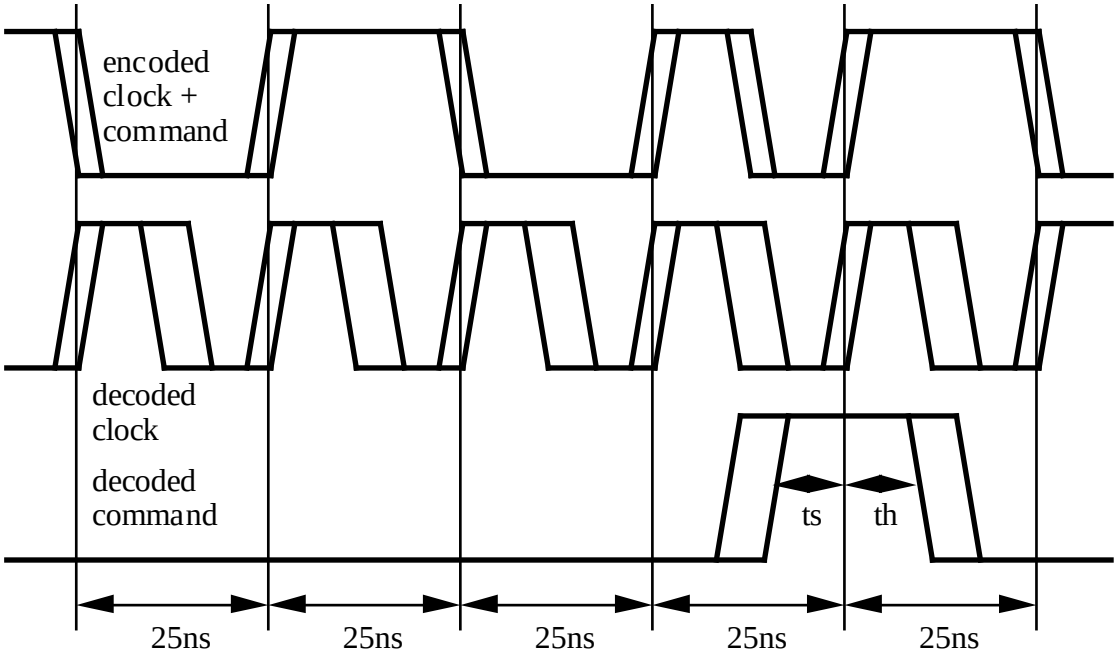

Figure 3. Worst case decoded clock and command outputs.

Clock leading edges (indicated on figure 3) are produced by transitions of the input, trailing edges are produced internally and will have more error than leading edges. Clock output duty cycle must be close to 50%; mark and space must each be 12.5ns ± 1ns, or better to meet ABC input requirements. Clock output jitter and duty cycle will depend mainly on the quality of the received signal. Command outputs must be approximately one full clock cycle wide and suitably phased with respect to clock leading edges to guarantee minimum setup and hold times (ts and th on figure 3) of 8ns for the ABC. Command outputs will be non-return-to-zero (NRZ). Input to output propagation delay of clock leading edges (not shown on figure 3 for clarity) approximately 3ns.
Two sets of clock and command outputs are required; clk0 and com0, clk1 and com1. Two control inputs must be provided to enable or disable each set of outputs. Control levels for clk0 and com0 will be nominally Lo = 0V±1V = enable, Hi = +4V±1V = disable. Control levels for clk1 and com1 will be nominally Lo = 0V±1V = disable, Hi = +4V±1V = enable. These levels make it possible for the control signal of each module to operate the reserve/redundant output of the previous module, thus saving one wire. Control inputs will be pulled down with a 10kohm resistance so 0 outputs will be enabled and 1 outputs disabled if control signals are not connected.
Outputs will be designed to match the LVDS voltage specification. This is a balanced differential voltage output centred on 1200mV ± 75mV with a minimum signal swing of 250mV, maximum of 400mV. DORIC4 may be made with slightly lower output impedance and slightly higher current capability than a standard LVDS output stage because the high capacitance loading of 12 ABCs plus hybrid tracking (estimated as 100pF) may produce very low impedance transmission lines. The rise and fall times

will be made slightly slower than a standard LVDS output stage to minimise noise injection into sensitive front end electronics. Rise and fall times 20% to 80% nominally 1ns.

3.1.5 General Requirements

After DORIC4 has been powered up the clock must be run for at least 25µs to allow the circuitry to settle before transmitting command signals.
DORIC4 will be required to operate at an ambient temperature up to 25°C during test and down to as low as -10°C when in use on the experiment.
Supply voltage nominally +4V±5%. DORIC4 must withstand an overvoltage of up to 2V without damage and function correctly with minimal decoupling or other external components over the specified temperature and nominal supply voltage ranges.
Power dissipation will be dominated by the output stage currents needed to drive low impedance or high capacitance loads. The four output drivers will use ~200mW in total. If possible design in a lower output current, pad programmable option. The optical receiver and biphase mark decoding circuitry should use less than 50mW.
Any bond pads which may be connected to long lines or to other modules by connectors should aim for electrostatic discharge (ESD) protection to IEC 801-2 compliance level 2, or higher. All other bond pads to be made as well protected as possible without reduction of device performance. Careful handling may be needed to prevent damage to sensitive pads during assembly.

3.1.6 Physical Requirements

Chip width 2.0mm, chip length 2.5mm, to fit into available space. Photodiode connections at one end, all other connections ideally at the other end. Pad layout to be discussed. Four input pads give balanced stray capacitance and allow reversal of the detector polarity without lead crossover. Test structures may be added in unused areas at the designers discretion. The following scheme is suggested, figure 4.

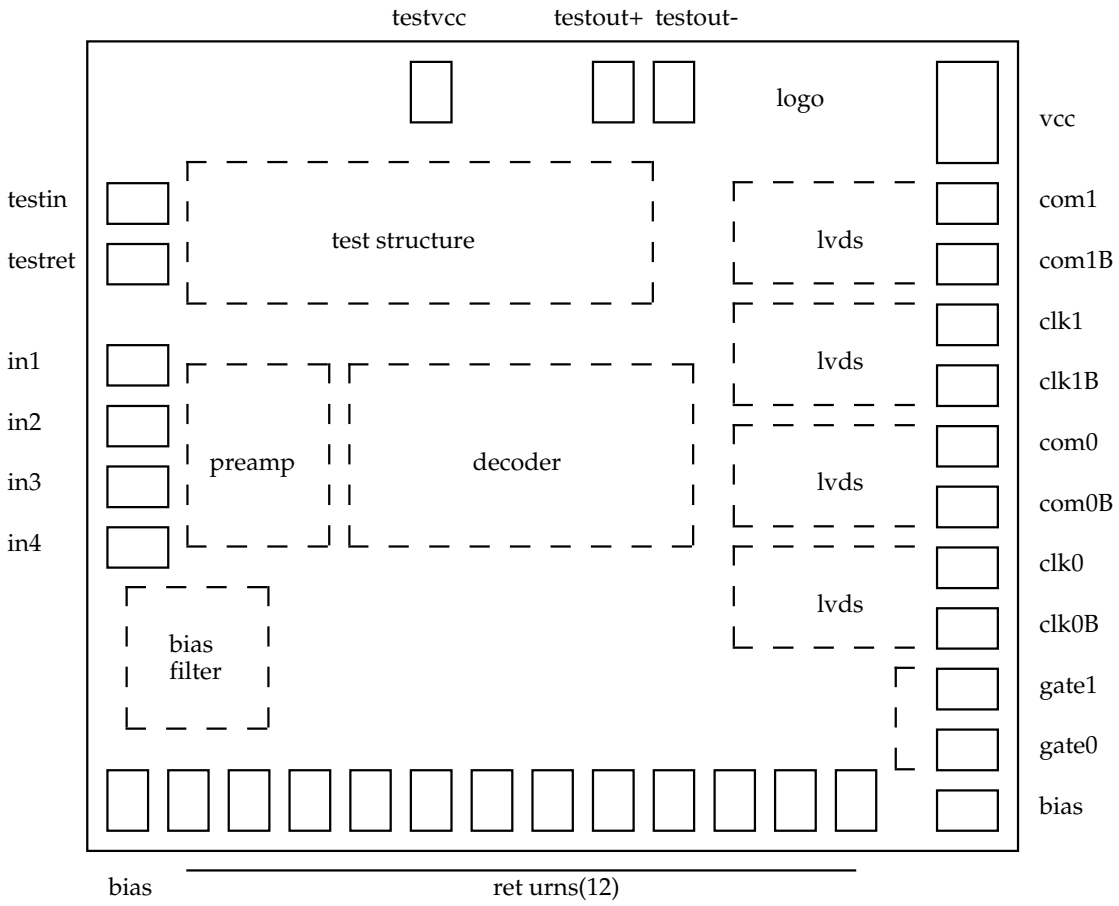

Figure 4. DORIC4 pad layout and naming.

3.1.7 Pad numbering and names

Pads are numbered in an anticlockwise direction starting at in1 for convenience.

Pad #	Pad Name	Function	
1	in1	PiN photodiode signal input	
2	in2	PiN photodiode signal input	
3	in3	PiN photodiode signal input	
4	in4	PiN photodiode signal input	
5	bias	PiN photodiode bias supply, common with 18	
6	ret	supply return	
7	ret	supply return	
8	ret	supply return	
9	ret	supply return	
10	ret	supply return	
11	ret	supply return	
12	ret	supply return	
13	ret	supply return	
14	ret	supply return	
15	ret	supply return	
16	ret	supply return	
17	ret	supply return	
18	bias	PiN photodiode bias supply, common with 5	
19	gate0	output0's enable, active low, 10k pulldown	
20	gate1	output1's enable, active high, 10k pulldown	
21	clk0B	LVDS clock0 output complement	
22	clk0	LVDS clock0 output true	
23	com0B	LVDS command0 output complement	
24	com0	LVDS command0 output true	
25	clk1B	LVDS clock1 output complement	
26	clk1	LVDS clock1 output true	
27	com1B	LVDS command1 output complement	
28	com1	LVDS command1 output true	
29	vcc	supply, +4V, pad large enough for several bond wires	
30	testoutB	test structure output complement	
31	testout	test structure output true	30 - 34 only
32	testvcc	test structure supply, +4V	used for test
33	testin	test structure input	purposes
34	testret	test structure return (testin signal return)	

Four cross-connected input pads will be supplied to avoid crossing of input bond wires if PiN connections or PiN bias require reversing.
The single vcc supply pad is large enough to take several bond wires. A minimum of two are needed to handle the supply current, more may be used to minimise inductance. A row of supply return pads will be provided. As many return pads may be bonded as are needed for good operation, six is suggested. (The input is differential and large amplitude so there is no need for a separate analogue return.)

3.2 Specification of deliverables

See Requirements.

3.3 Manufacturing

The circuitry will be designed using AMS 0.8µm BICMOS models and design rules for fabrication on an AMS MPW run. Submission date, possibly July 1998.
This process is not qualified as radiation hard but, if transistors are limited to npn bipolars only and if the circuitry is designed to minimise and to allow for degradation, it produces sufficiently radiation tolerant devices.

3.4 Testing and product control

A test plan will be written. These devices will be produced on a multi-project wafer so they will be delivered as small numbers of individual die. Probe testing is difficult but not impossible and is preferable to the alternatives (bonding, testing, removing and then re-bonding, or not testing at all). A conventional probe card and custom test driver will be designed and made. Some software may need to be developed.

3.5 Shipping and Installation

The customer will personally collect all of the deliverables.

3.6 Maintenance and further orders

All documentation will be kept for a period to be determined at Maintenance Review to facilitate maintenance and further orders.

4.0 Project Management

4.1 Personnel

Project manager:	D. J. White	djw@te.rl.ac.uk
Project engineer:	D. J. White	djw@te.rl.ac.uk
Engineer:	D. J. White	djw@te.rl.ac.uk
Customer:	A. R. Weidberg	t.weidberg1@ph.ox.ac.uk

4.2 Deliverables

Project documentation. Test results. Application notes. Tested die.

4.3 Project plan

Milestones, schedule, see also 4.4.
Design and layout start after project specification agreed at PDR, late January 1998.
Review progress and discuss test requirements at IDR, April 1998.
Complete test plan, April 1998.
AMS 0.8µm BICMOS MPW submission after FDR, July 1998.
Produce test fixtures, equipment and software, August 1998.
Planned leave, September 1998.
Commence testing, October 1998.
Tested die required for use by November 1998.

4.4 Design Reviews

Preliminary Design Review (PDR) to confirm Project Specification.
Interim Design Review (IDR) to review project progress and test requirements.
Final Design Review (FDR) to confirm the devices as designed meet requirements of Project Specification, including any change orders.
Concluding Review (CR) and Maintenance Review (MR) after delivery.

4.5 Training

Minimal training requirements, short familiarisation time for latest software issue. Assistance probably needed in setting up the software to run correctly. If assistance is not available then project timescales will need to be extended.

4.6 CAE and test equipment

Workstation, software, support, to suit selected process.
Test equipment as defined in test plan.

4.7 Costs and finance

Original estimate based on IMEC/Europractice MPW run using AMS; cost of 10 prototypes is ~£3k, possibly double to guarantee 20. By going direct to AMS; cost for 20 prototype chips is ~£2k. Larger quantities possible at increased cost.
Test fixtures and components are unlikely to cost more than £2k.
Finance to be arranged.

4.8 IPR and confidentiality

Technology Department owns the layout and schematic databases. Any masks or phototools will be procured by the Department. None of these items will be released unless the appropriate protective agreements are in place.

4.9 Safety

Low voltage, low power circuitry, no particular hazards associated with this project.

4.10 Environmental impact

Very little from final product.
Small amounts of inert substance which may be safely disposed of as landfill.