

Radiation Hardness Studies of the Front-end ASICs for the Optical Links of the ATLAS SemiConductor Tracker

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Abstract

Studies have been performed on the effects of radiation on ASICs incorporating bipolar npn transistors in the AMS 0.8 μm BiCMOS process. Radiation effects are reviewed and the approach used to achieve radiation tolerant ASICs is described. The radiation tests required to validate the ASICs for use in the ATLAS detector at the CERN Large Hadron Collider are discussed. The results demonstrate that they are sufficiently radiation tolerant for use in the ATLAS SemiConductor Tracker.

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1. Introduction

Optical links will be used in the ATLAS SemiConductor Tracker (SCT)[1] to transmit data from the detector modules to the off-detector electronics and to distribute the Timing, Trigger and Control (TTC) data from the counting room to the front-end electronics[2]. During the operation of the SCT at the Large Hadron Collider (LHC), all the on-detector components will be exposed to large fluences of charged and neutral particles. The SCT on-detector components have to be designed to be sufficiently radiation tolerant to survive 10 years of LHC operation. This paper describes the design and radiation testing of the front-end ASICs used for the SCT optical links. The radiation hardness of the other on-detector components of the optical links (PIN photodiodes, VCSELsⁱⁱ and fibres) are described in Refs[3-7].

The expected ATLAS radiation environment and the facilities used to simulate this environment are described in Section 2 and 3. The effects of radiation on bipolar transistors and the design approach used to improve the radiation tolerance are

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discussed in Section 4. The designs of the two ASICs are outlined in Section 5. The results of the radiation tests and of studies of the lifetime of the ASICs after irradiation are discussed in Section 6. Finally some conclusions are drawn in Section 7.

2. The ATLAS Radiation Environment and Test Facilities

The radiation received by the SCT will be dominated by primary and secondary particles from the proton-proton collisions. The expected fluences of charged and neutral particles have been calculated for different positions in the SCT assuming that the LHC will operate for a total integrated luminosity of $7.3 \cdot 10^{41} \text{ cm}^{-2}$ (from 3 years at low luminosity and 7 years at high luminosity)[1]. The absorbed ionising doses have been calculated for silicon (Gy(Si)). The damage due to non-ionising processes (i.e. bulk damage due mainly to charged particles and neutrons) is quoted in terms of the equivalent fluence of 1 MeV neutrons causing the same amount of damage in silicon (1 MeV (Si)) using the Non-Ionising Energy Loss (NIEL) hypothesis[8-10]. The worst case radiation levels for the SCT have been calculated for the modules closest to the beam line and an additional safety factor of 50% has been added to allow for the uncertainties in the calculations. The results are summarised in Table 1 below.

Table 1 The worst case ionisation dose and neutron fluence for the SCT after 10 years of LHC operation.

	Dose/Fluence	Units
Ionising Dose	100	kGy(Si)
Equivalent neutron fluence	$2 \cdot 10^{14}$	n (1 MeV(Si)) cm^{-2}

3. Irradiation Facilities

In this section the radiation sources used to test the ASICs are described. A neutron source was used to study the bulk damage effects and a gamma source was used to study the ionisation effects.

3.1 Neutron Irradiation facility

A reactor-based facility in Ljubljana, Slovenia (TRIGA) was used as the neutron source. The 250 kW TRIGA reactor provides a uniform neutron flux which is tunable according to the reactor power. The neutron energy spectrum falls off exponentially from 1 eV to around 1 MeV and then more quickly to a cut-off around 10 MeV[11]. The activation of metal foils has been used to calibrate the reactor and allow the neutron flux to be estimated for a given reactor power to a precision of around 10%. The neutron flux used was $2.2 \cdot 10^{12} \text{ n (1 MeV(Si)) cm}^{-2} \text{ s}^{-1}$.

3.2 Gamma Source

The gamma irradiations were performed with a Co^{60} source located at the Radiation Centre of the University of Birmingham. The Co^{60} source emits photons with energies of 1.17 MeV and 1.33 MeV. The doses were measured with Alanine dosimeters. A correction factor of 0.87 was applied to obtain the dose in silicon to take into account

the ratio of mass stopping power for silicon and Alanine[12]. The dose rate was 418 Gy(Si)/hour. There was a 3 mm thick aluminium wall between the source and the ASICs. This thickness is significantly greater than the range in aluminium of the highest energy Compton electrons (which have a kinetic energy of 1.12 MeV) which ensured that there was an approximate equilibrium for the creation and loss of electrons. This is required for the irradiation of ASICs with very thin active layers with a gamma source, in order to avoid the dose in the active region being significantly underestimated by the dosimeters. The average dose rate expected during 10 years of ATLAS operation is 1.1 Gy(Si)/hour while the dose rate expected during the periods of high luminosity LHC operation is 5.7 Gy(Si)/hour.

4. Theory of Radiation Effects and Design Approach

High energy heavy particles (protons, neutrons or heavy ions) cause lattice (or displacement) damage creating vacancies and interstitials. Gamma irradiation causes much less lattice damage. Lattice damage causes degradation of the component parameters. In bipolar transistors the most obvious effect is a reduction in the small signal current gain at low device currents. The main effect of ionising radiation is to produce trapped charges in oxide layers. Trapped charges can cause effects such as changes of resistance value and creation, or turning on, of unwanted devices such as parasitic transistors. The original intention was to produce working prototypes of devices that could if necessary be transferred to a radiation hard process, but to attempt to make the devices radiation hard by design.

The choice of components was deliberately limited to those expected to have good tolerance to the effects of radiation, npn bipolar transistors, polysilicon resistors and poly1-poly2 capacitors. This was based on previous design experience in similar junction isolated bipolar technologies and from information in published reports, e.g. [13-15]. Reasonable matching of closely spaced components was relied on, but the circuitry was designed to tolerate changes in the absolute values of passive components and the characteristics of transistors. A small family of very simple, current-mode, analogue and logic cells was designed. These cells, and complete circuits constructed from them, were shown to work in simulation with a wide range of component variation and transistor parameter degradation.

The npn bipolar transistors were operated at a relatively high current density where radiation damage was expected to produce the least effect on their characteristics. No radiation information was available for these devices at the time, but it was assumed that the radiation effects would be similar to those in devices made using other processes with comparable geometry and fabrication techniques. Some of the designs incorporated test devices which gave more information and validated the approach (see Section 6). Both of the ASIC designs were pad-bound so that there was plenty of space to separate components. Spacing was used to maximise the path length and minimise the effects of unwanted leakage paths. Other circuit and layout techniques were used to minimise problems caused by parasitic MOS and bipolar transistors.

Single event effects (SEE) causing bad data (soft errors) were minimised by reducing the area of the active devices and using simple circuitry with the smallest number of active components. By operating the transistors at high current density the deposited energy required to cause soft errors was maximised. The worst kind of single event

effects causing latch-up or burnout were guarded against by attention to detail in circuitry and layout. One method used was to ensure that there was sufficient series resistance in all paths to keep currents below the level that could cause damage. Long-term reliability was assured by designing metal tracking, contacts and vias to be run well below the manufacturers maximum current limits. These current limits were set to give good reliability at high operating temperature. For low operating temperature the reliability should be even better.

5. ASIC Designs

5.1 VDC

The VCSEL Driver Chip (VDC) translates the approximate LVDSⁱ signal produced by the ATLAS SCT front-end ASIC[1] into the drive signal required to operate the VCSEL. The input stage has a common mode voltage range exceeding the LVDS specification and works with signal amplitude range from less than the guaranteed minimum to greater than the nominal maximum. The input stage was over-designed to ensure correct operation, after irradiation, with poor quality input signals. The output driver had to produce a nominal 1mA dc bias current plus a variable switched current from 0 to 20mA. A control voltage input sets the switched current value. At full current the voltage drop across the VCSEL could be up to 2.5V. The supply voltage is $4V \pm 0.2V$ so the output driver stage has to work with only $\sim 1.3V$ across the current source and switching transistors. The data rate is 40 Mbits/s. The data stream is non-return-to-zero (NRZ) and the duty cycle could vary over a wide range so it was decided to make the output stage draw constant supply current. This approach uses more power but minimises disturbance of the supply and simplifies the decoupling. Two identical driver circuits were constructed on one substrate. The circuits are completely independent (apart from the common substrate) so one failed driver will not affect the other.

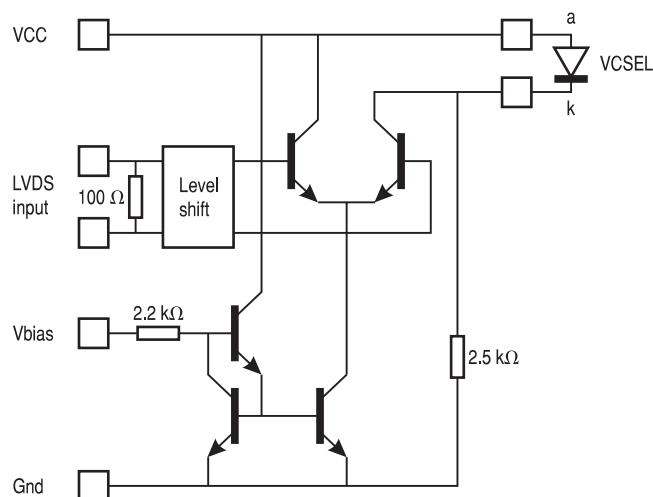


Figure 1 VDC Block diagram.

ⁱ Low Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI) Draft 1.3. IEEE P1596.3-1995

5.2 DORIC4

The DORIC4 ASIC decodes the biphasemark encoded TTC data and regenerates the 40 MHz clock and 40 Mbits/s data stream. This device was designed for use with a single PIN photodiode receiving a biphasemark encoded optical input signal. DORIC4 has a comparator input stage followed by clock and command decoding circuitry and LVDS output drivers, as shown in the block diagram in Figure 2.

The photodiode bias is applied to one signal input through a bias filter, the other signal input is taken through a resistor to ground. This produces a pair of pseudo-differential inputs that reject common mode noise. Inputs are AC coupled into the comparator; AC coupling automatically sets the threshold to half signal amplitude because the biphasemark signal input has 50% duty cycle. The signal input is expected to lie within the range 60 μ A to 600 μ A, but for extra safety margin the circuit was designed to work with signals from 40 μ A to 1mA. The comparator has a well-balanced, differential pair input stage with matched input resistors. Physical and thermal balance helps to minimise offset in the input stage but worst case offset could give a threshold variation of ± 5 μ A around the nominal mid-point. A small amount of offset was used in the comparator to prevent triggering on noise when no signal is present. (On a later version, DORIC4A, hysteresis is used rather than offset for better timing performance with low-level signals).

The clock and command signals are decoded from the received biphasemark signal as illustrated in Figure 3. The clock is decoded first and its duty cycle is adjusted to 50% by a delay-locked-loop. Three identical delay stages are used to produce the required total delay within the delay-locked-loop. Outputs from intermediate stages are used for internal timing and gating functions. The decoded clock is then used to detect and latch command signals. After switch-on the clock needs to be run for at least 1 μ s to allow the delay-locked-loop to settle before sending command signals. The internal gating is then set up to accept a data pulse as valid if it arrives within a 12.5 ns window (see Figure 3). Therefore a timing jitter of up to ± 6 ns will not cause errors in the decoded data.

The output stages translate the supply-line-referenced, differential outputs of the clock and command decoding circuitry to ground-referenced, LVDS compatible output signals. Well-balanced, differential outputs are needed to minimise feedback to sensitive inputs. LVDS outputs are ideal for signal transmission and may be easily translated into the correct signal levels to suit a wide range of logic families. Spare clock and command outputs allow operation of an adjacent module in case of failure of its own optical link. The outputs can be gated off when not in use. The single-ended gate inputs have a threshold of +2V and will work with low signals from -6 V to +1V, and high signals from +3V to +10V. Internal 20 k Ω pull-down resistors set the nominal operating conditions to normal outputs enabled and spare outputs disabled.

The whole circuit is designed to work from a nominal +4V ± 0.2 V supply. Internal filtering is used to minimise the effects of supply noise on the input stage. Other parts of the circuit are designed to tolerate supply noise and variation. The devices (VDC and DORIC4) are designed to be used as bare die, on a small hybrid assembly, with

the opto-electronic parts and decoupling components. The chips will be probe-tested for function while still on wafers. Wafers will then be sawn and picked for use.

DORIC4 block diagram

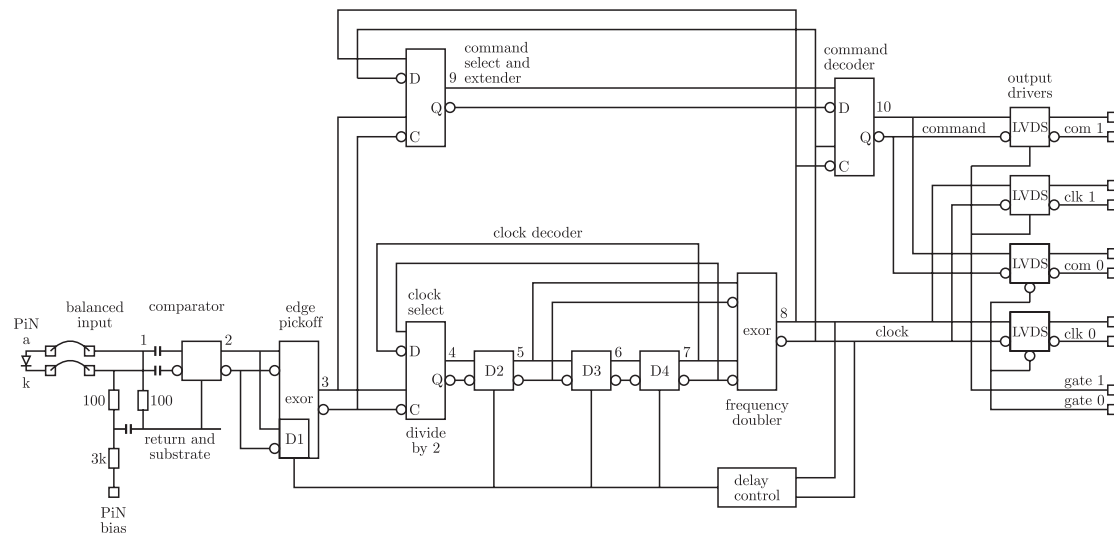


Figure 2 Block diagram for DORIC4

DORIC4 waveforms

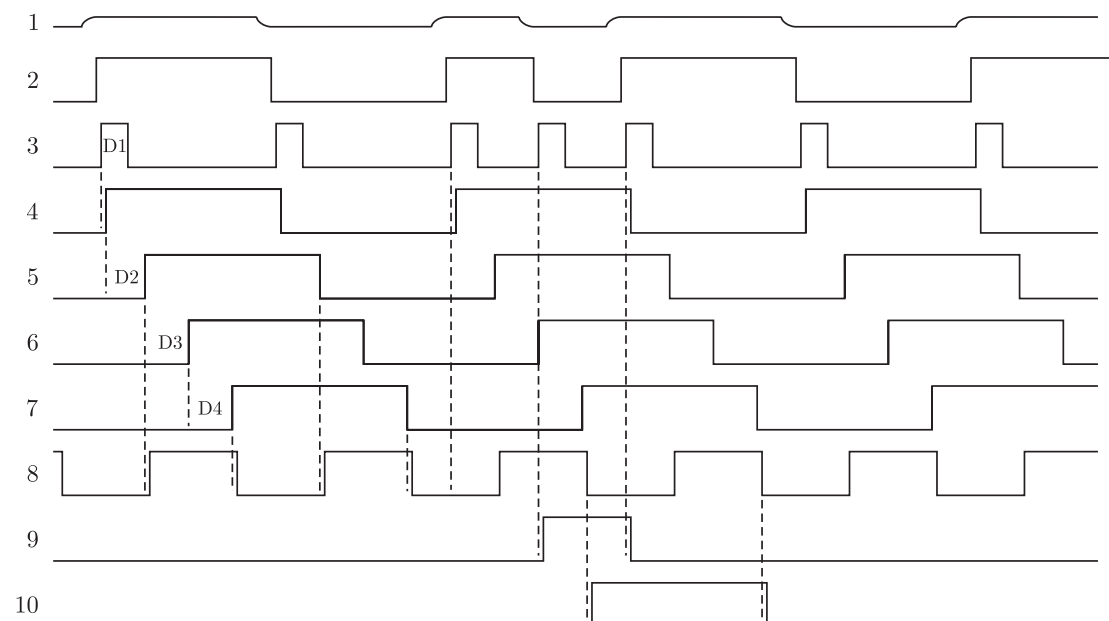


Figure 3 DORIC4 timing diagram. The signals are shown at different points in the circuit as marked on Figure 2

6. Radiation Results

A sample of 20 DORIC4 s and 9 VDCs ASICs were measured before irradiation on a probe station. The individual test transistors were measured on unirradiated VDCs in a DIL package. The VDC and DORIC4s were given an equivalent exposure of $2.5 \cdot 10^{14}$ n (1 MeV(Si)) cm^{-2} at the TRIGA reactor (see Section 3.1). This fluence is a factor

1.25 larger than the calculation of the expected fluences for the SCT quoted in Table 2 (see Section 2) which itself contained a 50% safety factor. The ASICs were not powered during the neutron exposure. The VDC and DORIC4s were re-measured on a probe station and then packaged so that they could be powered during the subsequent gamma irradiation. The dose received during the gamma irradiation was 100 kGy(Si). The currents drawn by the ASICs were monitored during the gamma irradiation, but no significant change in current was observed. The individual test transistors and resistors were measured on the VDC chips (after both neutron and gamma irradiation). The performances of the complete VDC and DORIC4 ASICs were also measured. Measurements were also performed to estimate the lifetime of the irradiated ASICs.

6.1 Test Transistors and Resistors

The test transistors and resistors were measured on unirradiated and irradiated VDC ASICs.

6.1.1 Test Transistors

The small signal DC current gain, h_{fe} , was measured as a function of collector current, I_C , on samples of transistors that were not irradiated and on samples that were irradiated. The results are summarised in Figure 4 below.

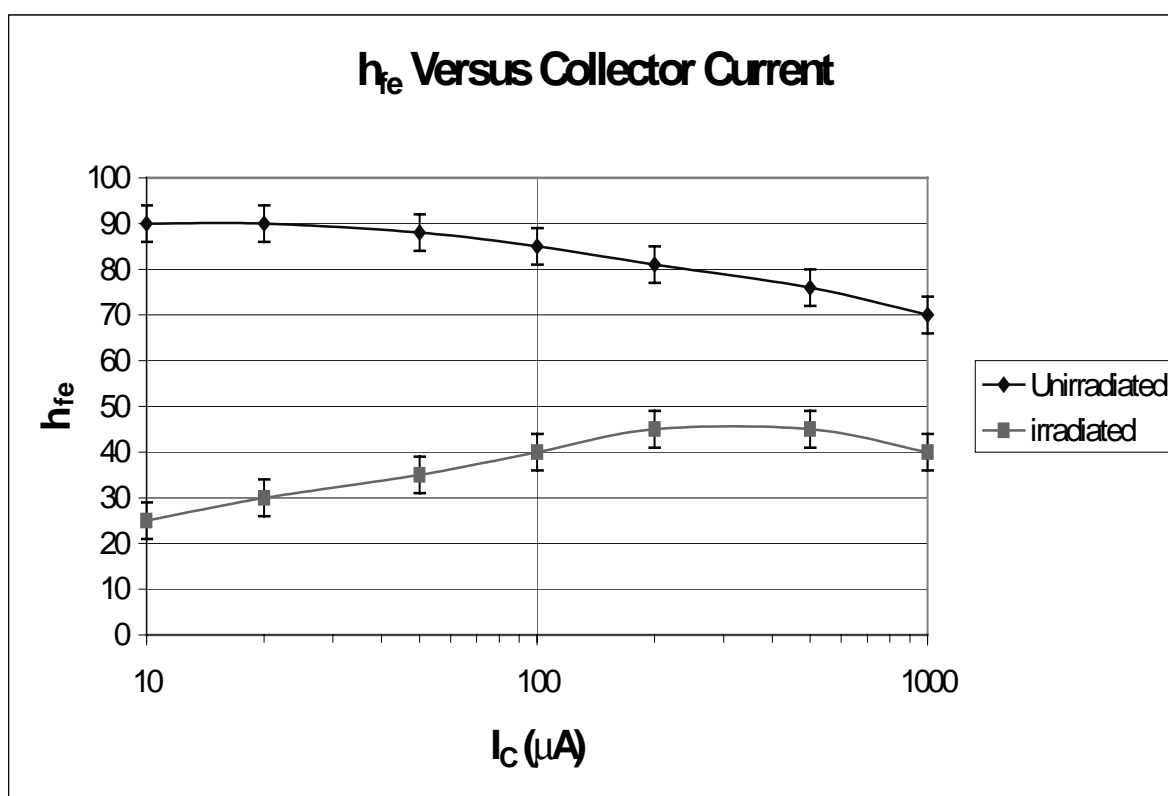


Figure 4 Measurements of small signal gain, h_{fe} , versus collector current for unirradiated and irradiated transistors.

The results for irradiated and unirradiated transistors are each based on measurements of the average of two transistors but other transistors on the same wafer showed very similar results. The fall of current gain at high current for the unirradiated devices is a normal feature. The fall of current gain at low values of collector current for the irradiated transistors is due to the radiation induced leakage current causing an increase in the base current (see Section 4). Note that the transistors in VDC and DORIC4 are operated at a value of $I_C=125\ \mu\text{A}$ at which the current gain h_{fe} after irradiation is equal to about 45. Given that the simulations of DORIC4 and VDC showed that the ASICs worked with h_{fe} values as low as 10, then the complete DORIC4 and VDC ASICs would be expected to work after irradiation with no significant degradation in performance.

The gamma irradiation was performed at a rate 73 times higher than that expected in ATLASⁱ. Therefore the effects of the same exposure at a lower rate might be larger. However recent results have suggested that the rate dependent effects are small provided that there is sufficient annealing time between the end of the exposure and the measurements[17]. Given the large difference between the measured and allowed degradation, the ASICs would still be expected to work correctly even if there was a large rate dependent effect on the radiation damage.

6.1.2 Resistors

The resistances of test resistors and of resistors in the main VDC ASIC were measured on unirradiated and irradiated VDC ASICs (irradiated with neutrons and gammas as described above). The results are given in Table 2 below.

Table 2 Measured resistance for unirradiated and irradiated ASICs.

Nominal Resistance (k Ω)	Unirradiated Resistance (k Ω)	Irradiated Resistance (k Ω)	Resistor powered during gamma irradiation	Chip Number
5.025	5.04		-	1
5.025	5.06		-	1
5.025		5.40	No	2
5.025		5.44	No	2
5.025		5.14	No	3
5.025		5.16	No	3
2.512	2.46		-	1
2.512	2.48		-	1
2.512		2.68	Yes	2
2.512		2.52	Yes	3
2.512		2.50	Yes	3

The matching tolerance between resistors on the same chip is ~1% as expected and this is not significantly deteriorated by irradiation. It is not possible to deduce the precise change in resistance with radiation as no measurements were made on the same resistors before and after irradiation. However the indication from the data is

ⁱ The neutrons produce bulk damage only, so there are not expected to be any rate dependant effects.

that the change is less than 10% which is smaller than the expected process variation. Therefore any changes in resistor values are not expected to be a problem for either DORIC4 or VDC.

6.2 Complete ASICs

Simple functionality tests were performed on the unirradiated and irradiated DORIC4 and VDC ASICs.

6.2.1 DORIC4 Tests

The DORIC4s were powered and electrical signals were used to simulate the current from a PIN photodiode. An electrical signal was fed separately into each DORIC4 input. The amplitude of the signal was chosen to simulate the signal out of an irradiated PIN diode for an optical signal of amplitude equal to 200 μW , i.e. the minimum signal given in the specifications for DORIC4. A simple BiPhase Mark generator was used to encode data onto a 40 MHz clock. A burst of 7 “ones” was sent every 128 clock cycles. The recovered 40 MHz clock and the decoded data stream were checked with an oscilloscope. The recovered clock signal was checked for pulse distortion before, during and after the burst of data. All 20 DORIC4s passed these functionality tests before irradiation. All these ASICs passed the same functionality testing after the neutron irradiation and after the gamma irradiation. A more complete test of the analogue performance of the previous version of the DORIC4 ASIC (DORIC3) showed that there was no significant increase in noise after irradiation and the irradiated DORIC3 functioned correctly inside an ATLAS SCT TTC link [2].

6.2.2 VDC Tests

The VDC chips were powered and the inputs driven with a 20 MHz LVDS clock signal. The outputs were measured with an oscilloscope. The amplitude of the LVDS input signal was varied over the minimum to maximum LVDS allowed range. An offset voltage of $\pm 1\text{V}$ was applied to check the common mode range. A scan of current output versus voltage setting was performed to verify that the output amplitude could be adjusted over the full range. The speed of the output pulse was checked with an oscilloscope. All 9 VDC ASICs worked correctly before irradiation and all 9 worked after the neutron irradiation. Two of the VDCs were mechanically damaged during packaging between the neutron and gamma irradiation and on these two ASICs only one channel worked correctly after the gamma irradiation. For the undamaged chips both channels on the remaining 7 ASICs worked correctly after the gamma irradiation.

6.3 Lifetime After Irradiation

The SCT has to operate reliably for 10 years with little or no maintenance. Therefore the lifetime of the ASICs has to be long enough to ensure that there will be a negligible failure rate during this period. From the manufacturer’s data[16] the lifetime of the ASICs is expected to be very long at the low operating temperatures in the SCT. The designs have tried to optimise the lifetime by operating the ASICs at currents much lower than the maximum allowed values. There was a possibility that

the lifetime of the ASICs would be greatly reduced by the effects of irradiation, therefore it was essential to estimate the lifetimes of the ASICs after radiation.

The effects of early failures (“infant mortality”) of ASICs in their operation can be screened out by performing burn-in tests. In order to determine the lifetimes of ASICs that survive the burn-in tests, accelerated life testing of microelectronics can be performed by tests at elevated temperatures[18,19]. Accelerated ageing tests were performed on samples of the irradiated ASICs in order to estimate the lifetime of the ASICs in the ATLAS radiation environment. A sample of 10 of the irradiated DORIC4 ASICs were operated for 168 hours at a temperature of 100 °C (monitored by a thermocouple attached to one of the packages). The ASICs were all powered and clocked correctly during the accelerated ageing test. All 10 DORIC4s passed the functionality testing after this period. According to the Arrhenius equation, this gives an accelerated ageing factor of

$$AF = \exp\{E_a / kT_1 - E_a / kT_2\}$$

The activation energy E_a for microelectronics is conventionally taken to be 1.0 eV[20] but the manufacturer’s quote a value of 0.7 eV[16]. However as the manufacturer’s data refer to ASICs operated under harsher environmental and operating conditions than in ATLAS, a value of 0.8 eV will be used here. The expected operating temperature in the SCT is around 0 °C, therefore the equivalent operating time in ATLAS is $9 \cdot 10^4$ days. Assuming the detector operates for 100 days a year[1] this implies at 90% confidence level, the percentage of ASICs that would be expected to fail in the 10 years of LHC operation is less than 0.3%. The ATLAS SCT readout uses redundancy to ensure immunity to single point failure[1]. Therefore the loss of efficiency resulting from such a low failure rate would be negligible.

7. Conclusions

A set of simple design rules has been found to use npn transistors in the AMS 0.8 µm BiCMOS process to produce radiation tolerant ASICs. The designs of the VDC and DORIC4 ASICs to be used in the ATLAS SCT optical readout chain have been explained. Radiation testing of test structures and complete ASICs have shown that they can survive the ATLAS SCT radiation environment for 10 years of LHC operation. Accelerated ageing testing of the ASICs after irradiation has shown that the device lifetimes are suitable for 10 years of LHC operation.

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References

1. ATLAS Inner Detector Technical Design Report, CERN/LHCC/97-16/17.

- 2.** D.G. Charlton et al., System Test of Radiation Hardness of Optical Links for the ATLAS SemiConductor Tracker, Nucl. Inst. and Meth. A443 (2000) 430.
- 3.** J.D. Dowell et al., Irradiation tests of photodiodes for the ATLAS SCT readout, Nucl. Inst. and Meth. A 424 (1999) 483.
- 4.** D.G. Charlton et. al., Radiation Hardness and Lifetime Studies of Photodiodes for the Optical Readout of the ATLAS SCT, submitted to Nucl. Instr. And Meth. A.
- 5.** J. Beringer et al., Radiation Hardness and Lifetime Studies of LEDs and VCSELs for the Optical Readout of the SCT, Nucl. Instr. Meth. A 435 (1999) 375.
- 6.** D.G. Charlton et al., Radiation Tests of Optical Link Components for the ATLAS SCT, proceedings of the 4th Workshop on Electronics for the LHC, Rome 21st-25th September 1998, CERN/LHCC/98-36.
- 7.** G. Mahout et al., Irradiation Studies of Multimode Optical Fibres for use in ATLAS Front-end Links, accepted for publication in Nucl. Instr. And Meth. A (1999).
- 8.** A. Chilingarov et al., Radiation damage due to NIEL in GaAs Particle Detectors, ATLAS Internal Note INDET-NO-134, June 1996.
- 9.** E.A. Burke et al., IEEE Trans. Nul. Sci 34 (1987) 1220.
- 10.** G.P. Summers et al., IEEE Trans. Nucl. Sci 40 (1993) 1372.
- 11.** D. Žontar et al., Nucl. Instr. and Meth. A426(1999) 51.
- 12.** G.C. Messenger and M.S. Ash, "The effects of Radiation on Electronic systems", p 377, Van Norstran Reinhold, New York 1986.
- 13.** R.N. Nowlin et al., IEEE Trans. Nul. Sci 40 (1993) 1686.
- 14.** SCT Technical Proposal Backup Document, ATLAS-INDET-N0-085.
- 15.** M.A. Baturutsky et al., Charge-sensitive preamplifier IC for silicon calorimetry at colliders, Nucl. Instr. And Meth. A352 (1995) 604.
- 16.** AMS report available on www at url: www.ams.int/quality/
- 17.** D. Dorfán et al., Measurement of Dose Rate Dependence of Radiation Induced Damage to the Current Gain in Bipolar Transistor, presented at the IEE Nuclear Science Symposium, November 8-14 November 1998, Toronto. Preprint SCIPP 98/02 available on www at url: http://scipp.ucsc.edu/~hartmut/IEEE_98/N17-3-record.ps.
- 18.** F. Jensen and N.E. Peterson, Burn-in: an engineering approach to the design and analysis of burn-in procedures, J. Wiley and Sons, 1986.
- 19.** H.S. Blanks, The Temperature Dependence of Component Failure Rate, Microelectronics Reliability, 20 (1980) 297.
- 20.** MIL-STD-883B. Available on www at url: <http://www.dsccl.dla.mil/programs/milspec/ListDocs.asp?BasicDoc=MIL-STD-883>.